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AND8343/D

NIS5132/5 Demo Board

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General Description

The NIS5132 and NIS5135 electronic fuses are monolithic, integrated circuits that offer superior protection for overcurrent, overvoltage The NIS5132 is designed for 12 volt systems while the NIS5135 is designed for 5 volt systems. These two chips can be easily interfaced for systems that include both a 5 and a 12 volt bus. By tying the enable pins together both units will shutdown if either unit encounters a fault condition.

This board can be used to examine the behavior of either unit individually or both units together. A set of jumpers is provided to allow the enable pins to be connected or disconnected from each other.

Parts Selection

There is a pad on the board for a ceramic capacitor on the input. This capacitor is not required for operation, but is available in the event that there will be some system capacitance that is desired to be duplicated.

The current limit resistor is a small chip resistor. Since the current in this resistor is very low, most small chip resistors will be suitable. The power dissipation is based on a voltage drop of approximately 70 mV or:

$$P_{R-Limit} = 0.07\ V^2 \times R_{\_Limit}$$

The dv/dt capacitor, if used, should be a ceramic capacitor.

Application of Power

If two parts are mounted to the board, either device can be tested or both can, and the devices can be powered up in any order. Once power is applied, the output will ramp up with a controlled slew rate. If there is no capacitor on the dv/dt pin the output voltage will reach the input voltage in about 2 ms. If an external capacitor is connected to the dv/dt pin the capacitor required for the desired time for the output to reach the input will be:

$$C_{ext} = \frac{t_{0-5}}{30e6} - 50\ pF \qquad \text{for 5 V device}$$

$$C_{ext} = \frac{t_{0-12}}{24e6} - 50\ pF \qquad \text{for 12 V device}$$

So if the output of the 12 volt device was to be ramped from 0 to 12 volts in 50 ms, the required capacitor would be:

$$C_{ext} = \frac{50\ ms}{24e6} - 50\ pF = 2\ nF$$

The dv/dt circuit will control the turn on time unless the current required to do so exceeds the short circuit current limit setting of the chip, in which case the current will be limited to the lower level and the turn on time will increase.

It is not advisable to connect any circuitry to the dv/dt pin other than a ceramic (or other low leakage) capacitor. The internal current source that charges the capacitor can provide 13 μA so even an oscilloscope probe connected to this pin can have a noticeable impact on the operation of this circuit.

Protection Features

Current Limit

These eFuses employ a two level current limit circuit. A resistor selection chart is available in the data sheet for the appropriate device. At turn on, when the gate of the power MOSFET is controlling the current through the device, it will be operating in the short circuit current limit mode, which is the lower of the two curves.

Once the FET is fully enhanced the current limit circuit will shift to the overload (or upper) curve. In this mode of operation, the device will not current limit until the current reaches the level of the overload curve. Once this current level has been reached, the current limit will automatically reduce to the short circuit level. For a more detailed description of how this circuit functions please refer to application note AND8140/D.

To test the short circuit current limit the chip may be turned on into a short. The overload current limit level is tested by starting up the chip into a load that is less than the short circuit current level. While the chip is operational, increase the load current until the current level falls to the short circuit level. The highest current reached before the current dropped off is the overload level.

Overvoltage Clamp

The output bus is protected from input surges by an active clamp that limits the maximum output voltage. This circuit does not shut down the chip but rather, it acts as a linear regulator.

This feature can easily be tested by simply increasing the input voltage and watching the level of the output voltage. When the output voltage stops increasing the limit has been reached. Depending on the load current, the device may shut down due to its die temperature reaching the thermal limit level.

UVLO

The purpose of the internal Under Voltage Lockout circuit is to assure that the chip performs properly when powered up. If the input voltage drops below a level where the internal circuits function properly, the UVLO will shut off the chip and hold it off.

To test this, reduce the input voltage until the output goes low. There should be no odd behavior during the shut down.

Thermal Shutdown

The die of the power MOSFET is protected by a thermal sensing circuit. This is the only internal circuit that can shut down the chip. There are two thermal versions of this eFuse which can either latch the output off until restarted, or allow for an automatic restart.

The auto-retry devices will shut down the output when the thermal limit is reached and enable the output when the die cools down 40°C. The latching devices will disable the output until power is recycled to the chip or the enable signal is pulled low and then released.

To test this function, short the output to ground either with power applied or before power is applied. The latching part will operate until it reaches thermal limit and then shut down. It can be restarted by either of the methods described above. The auto-retry devices will pulse the output until the short is removed.

Enable

These devices incorporate a novel, three-state signal to control the device. In the high state (V_{enable} > 3.30 V) the output will be enabled.

If a thermal fault occurs, the output will be set to the intermediate state (0.82 < En_{mid} < 1.97). In this state the output is off. This signal can be monitored to determine if a thermal fault has occurred.

To reset the device, or to inhibit operation, the enable pin must be pulled to a level of 0.35 volts or less.

To check the intermediate level, short the output as explained above and note the level of this pin while the output is in its disabled state.

To shut the unit down via the enable pin, apply a voltage of 5 to 10 volts at the “Enable Control” test point. If this point is open or grounded, the enable signal will be high and the units will function normally.

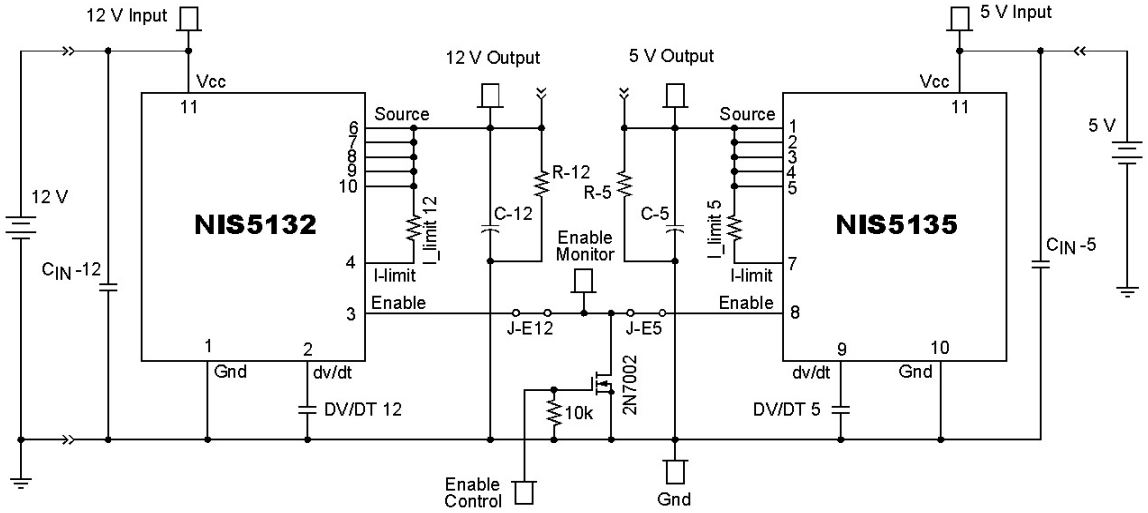

Figure 1. Demo Board Schematic

Board Features

Banana jacks are provided for easy attachment of power sources and loads. Test points are also included at many nodes in the circuit.

The enable function of these devices allows for simultaneous shutdown due to an enable shutdown or thermal shutdown. Jumpers J-E12 and J-E5 allow either or both units to be connected to the enable interface transistor (2N7002). To observe the individual operation of a device, remove the jumper for the opposite part. i.e. If the NIS5132 is being tested remove the J-E5 jumper so that the enable signal will only interact with the NIS5132 chip.

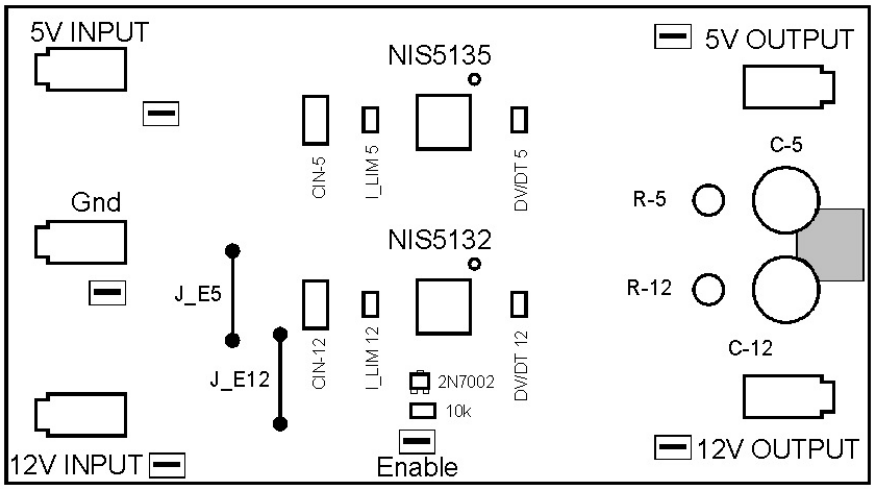

Figure 2. Demo Board Layout

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