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Power Dissipation in Case of Bus Failure

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APPLICATION NOTE

AMIS−30660 High Speed CAN transceiver is designed to withstand bus failures. Without any damage to the IC the CANH or CANL line may be shorted to ground, V_{CC} or the battery supply. However in some bus failure conditions an increase in power dissipation might occur. This will lead to a rise in junction temperature.

Two bus states can be distinguished: recessive and dominant. In both states both CANH and CANL can be shorted to GND, V_{CC} or V_{BAT}. In this application note we are investigating the worst case conditions therefore short to V_{CC} is not discussed.

Recessive State

In the recessive state TxD = 1 and both CANH and CANL drivers are disabled. The figure below illustrates the equivalent schematic. R_{BUS} is the total impedance of the (split) termination on both end−sides of the CAN bus. The typical value is 60 Ω. $R_{i,cm}$ is the common mode input impedance with a typical value of 25 kΩ. V_{CC} is the 5 V supply. Without power (V_{CC} = 0 V) the common mode voltage is still kept by a passive clamp but can be higher than $V_{CC}/2$. This particular condition is not taken into account in the calculations.

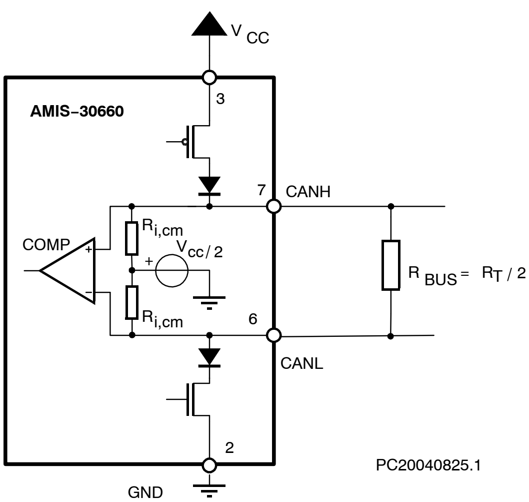

Figure 1. Equivalent Schematic in Recessive State

The power dissipation for the different bus−error conditions is given in the table below.

Table 1. POWER DISSIPATION FOR CAN−BUS ERRORS IN RECESSIVE STATE

BUS	Short to	
	GND	V_{BAT}
CANL	$P \approx = \frac{V_{CC}^{\ 2}}{2R_{i,cm}}$	$P \approx = \frac{2(V_{BAT} - V_{CC}/2)^2}{2R_{i,CM}}$
CANH	$P \approx = \frac{V_{CC}^{\ 2}}{2R_{i,cm}}$	$P \approx = \frac{2(V_{BAT} - V_{CC}/2)^2}{2R_{i,CM}}$

Calculated for V_{CC} = 5 V, V_{BAT} = 24 V, $R_{i,cm}$.= 25 kΩ and R_{BUS} << $R_{i,cm}$ yields in:

Table 2. CALCULATED POWER DISSIPATION FOR CAN−BUS ERRORS IN RECESSIVE STATE

BUS	Short to	
	GND	V_{BAT}
CANL	0.5 mW	37 mW
CANH	0.5 mW	37 mW

Dominant State

In dominant state TxD = 0 and both drivers are active. In case of a short circuit the currents for both CANH and CANL are limited to $I_{o(sc)}$ which is 120 mA in worst case condition. The figure below illustrates the equivalent schematic.

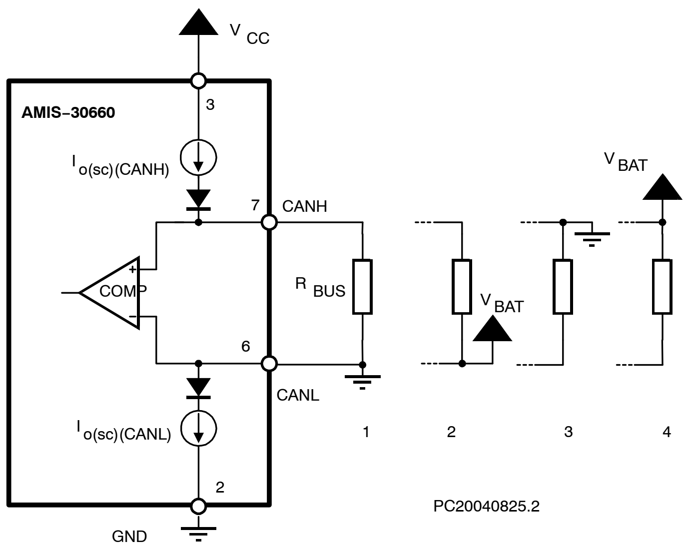

Figure 2. Equivalent Schematic in Dominant State

The power dissipation for the different bus−error conditions is given in the table below.

Table 3. POWER DISSIPATION FOR CAN−BUS ERRORS IN DOMINANT STATE

BUS	Short to	
	GND	V_{BAT}
CANL	• See Figure 2 Case (1) • Bus communication possible but with bit timing limitations	• See Figure 2 Case (2) • Both CANL / CANH are on V_{BAT} level through R_{BUS} ♦ No communication possible ♦ Time−out by master
	$P = \frac{V_{O(dom)CANH}(V_{CC} - VSubO(dom)CANH)}{R_{BUS}}$	$P = V_{BAT} \cdot I_{O(sc)(CANHL)}$
CANH	• See Figure 2 Case (3) • Both CANL / CANH are on GND level through R_{BUS} → ♦ No communication possible ♦ Time−out by master	• See Figure 2 Case (4) • Bus communication possible but with bit timing limitations
	$P = V_{CC} \cdot I_{O(sc)(CANH)}$	$P = V_{BAT} \cdot I_{O(sc)(CANL)} - R_{BUS} \cdot I_{O(sc)(CANL)}{}^2$

Calculated for V_{CC} = 5 V, V_{BAT} = 24 V, R_{BUS}.= 60 Ω, $I_{o(SC)(CANL)}$ = 120 mA, $|I_{o(SC)(CANH)}|$ = 95 mA and $V_{o(dom)CANH}$ = 3.6 V yields in:

Table 4. CALCULATED POWER DISSIPATION FOR CAN−BUS ERRORS IN DOMINANT STATE

BUS	Short to	
	GND	V_{BAT}
CANL	84 mW	2.88 W (Note 1)
CANH	475 mW	2.02 W

1. Because no communication is possible, the master (depending on the application software) will cease the communication (= permanent recessive state) and the dissipated power drops to 37 mW.

Average Power Dissipation and Related Increase in Junction Temperature

The worst case condition from application point of view is a short to V_{BAT} on the CANH pin in dominant state. Communication is still possible but the dissipation is 2.02 W giving the boundary conditions as stipulated in Table 4.

Calculating with a duty cycle of 50% (meaning 50% of the transmission time the bus is in dominant state) the average power dissipation is 1.01 W (neglecting the 37 mW dissipation in recessive state)

The thermal resistance of the package is 150 K/W in free air. Soldered on a 2 layer PCB $R_{th(vj-a)}$ < 100 K/W is expected. Calculating with 100 K/W yields in a worst case expected temperature increase of 101°C.

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