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PCB Layout Guidelines for High Frequency Signaling Products

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APPLICATION NOTE

INTRODUCTION

There is an increase of devices and circuitry in usage of high speed, low consumption, small volume and lower interference. Hence PCB design is an important stage of electronic product design. It forms a connection between function and electronic components, and is also an important part of power circuit design. High frequency circuit has the higher integration and the higher layout density, making it necessary to know how to make layout more reliable. The use of multilayer board becomes a necessity and an effective means to reduce cross interference of signals, better grounding and lower parasitic inductance.

This application note looks at the different layout types, practices and guidelines, types of material and factors influencing the high frequency signal transfers.

The aim of the design of the PCB is to achieve:

- Lower On−board Noise Generation due to Distributed Power Network
- Least Cross−talk between Traces
- Reduction of Ground Bounce Effect
- Best Impedance Matching
- Provide Correct Signal Line Termination

PCB TRANSMISSION LINE LAYOUT TYPES

A high−frequency signal that propagates through a long line on the PCB from driver to receiver is affected by the loss tangent of the dielectric material. More the loss tangent means higher dielectric absorption leading to increased attenuation at higher frequencies. Transmission line is a trace, with combination of resistance, inductance and capacitance.

Any circuit trace on the PCB has characteristic impedance associated with it. This impedance is dependent on trace width, thickness, dielectric constant of the material used and height between the trace and reference plane. The impedance is inversely proportional to trace width and directly proportional to trace height above the ground plane.

There are two types of transmission line layouts: Microstrip and Stripline. Refer Figure 1 and 2.

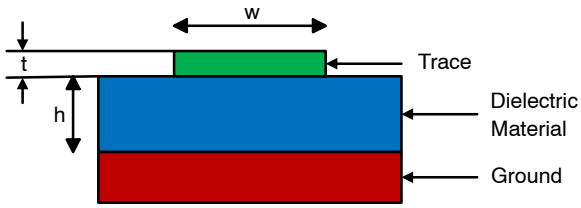

Figure 1. Microstrip Transmission Line Layout

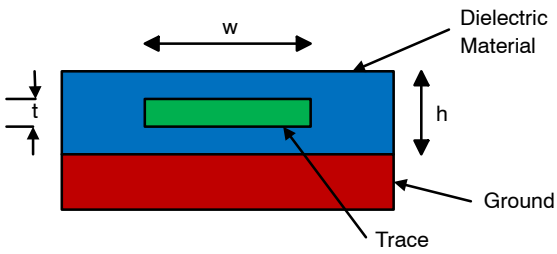

Figure 2. Stripline Transmission Line Layout

Where:
w = width of trace,
t = thickness of trace,
h = height of Dielectric

A circuit trace routed on an inside layer of the PCB with two low−voltage reference planes (such as, power and/or GND) forms a stripline layout. The rate of change with trace height above GND is much slower in a stripline layout compared with a microstrip layout. To achieve the same impedance, the dielectric span must be greater in stripline layouts compared with microstrip layouts. Hence stripline layout PCBs with controlled impedance lines are thicker than microstrip layout PCB.

FACTORS TO BE CONSIDERED FOR PCB LAYOUT

Crosstalk and How to Minimize

Crosstalk is the unwanted coupling of signals between parallel traces. Crosstalk refers to unexpected voltage noise interference on adjacent transmission lines as a result of electromagnetic coupling when signals are being transmitted on transmission lines. Proper routing and layer stack− up through microstrip and stripline layouts can minimize crosstalk.

Steps to Reduce/Minimize Crosstalk

- Increase the spacing between signal lines as much as possible. Traces distance must be at least three times the dielectric height.
- To help de−couple from adjacent signals, the signal traces must be close to the ground plane. Lower the distance between the trace and the ground plane to under 10 mils. Ensure the distance between the centers of two adjacent traces be at least four times the trace width.
- The clock line should be perpendicular to the key signal lines rather than parallel.
- Terminate clock signals to minimize reflection.
- Use differential routing techniques where possible.
- To reduce coupling, route single−ended signals on different layers perpendicular to each other.

Signal Integrity and Ways to Improve

Follow the Below Guidelines for Single−ended Trace

- Keep the traces as straight and of minimum length as possible. Where traces needs bending (due to component or PCB), use arc−shaped traces of 45° angle instead of right−angle bends. Figure 3 and 4 below shows examples of proper and improper ways of trace routing respectively.
- Do not use multiple signal layers for clock signals.
- Do not use via in clock transmission lines as it can cause impedance change and reflection.
- Place a ground plane next to the outer layer to minimize noise. If a clock trace is used in an inner layer, then place it between two reference planes.
- Terminate clock signals to minimize reflection.

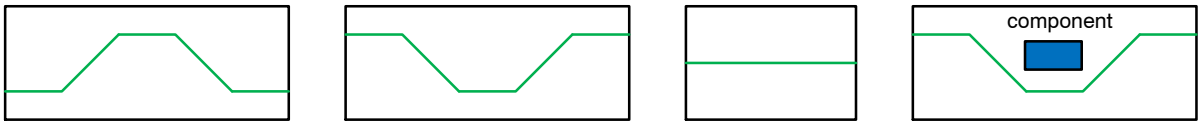

Figure 3. Proper Ways of Trace Routing

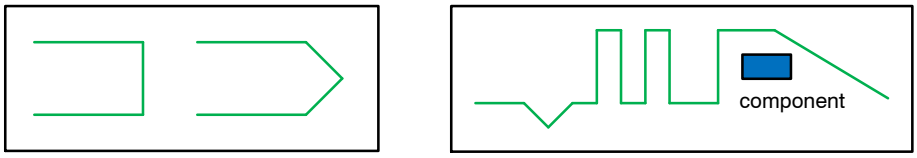

Figure 4. Improper Ways of Trace Routing

Follow the Below Guidelines for Differential Traces

- Keep the distance between the differential pair traces equal over the entire trace length. Keep the distance between the differential traces at least thrice the dielectric height for lower reflection noise. Ensure the distance between two differential pairs is at least twice that of the distance between the differential traces (or six times the dielectric height). Refer Figure 5 indicating the distances.
- Avoid multiple via to prevent impedance.
- Ensure the length of the two traces are equal. If not possible difference in length should be < 5mil. Add additional length close to the mismatched ends.
- Keep the traces as straight as possible. Where traces needs bending (due to component or PCB), use arc−shaped traces of 45° angle instead of right−angle bends uniformly following for both the traces. Figure 6 and 7 below shows examples of proper and improper ways of trace routing respectively.

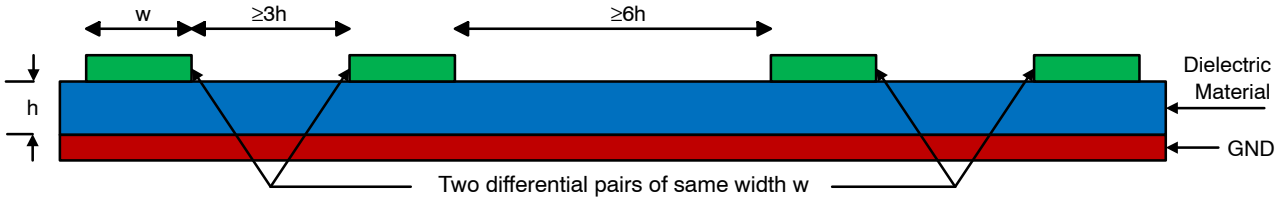

Figure 5. Distances that Need to be Maintained between the Traces

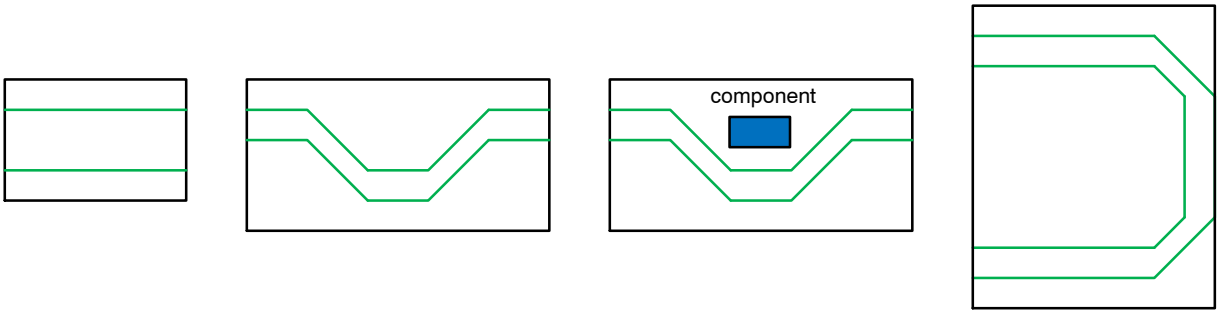

Figure 6. Proper Ways of Trace Routing

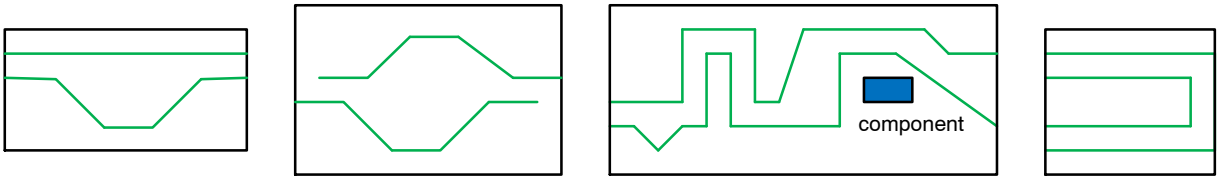

Figure 7. Improper Ways of Trace Routing

Layout Options to Reduce Ground Bounce

Ground bounce phenomena at board level occurs due to multiple outputs switch at faster times with higher transient currents as they discharge load capacitances. Key lies in reduction of the parasitic inductance along the switching path.

- Use wide, short traces between the Vias and capacitor pads, or place the Vias next to the capacitor pad. Use bigger size Vias to connect the capacitor pad to the power and ground plane to minimize the inductance in decoupling capacitors. Use low ESR and ESL surface mount capacitors to minimize the lead inductance. It is preferable to have multiple value capacitors in parallel close to each other.
- Traces from power pins to a power plane must be wide and short reducing inductance and voltage drops.
- Connect each ground pin or via to the ground plane individually. Avoid Daisy chain connection.
- Add the recommended decoupling capacitors for as many VCC/GND pairs as possible placing them close to the power and ground pins of the device.
- Do not leave the unused I/O pin float or open. Connect these as an output pin pulled to GND or VCC.
- Eliminate sockets whenever possible.
- Distribute the number of outputs that are going to switch simultaneously evenly throughout the device.
- Use multi−layer PCBs that provide separate VCC and ground planes to reduce trace inductance.
- Place the power and ground pins next to each other.
- Note that Wire wrapping the VCC and ground supplies usually increases the amount of ground bounce.

Recommendations for Power Plane Distribution

You can use power planes on multi−layer PCBs for VCC and GND to the devices. Because the power plane covers the full area of the PCB, its DC resistance is very low. The power plane maintains VCC and distributes it equally to all devices while providing very high current−sink capability, noise protection, and shielding for the logic signals on the PCB.

- Use lower planes to distribute power.
- Separate analog and digital power planes. If not possible, use split planes partitions.
- Ensure the analog and digital components are placed only over their respective ground planes.
- Use ferrite beads to isolate the two power planes. The power plane must be less than ground plane around the board edge by ≥ 20 times thickness of dielectric material to avoid fringing RF radiation.

Characteristic Impedance, Impedance Matching, Reflections and Termination Methods

Impedance and Reflections

Characteristic impedance is an important parameter in impedance matching that influences reflection, over shoot and under shoot and directly relates with integrity of high−speed signal transmission.

Mismatched impedance causes signals to reflect back and forth along the lines, which causes ringing at the load receiver. The ringing reduces the dynamic range of the receiver and can cause false triggering.

During the transmission process, when the impedance does not match, the signal will be reflected in the transmission channel, which will make the main signal overshoot, causing the signal to fluctuate near the logical threshold.

The basic method to eliminate reflection is to make the load impedance and characteristic impedance of the transmission signal match. As the difference between the load impedance and the characteristic impedance of the transmission line is larger, the reflection is larger, so the characteristic impedance of the signal transmission line should be equal to the load and impedance as much as possible.

When the transient impedance along transmission lines is a constant value, this value is regarded as the characteristic impedance on transmission lines. For micro strip lines and strip lines on PCB, their characteristic impedance are calculated using dedicated tools.

To eliminate reflections, the impedance of the source must equal the impedance of the trace as well as the impedance of the load. The radiation intensity of the signal is directly proportional to the routing length of the signal line. The longer the high−frequency signal lead is, the more easily it can be coupled to its components. Therefore, for high frequency signal lines such as signal clock, crystal oscillator, DDR data, LVDS, USB and HDMI, the shorter the routing length is required, the better.

PCB Layout Recommendations

- Digital ground and analog ground should be divided on PCB with mixed signals.
- Analog and digital electronic components are separated with analog ground distributed in analog area and digital ground distributed in digital area.
- Analog ground and digital ground are connected with magnetic beads to be capable of implementing the separation between digital ground and analog ground.
- High−speed signal lines should be on the top surface of PCB and holes/Vias should be avoided.
- Impedance matching of 50 Ω should be carried out at single terminal routing and impedance matching of 100 Ω is required for differential routing.

Termination Methods

Aim is to have impedance compatibility where characteristic impedance on signal transmission path constant. So the reflection coefficient must be nil, which means no reflection on transmission path.

There are two ways of termination − Source and End termination. Source termination uses a series resistor in transmission lines at positions close to near−source end. The intention is to stop the second reflection of transmission lines. End termination uses a pull−up or pull−down resistor positioned close to load terminal in order to implement impedance matching.

Refer to the Figure 8 and 9 below that shows the termination implementation.

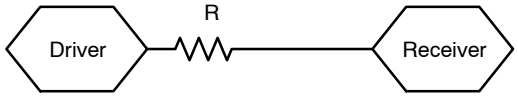

Figure 8. Source Termination

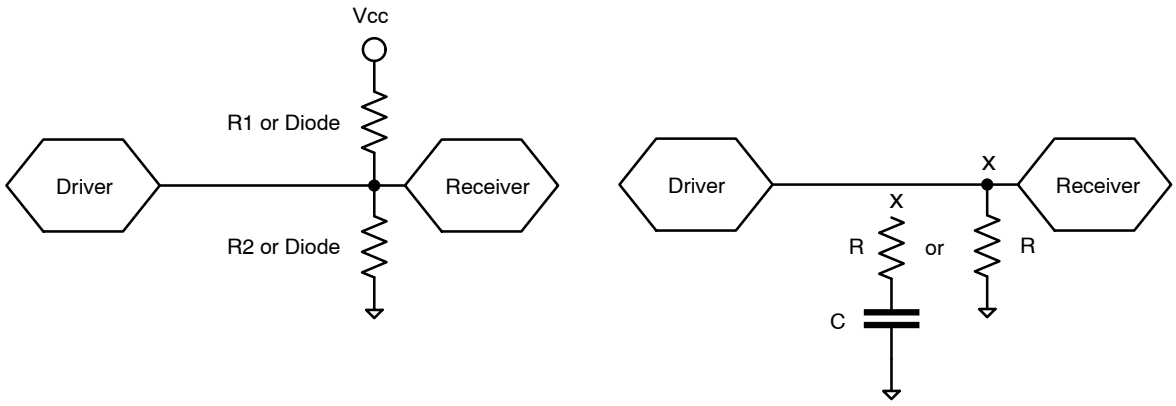

Figure 9. End Termination

PCB Material and Multi−layer Stack Up

PCB Material

The needed PCB build−up depends on the component packages used, required signal trace density, and impedance matching requirements. The High speed boards with a multilayer PCB having ground and power supply planes is mandatory. Solid copper planes allows to keep the device ground and power connections short. The ground plane offers low inductance return paths for the high speed signals.

Though FR−4 PCB laminate material is widely used, it is economical for frequencies below 1 GHz beyond which high speed digital signal will be affected by the parameters of the printed circuit board laminate that it travels on.

Dedicated high speed laminates like *Rogers RO4350* have better properties at higher frequencies > 1 GHz. This is a high frequency, high−temperature material known for good impedance consistency. The relative dielectric constant of the *Rogers RO4350* material is constant (roughly 3.5) from 0 up to 15 GHz. Alternative to Rogers is the Nelco or SI or Megtron material type.

A signal moving on the PCB will have a speed that is dependent on the dielectric constant of the printed circuit board. If dielectric constant varies with frequency, then different frequency components of the signal will reach the load at different times causing distortion of the digital signal. The signal losses due to PCB material increase with frequency. Again, each harmonic of the digital signal will be attenuated according to that frequency of operation. Increased loss of the signal components will add to the distortion of the digital signal. Printed circuit board layout is often the single most important factor affecting the electromagnetic compatibility of electronic systems.

Multi−layer Stack Up Recommendations

- The signal layer should be placed adjacent to a plane layer to provide the signals with a good return path.
- All of the high speed signals should be on the inner layers of your board between planes to provide shielding against any external emitted radiation.
- Multiple ground planes should be used in the layer stack up to lower the reference impedance and reduce common−mode radiation from affecting the circuit. The noise generated by four−layer board is ~20 dB lower than that by 2−layer board.
- Ensure VCC and Ground plane are on one complete plane.

Figure 10 below shows an example of the 6 layer stack up.

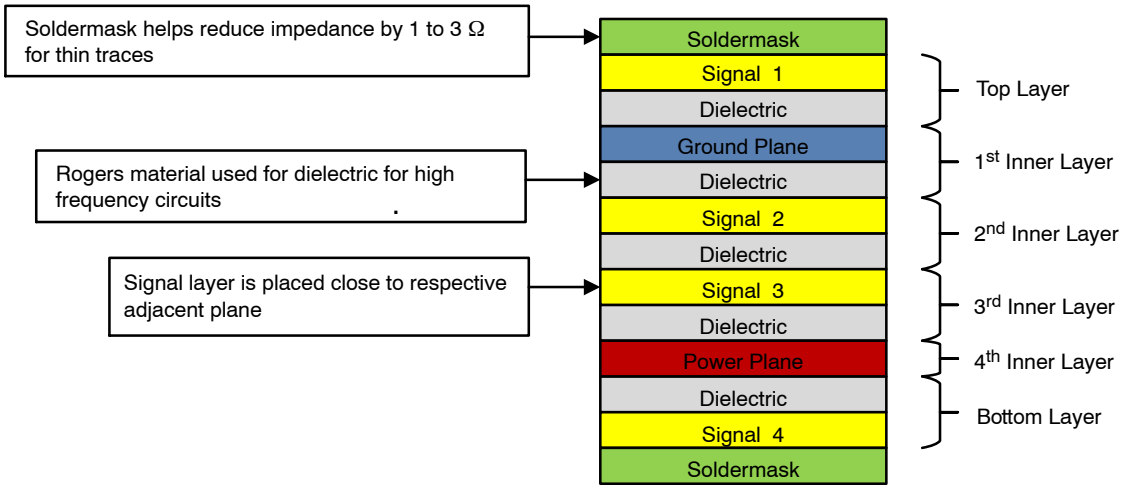

Figure 10. 6 Layer PCB Stack−up

Vias and Guidelines on Its Usage

Vias though useful to shift between PCB layers adds additional inductance and capacitance leading to change in impedance causing reflection. The less Vias are used in connection, the better. Vias can bring about a distribution capacitance of about 0.5 pF, reducing the number of Vias can significantly increase the speed and reduce the possibility of data error.

- Do not use Vias in clock transmission lines and in differential traces.
- Terminate clock signals to minimize reflection.
- Use wide, short traces between the Vias and capacitor pads. Use a bigger via size to connect the capacitor pad to the power and ground plane.
- Vias should be connected to the ground plane individually.
- If Vias are used to return your currents to their termination, then ensure that the Vias are tightly coupled, impedance matched differential Vias to ensure your signals arrive on time. The return Vias must be placed close to the signal Vias to minimize the length.
- Vias provide for an efficient path for current return preventing currents spreading around splits in the ground plane leading to loss of signal integrity. Vias ensure each of the signals will take a path of least impedance while going from source to sink.
- Ensure Blind and buried Vias do not result in any stubs. The Vias stubs should be kept to a minimum to reduce the discontinuities. Via stubs should be less than 15 mils. Figure 11 below shows examples of Vias connections.

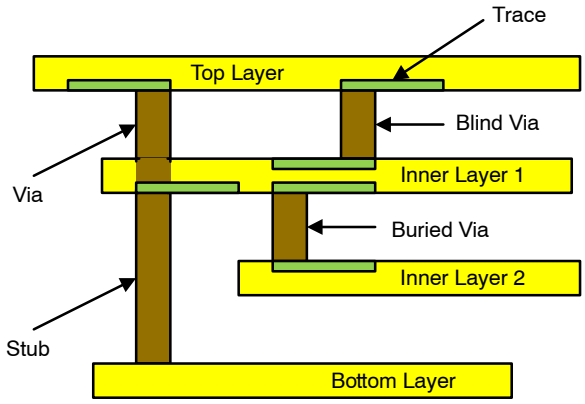

Figure 11. Types of Vias Connection

CONCLUSION

To optimize design & signal integrity and obtain higher electromagnetic compatibility in high−speed PCB design, it is required to have a reasonable layout and routing, avoidance of unnecessary turns and Vias, impedance continuity and matching, integrated signal reference planes and excellent grounding.

The above application note provides basics of PCB routing required for high speed signals.

We also recommend study of ON Application Note AN6103 for USB3.1.

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