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Use of NCP81172 for Extended Output Voltage Range

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APPLICATION NOTE

Introduction

The NCP81172 is a general−purpose two−phase synchronous buck controller, which has a typical application circuit as shown in Figure 1 if PWM−VID function is not employed. In Figure 1, the voltage V_{REFIN} at REFIN pin is the reference voltage for regulation of output voltage V_{OUT}, i.e. $V_{OUT} = V_{REFIN}$. V_{REFIN} is always lower than the voltage VREF having a typical value of 2 V. As a result of that, V_{OUT} cannot be higher than 2 V. To support applications with extended output voltage range, an application solution is illustrated in this application note.

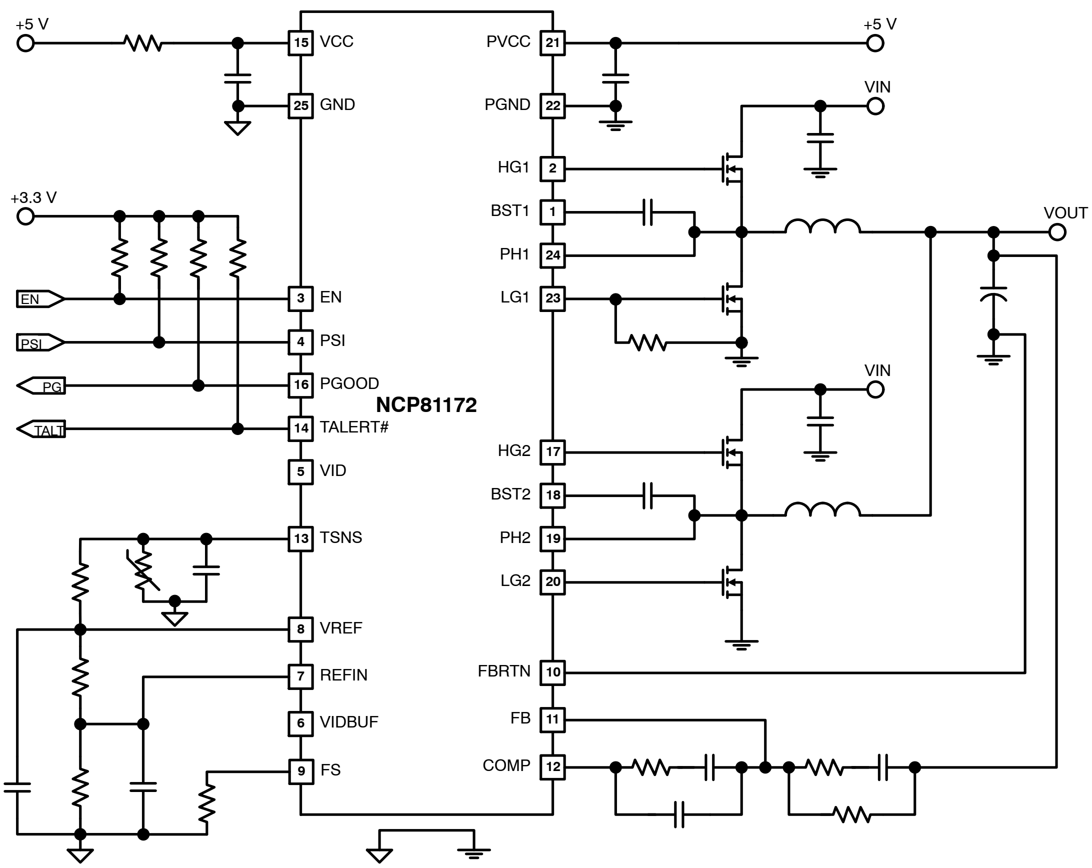

Figure 1. Typical Application Circuit for V_{OUT} < 2 V

Solution Description

Figure 2 shows a proposed solution for extended output voltage range. The major difference from the solution of Figure 1 is that an additional resistor R_{FB2} is applied between FB pin and FBRTN pin, which boosts output voltage to be higher than the voltage set at REFIN pin.

In steady−state operation, the voltage difference between REFIN and GND is equal to the voltage difference between FB and FBRTN. Hence, the output voltage V_{OUT} is given by

$$V_{OUT} = V_{REFIN} \cdot \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \qquad \text{(eq. 1)}$$

where the REFIN voltage V_{REFIN} is set by the resistor divider at REFIN pin:

$$V_{REFIN} = V_{VREF} \cdot \frac{R_{VREF2}}{R_{VREF1} + R_{VREF2}} \qquad \text{(eq. 2)}$$

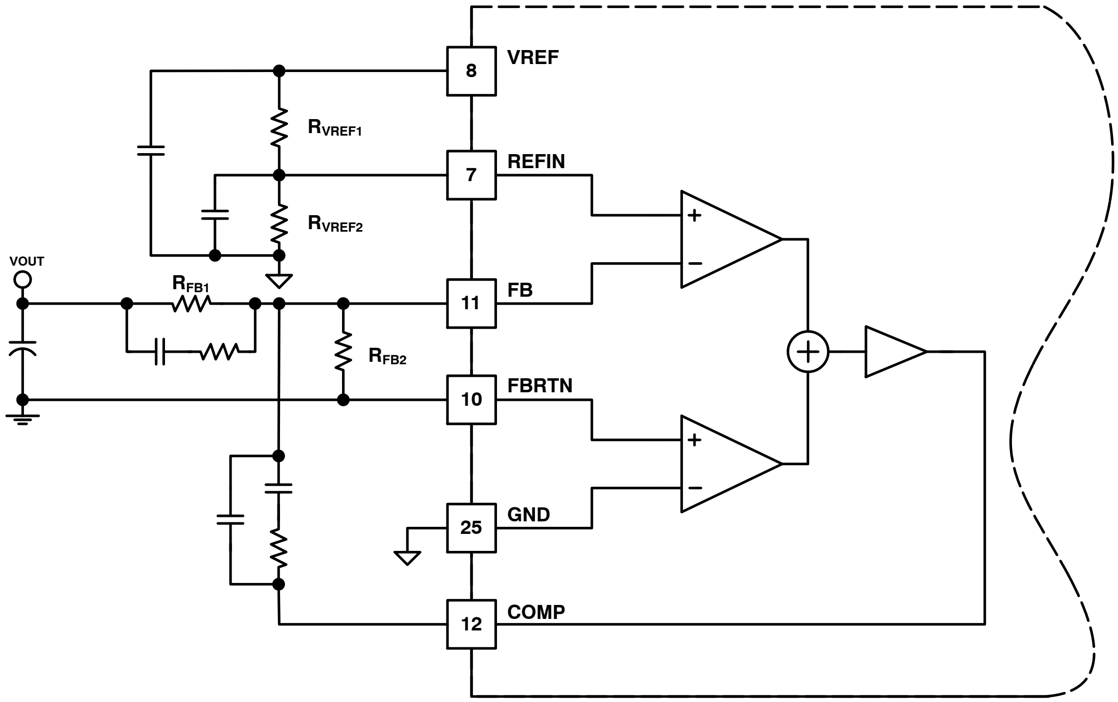

Figure 2. Application Circuit for Extended Output Voltage Range

One thing needs to mention, the NCP81172 is not designed for 2−phase applications in which conversion ratio V_{OUT}/V_{IN} is over 0.45. In another word, V_{IN} has to be higher than about 2.3 times of V_{OUT} in 2−phase mode to assure stable operation. However, the 1−phase operation does not have this limitation.

Design Guideline

1. REFIN Voltage Programming

The NCP81172 has an output over voltage protection function, which is based on voltage detection at FB pin. The over voltage threshold is equal to VREF having a typical value of 2 V. The maximum acceptable REFIN voltage can be defined by a predetermined over voltage threshold K_{OV}, e.g. 130%.

$$V_{REFIN} = \frac{V_{VREF}}{K_{OV}} \qquad \text{(eq. 3)}$$

Select resistance values for R_{VREF1} and R_{VREF2} to get the appropriate REFIN voltage, and make the total resistance value of the two resistors in a range from 5 kΩ to 50 kΩ.

2. Output Voltage Programming

After REFIN voltage is defined, the output voltage programming can be done by designing the feedback divider comprised of R_{FB1} and R_{FB2}. Usually R_{FB1} is arbitrarily selected in a range from 1 kΩ to 50 kΩ, and then R_{FB2} can be obtained by

$$R_{FB2} = R_{FB1} \cdot \frac{V_{REFIN}}{V_{OUT} - V_{REFIN}} \qquad \text{(eq. 4)}$$

3. Switching Frequency Programming

Switching frequency of the NCP81172 is programmed by a resistor R_{FS} applied from FS pin to ground. The typical switching frequency range is from 200 kHz to 800 kHz. Figure 3 shows a measurement based on a typical application under a condition of V_{IN} = 12 V, V_{OUT} = V_{REFIN} = 1.0 V, I_{OUT} = 20 A for PS0 mode operation (2−phase) and I_{OUT} = 10 A for PS1 mode operation (1−phase).

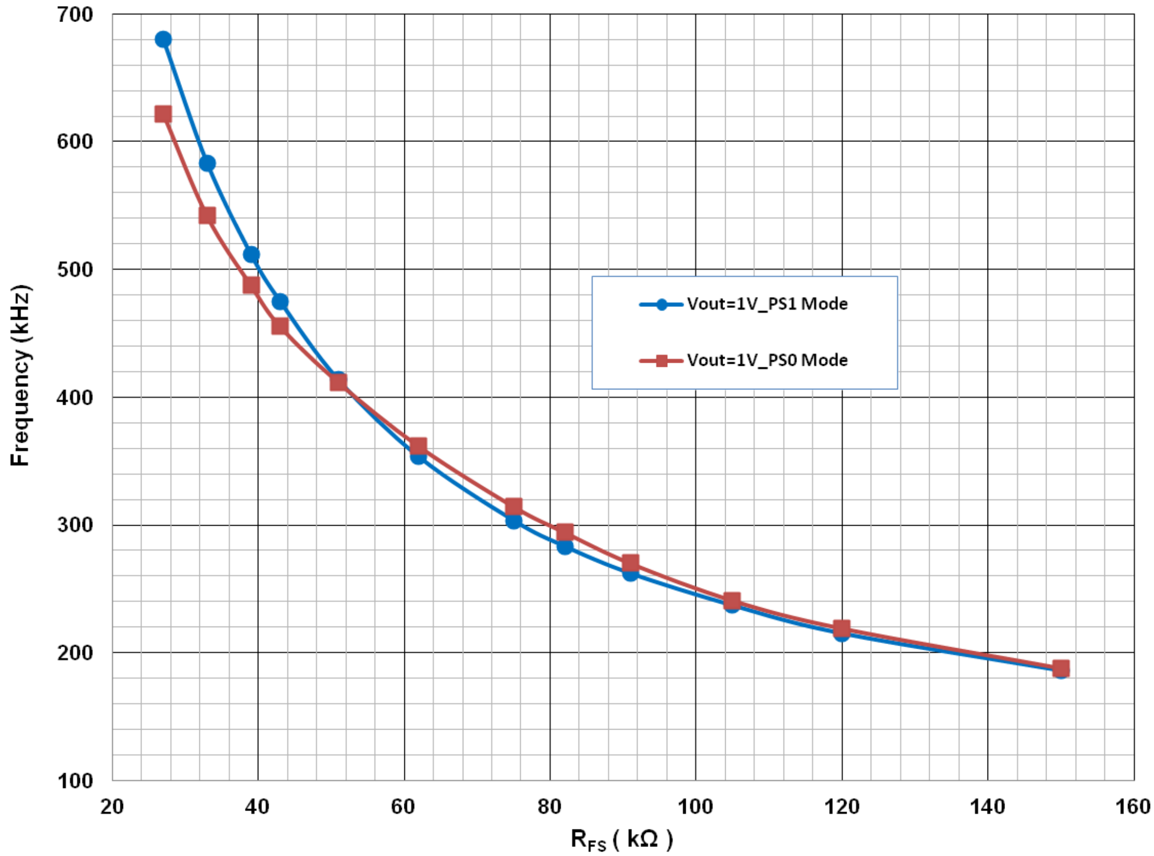

Figure 3. Switching Frequency Programmed by R_{FS} under Condition of V_{OUT} = V_{REFIN} = 1.0 V

The PWM control of the NCP81172, ramp pulse modulation (RPM), is one kind of ripple regulators. The three major determinant factors for the average PWM on time are input supply voltage V_{IN}, REFIN voltage V_{REFIN}, and frequency programming resistor R_{FS}. The NCP81172 has a built−in V_{IN} feedforward function in internal ramp signal in order to reduce frequency variation caused by variable supply voltage, and it is not a concern in this application note. In applications with V_{OUT} = V_{REFIN}, PWM on time is proportional to V_{OUT} such that frequency maintains quasi constant when V_{OUT} changes if R_{FS} is fixed. Due to this reason, Figure 3 can be used as a frequency programming reference for applications with V_{OUT} = V_{REFIN}.

However, situation changes in applications where V_{OUT} regulation level is higher than V_{REFIN} level, i.e. V_{OUT} > V_{REFIN}. The PWM on time does not change much over V_{OUT} level programming by means of adjusting R_{FB} at FB pin without any change in either R_{FS} or V_{REFIN}, therefore, the higher V_{OUT} level the higher switching frequency. Figure 4 shows an exemplary measurement under a condition of V_{REFIN} = 1.0 V, R_{FS} = 62 kΩ, and V_{OUT} changing from 1.0 V to 3.3 V by adjusting R_{FB}.

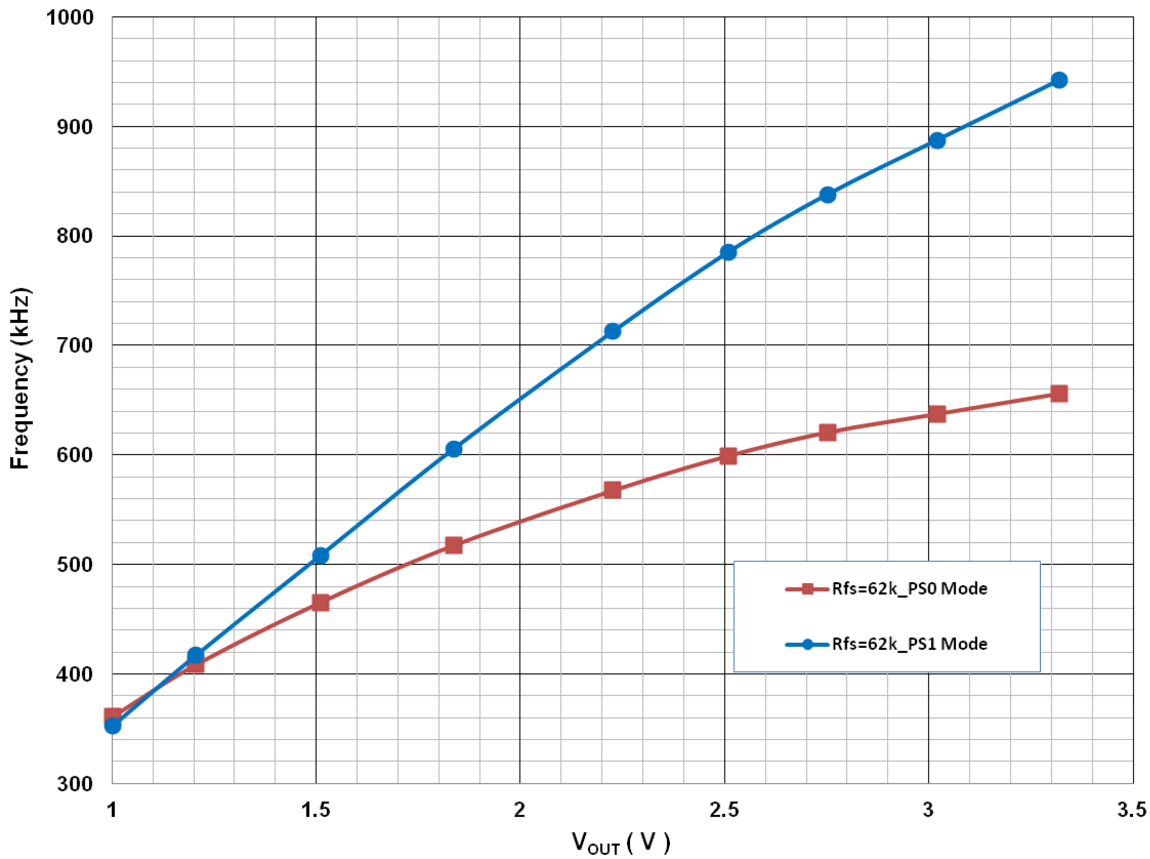

Figure 4. Switching Frequency Changes with V_{OUT} Programming under Condition of V_{REFIN} = 1.0 V and R_{FS} = 62 kΩ

To provide a guide for frequency programming in applications with $V_{OUT} > V_{REFIN}$, the switching frequency in PS0 mode operation (2−phase) can be estimated by

$$F_{SW(kHz)} = 6500 \cdot R_{FS(k\Omega)}{}^{-0.7} \cdot \left(\frac{V_{OUT}}{V_{REFIN}}\right)^{0.5} \quad \text{(eq. 5)}$$

and the switching frequency in PS1 mode operation (1−phase) can be estimated by

$$F_{SW(kHz)} = 8500 \cdot R_{FS(k\Omega)}{}^{-0.77} \cdot \left(\frac{V_{OUT}}{V_{REFIN}}\right)^{0.83} \quad \text{(eq. 6)}$$

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