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Forward Error Correction (FEC)

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APPLICATION NOTE

Overview

Forward Error Correction (FEC) is a method to make a transceiver more robust against noise. This is achieved by inserting redundant bits, i.e. bits that are computed from other bits and therefore do not contain independent information, which allow the receiver to correctly decode the bitstream even if some bits have been corrupted by noise.

The AX5042 supports FEC. If enabled, two new blocks are inserted into the transmit chain between encoder and modulator:

1. An encoder adds redundant bits to the bitstream
2. An interleaver reorders the bitstream

The inverse operations are inserted into the receive chain:

1. A deinterleaver and its associated synchronization circuitry re−reorders the bits into their natural order
2. A Viterbi decoder recovers the original transmit bits

Operation

The encoder and the decoder operate fully automatically and do not need any software intervention. The de−interleaver synchronization circuitry however needs some help from the microcontroller software.

While the encoder and the decoder operate independent from any framing format, the deinterleaver synchronization requires HDLC Flags. That is, in order to use FEC, the framing format must be HDLC, and the differential encoder, inverter, scrambler and Manchester must be off. Note that the scrambler is not necessary with FEC, since the convolutional encoder already removes DC content and shapes the output spectrum.

Whenever two or more sequential (back−to−back) HDLC flags enter the FEC encoder, it aligns the second and all following flags to the interleaver by inserting up to 7 zeros. The De−interleaver synchronization circuitry in the receiver then searches for this aligned and interleaved flag sequence.

It is therefore recommended to transmit two flags between packets, to allow a receiver that missed the first packet the chance to synchronize for the second packet.

The receiver automatically searches for the synchronization sequence. It needs to be prevented by the microcontroller from the following:

1. from changing the synchronization during reception
2. from falsely locking and keeping lock on the wrong phase

The receiver is prevented from changing the synchronization when both FECPOS and FECNEG in the FEC register are zero.

Restarting the synchronization after false lock is achieved by first clearing both FECPOS and FECNEG in the FEC register, and then re−enable either FECPOS or FECNEG or both.

The microcontroller firmware has to implement a heuristic that balances the following conflicting goals:

- Freeze synchronization as soon as a correct reception is likely going on, otherwise a correct packet might be corrupted by a false relock
- Restart synchronization as soon as possible if it is locked falsely, otherwise the receiver might miss a packet.

The following criteria may be used as part of this heuristic:

- If a sequence of say 10 back−to−back flags is received, that likely indicates that the receiver is correctly synchronized and receives the transmitter preamble, so synchronization should be frozen.
- Most frame formats employ a destination address at the beginning of the frame. If a HDLC frame start is received and the destination address does not match the local station, this either indicates an “uninteresting” packet or false lock, and therefore synchronization should be restarted.

The details of the heuristic are very much dependent on the actual frame format and the timing of the system, so they should be tuned accordingly.

FEC Specific Register Bank Description

This section describes the bits of the parts of the register bank related to FEC in detail. The registers are grouped by functional block to facilitate programming.

No checks are made whether the programmed combination of bits makes sense! Bit 0 is always the LSB.

NOTES: Whole registers or register bits marked as reserved should be kept at their default values.

All addresses not documented here must not be accessed, neither in reading nor in writing.

Table 1. CONTROL REGISTER MAP

Add	Name	Dir	Reset	Bit 7	6	5	4	3	2	1	0	Description
Forward Error Correction												
18	FEC	RW	00000000	SHORTMEM	RSTVITERBI	FECNEG	FECPOS	FECINPSHIFT(2:0)			FECENA	FEC (Viterbi) Configuration
19	FECSYNC	RW	01100010	FECSYNC(7:0)								Interleaver Synchronization Threshold
1A	FECSTATUS	RW	−−−−−−−−	FECINV	MAXMETRIC(6:0)							FEC Status

Register Descriptions

Table 2. FEC

The register controls the operation of the forward error correction (FEC) block.

Name	Bits	R/W	Reset	Description
FECENA	0	RW	0	Enable FEC (Encoder)
FECINPSHIFT	3:1	RW	000	Attenuate soft Rx Data by $2^{-FECINPSHIFT}$
FECPOS	4	RW	0	Enable noninverted Interleaver Synchronization
FECNEG	5	RW	0	Enable inverted Interleaver Synchronization
RSTVITERBI	6	RW	0	Reset Viterbi Decoder
SHORTMEM	7	RW	0	Shorten Backtrack Memory

FECENA enables the Forward Error Correction and the Interleaver.

For PSK, enable both FECPOS and FECNEG. For all other modulations, only FECPOS should be enabled.

In the TX, HDLC flags are aligned (by inserting zero bits) to the interleaver. In the RX, a convolver to the encoded / interleaved flag sequence establishes deinterleaver synchronization and inversion detection. Therefore, FEC only works together with HDLC framing.

The Viterbi decoder uses soft metric.

Table 3. FECSYNC

This register specifies the interleaver synchronization threshold.

Name	Bits	R/W	Reset	Description
FECSYNC	7:0	RW	01100010	Interleaver Synchronization Threshold

Table 4. FECSTATUS

This register reports the synchronization status.

Name	Bits	R/W	Reset	Description
MAXMETRIC	6:0	R	−−−−−−−−	Metric increment of the survivor path
FECINV	7	R	−	Inverted Synchronization Sequence received

References

[1] AX5042 Datasheet, see http://www.onsemi.com
[2] AX5042 Programming Manual, see http://www.onsemi.com
[3] AX5042 Evaluation Software, see http://www.onsemi.com
[4] Wikipedia. High−Level Data Link Control. http://en.wikipedia.org/wiki/HDLC

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