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Switching From a NCP1631- to a NCP1632-driven Interleaved PFC

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APPLICATION NOTE

Introduction

The NCP1632 is an up−graded version of the NCP1631.

Like “his father”, the NCP1632 is a dual MOSFET driver for interleaved PFC applications. Interleaving consists of paralleling two small stages in lieu of a bigger one, more difficult to design. This approach has several merits like the ease of implementation, the use of smaller components or a better distribution of the heating. Also, interleaving extends the power range of Critical conduction Mode (CrM) which is an efficient and cost−effective technique (no need for low t_{rr} diodes). In addition, the NCP1632 drivers are 180° phase shifted for a significant reduction of the current ripple.

It is worth noting that the NCP1632 has also inherited the NCP1631 capability to limit the switching frequency range. Like the NCP1631, the NCP1632 is designed to operate in critical conduction mode (CrM) in heavy load conditions and in discontinuous conduction mode (DCM) with frequency foldback in light load for an optimized efficiency over the whole power range. In no−load conditions, the two circuits further reduce operation losses by entering the skip mode.

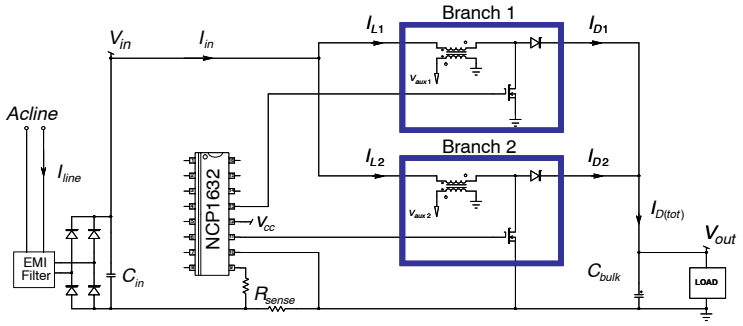


Figure 1. 2−Phase Interleaved PFC Stage

Note that the frequency clamped mode of operation not only optimizes the efficiency but also provides a significant reduction of the boost inductors’ size. The switching frequency of pure CrM solutions becomes high as the load decays. It is then necessary to use high inductances for containing the medium− and light−load frequency to levels compatible with targeted efficiency ratios. By contrast, the frequency clamped mode inherently prevents inefficient frequency levels. It allows to dimensioning the boost inductors for the only full load and as a result, to using smaller ones. As an example, the NCP1632 300 W evaluation board yields high−level performance with 150 μH boost inductors when a pure critical conduction mode solution would require about 250 μH to 350 μH ones.

In addition, the NCP1632 incorporates protection features for a rugged operation. More generally, the NCP1632 functions make it the ideal candidate in systems where cost−effectiveness, reliability, low stand−by power, high−level efficiency over the load range and near−unity power factor are the key parameters.

DIFFERENCES BETWEEN THE NCP1631 AND THE NCP1632

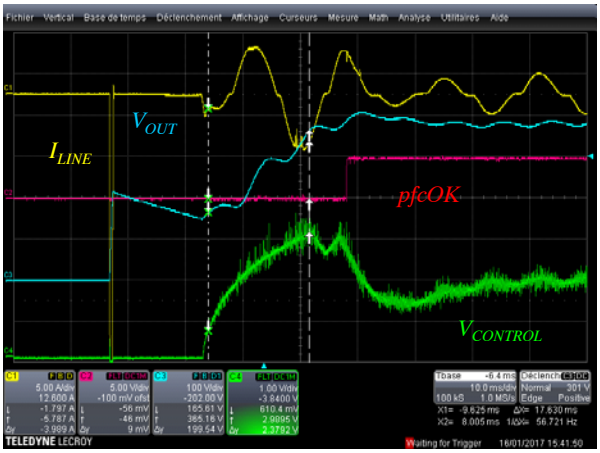
There are 4 differences in the operation of the two circuits:

- Up−graded startup phase
- Brown−out blanking time extended to 500 ms
- Latch threshold reduced to 166 mV
- Different control of the switching frequency

Improved Startup Phase

In the NCP1631, the dynamic response enhancer (DRE) which speeds−up the response if the output drops below 95.5% of its nominal value, is disabled until pfcOK is high. In other words, the DRE function is off until the output voltage has reached the target level. This ensures a slow rise of the control signal (compensation pin voltage) and hence, a gradual power increase and finally a soft start.

No Load



0.4 A Load

Figure 2. Start−up Phases @ 115 V rms

The NCP1632 enables part of the DRE during the start−up phase with two benefits:

- A shortened start−up phase. Figure 2 shows start−up phases obtained with the NCP1632 (tests made on a NCP1631 evaluation board modified to be NCP1632−driven according to Figure 10). The output voltage reaches its targeted level within 18 ms when the PFC stage is unloaded and within less than 30 ms at 50% load (tests made @ 115 V rms)
- A minimized start−up over−voltage as shown by Figure 2, when a type−2 compensation is used (provided by C_9, C_{10} and R_{19} of Figure 10).

Brown−Out Extended Blanking Time

The NCP1631 and the NCP1632 embed the same brown−out block which consists of monitoring the input voltage. Practically, a portion of the average input voltage is applied to the BO pin. This V_{BO} signal is used for feedforward and is compared to an internal reference for brown−out protection. The brown−out comparator has a programmable hysteresis.

A brown−out fault is detected if V_{BO} happens to drop below the BO threshold ($V_{BO(TH)}$ which is 1 V typically). A blanking time is however implemented which prevents the BO protection for tripping immediately. A BO fault is detected only if a new ($V_{BO} < V_{BO(TH)}$) event is detected during the 50 ms window time started after the blanking time has elapsed. More details can be found in the data sheet [1].

The blanking delay is implemented to help pass hold−up time requirements.

This blanking time was of 50 ms (typically) in the NCP1631. It has been lengthened to 500 ms in the NCP1632.

Reduced Latch Comparator Threshold

Pin 10 is the input of an internal latching−off comparator. If $V_{pin\,10}$ exceeds the V_{LATCH} threshold, the part latches−off until the circuit is reset (that is, when V_{CC} drops below $V_{CC(reset)}$, 5.75 V typically).

In the NCP1631, the V_{LATCH} threshold is set to a relatively high level (2.5 V typically) while it has a lower value in the NCP1632 (166 mV typically).

Frequency Control Mode

Whatever the power is, the NCP1631 is designed to clamp the switching frequency to a level set by the oscillator. When the load decays below a threshold set by the pin 6 external resistor, the NCP1631 enters the frequency foldback mode: the switching frequency remains clamped but to a lower level according to a characteristic controlled by the pin6 current. In both cases, as shown by Figure 4, the NCP1631 automatically transitions between CrM and DCM

depending on the current cycle duration being longer or shorter than the clamp frequency set by the oscillator.

The NCP1631 maintains a high PF performance in all modes CrM, DCM, CrM and DCM. However, the transitions between CrM and DCM can lead to small discontinuities of the line current. Similarly (but to a lesser extend), DCM transitions between valley n and valley (n+1) and vice versa can also cause slight bumps of the line current [1].

1. In all modes, the NCP1631 and the NCP1632 tend to turn on the MOSFETs when the drain−source voltage is minimal, that is, at the so−called valley. Hence, in DCM, the MOSFET will close at the valley next to the turn on clock. Since the inductor current cycle duration varies over the input voltage sinusoid, the dead−time and hence the turn−on valley rank will have to change accordingly.

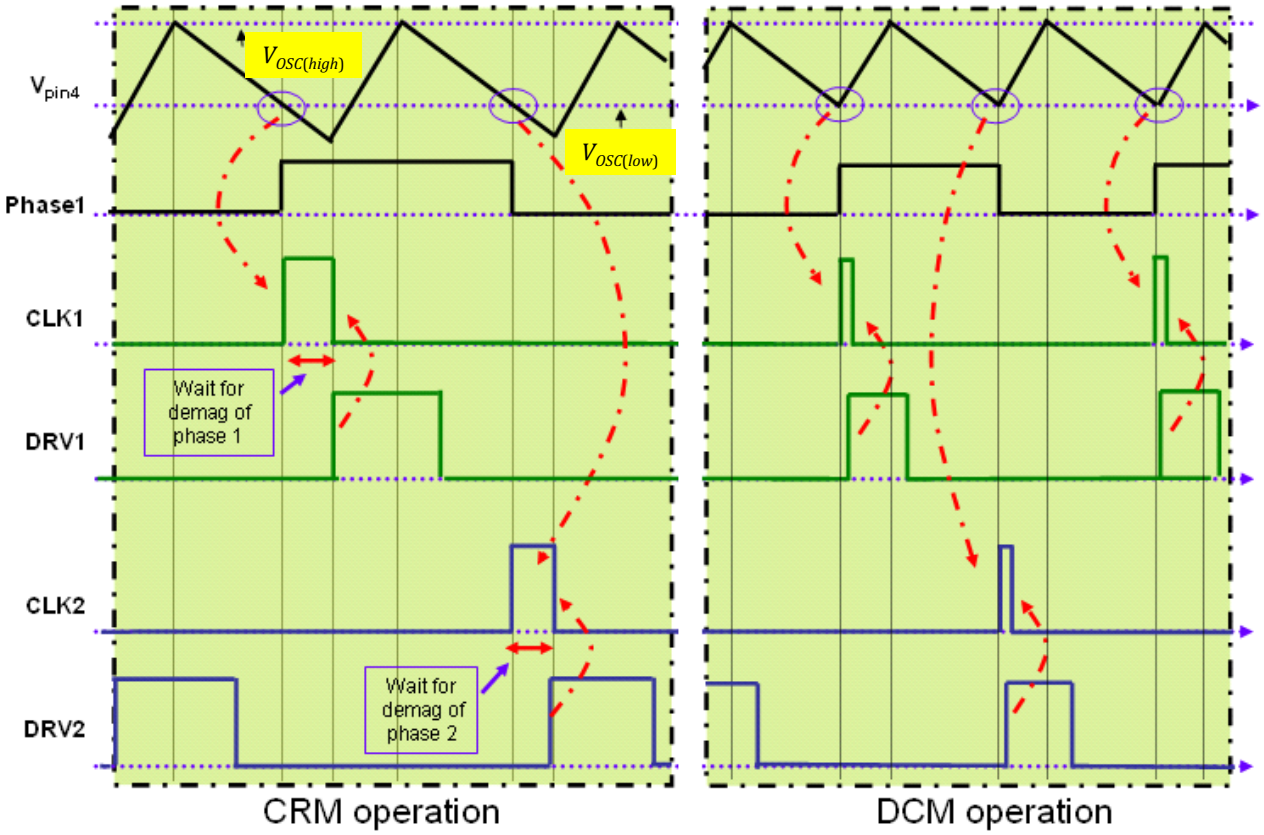


Figure 3. NCP1631 and NCP1632 Oscillator Operation (in HFC Mode for the NCP1632)

To avoid them, the NCP1632 is optimized to operate:

- In pure CrM without any frequency−clamp interaction when the line current magnitude is high
- In deep DCM when the line current magnitude is below a programmed level. Deep DCM means that the switching frequency is low enough to ensure a significant dead−time and to prevent transitions between CrM and DCM within the input voltage sinusoid.

The transition from one mode to the other is made based on the input average current. Practically, a programmable portion of the input average current is computed on the FFOLD pin (pin 6), so that:

- The NCP1632 operates in Frequency foldback (FFOLD) mode when V_{FFOLD} gets below 3 V. In this case, the oscillator lower threshold is lowered to increase the oscillator swing and thus, to reduce its frequency [2]. The oscillator lower threshold is further reduced if V_{FFOLD} decreases more.
- The NCP1632 operates High Frequency Clamp (HFC) mode when V_{FFOLD} exceeds 4 V. In this mode, the oscillator lower threshold is set to its maximum value (4 V typically). As a result, the clamp level of the switching frequency is at its maximum level and the PFC stage mostly runs in critical conduction mode which is more efficient than the discontinuous conduction mode in heavy load conditions.

The FFOLD pin voltage V_{FFOLD} is representative of the line current magnitude. Thus, the FFOLD mode will be set in medium− and light−load conditions while the HFC mode will be enabled in heavy load ones.

2. Instead of increasing the oscillator swing by lowering its lower threshold, the NCP1631 reduces the oscillator charge and discharge current to reduce the clamp frequency when in frequency foldback.

Optimally with a 2−slope oscillator (see next section), the HFC mode must lead the circuit to operate in pure CrM and the FFOLD mode, to operate in deep DCM [3].

3. Deep DCM means that the switching frequency is low enough to ensure a significant dead−time and prevent transitions between CrM and DCM within the input voltage sinusoid.

In other words, the NCP1632 is designed to operate in pure CrM at full load and deep DCM in medium− to light−load conditions. Efficiency can hence be optimized over the load range without repeated transitions between the CrM and DCM operation modes.

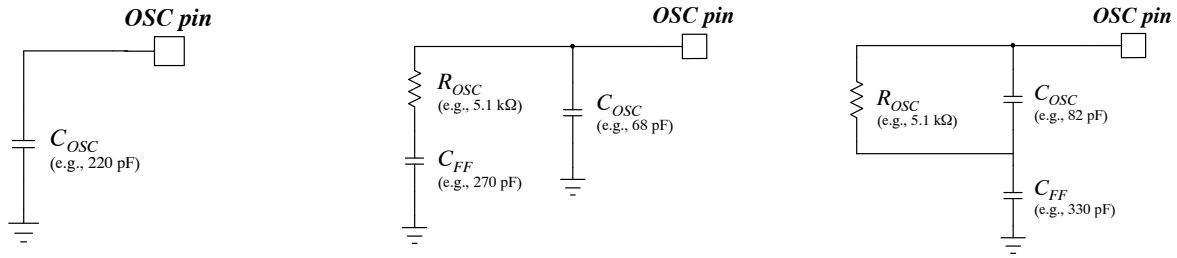
The next section details these aspects.

NCP1632 FREQUENCY CONTROL MODE

As aforementioned, the NCP1632 control of the switching frequency differs from the NCP1631 one. This section details its functioning.

A 2−Slope Oscillator

In Figure 5a) configuration, a single capacitor sets a frequency clamp. For instance, C_{OSC} = 220 pF forces 120 kHz to be the maximum frequency within each branch (the FFOLD mode reduces this level in light load conditions). Such a clamp value is likely to force DCM operation in part of the input voltage sinusoid (near the line zero crossing in particular where the inductor current cycle is short). To be able to force full CrM operation over a large working range, we would need to reduce C_{OSC} to a very low value. Still however, the oscillator must keep able to keep synchronized to the current cycle for proper out−of−phase control. This requires the oscillator swing to not to exceed its 1 V to 5 V range even in heavy load conditions when the switching frequency in each individual branch generally drops below 100 kHz. This is generally not possible with a single small capacitor on the OSC pin.



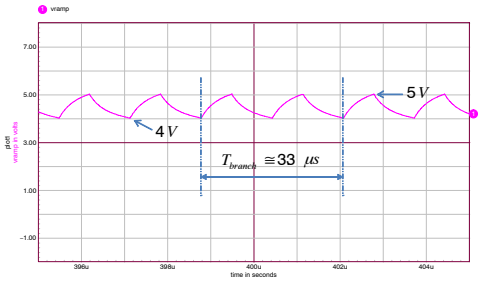
a.) Basic configuration a.) Option 1 a.) Option 2

Figure 4. External Components Driving the OSC Pin

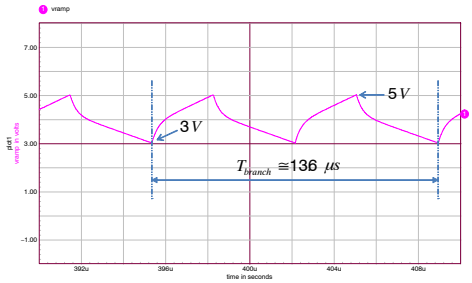
Instead, the schematic of either Figure 5b) or Figure 5c) is to be used where:

- C_{OSC} (which value is much less than the second capacitance C_{FF}) sets the high−frequency operation necessary for operating in CrM
- R_{OSC} limits the influence of the C_{FF} capacitor as long as the oscillator swing remains below (R_{OSC}.I_{OSC}) where I_{OSC} is the charge or discharge current depending on the sequence. The voltage across C_{OSC} being limited by R_{OSC} (to about 1 V with 5.1 kΩ), the second much−higher−value capacitor (C_{FF}) is engaged when heavy−load CrM operation imposes a larger oscillator swing.
- C_{FF} is also the major contributor in adjusting the frequency in light load (when the frequency foldback mode forces deep DCM operation). As previously mentioned, C_{FF} also ensures that the oscillator voltage can stay above 1 V in deep CrM conditions.

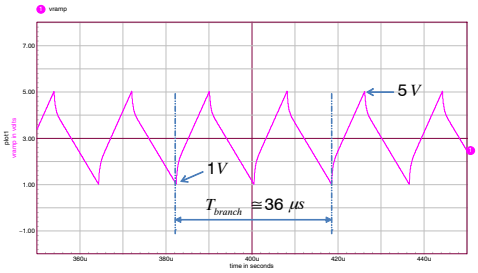
Finally, Figure 5b) and c) configurations provide some kind of variable−capacitance oscillator. For instance, Option b) provides the following typical characteristics:



300 kHz frequency clamp in HFC mode (V_{FFOLD} > 4 V)



73 kHz frequency clamp when entering FFOLD mode (V_{FFOLD} = 3 V)



28 kHz minimum frequency clamp (deepest DCM @ V_{FFOLD} = 1 V)

Figure 5. Clamp Frequency in Each Individual Branch with the Configuration of Figure 4 b)

Managing the HFC to FFOLD Transition

The NCP1632 FFOLD pin sources a current proportional to the input current (I_{CS}). This current is changed into a dc voltage by means of an external (R//C) network applied to the FFOLD pin. The obtained V_{FFOLD} voltage is hence proportional to the line average current. As illustrated by Figure 6, the PFC stage enters the frequency foldback mode (FFOLD mode) when V_{FFOLD} goes below 3.0 V, and recovers high−frequency clamp mode (HFC mode) when the FFOLD voltage exceeds 4 V.

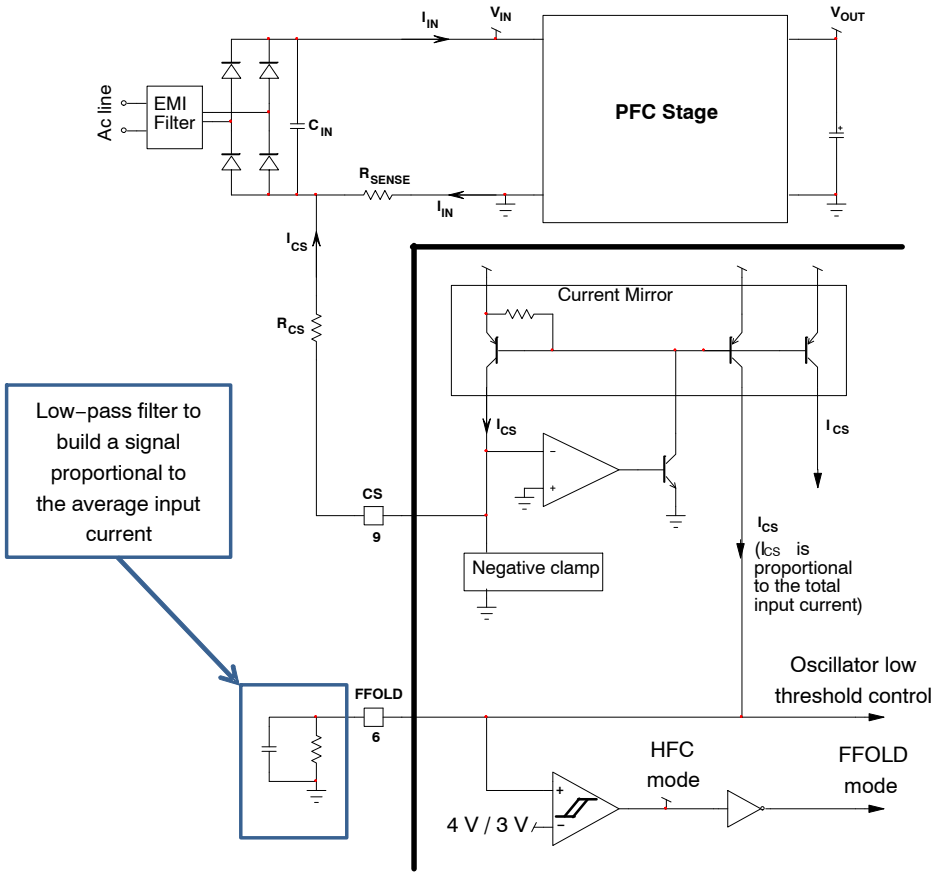


Figure 6. Frequency Foldback Control

In HFC mode, the oscillator lower threshold (V_{OSCL}) is fixed and equal to $V_{OSC(low)}$ (4 V typically).

In FFOLD mode, V_{OSCL} is modulated by the FFOLD pin voltage as follows:

- $V_{OSCL} = V_{FFOLD}$ if V_{FFOLD} is between 1 and 3 V
- V_{OSCL} = 1 V if V_{FFOLD} is below 1 V
- V_{OSCL} = 3 V if V_{FFOLD} exceeds 3 V

Figure 7 illustrates a “natural” transition FFOLD to HFC mode.

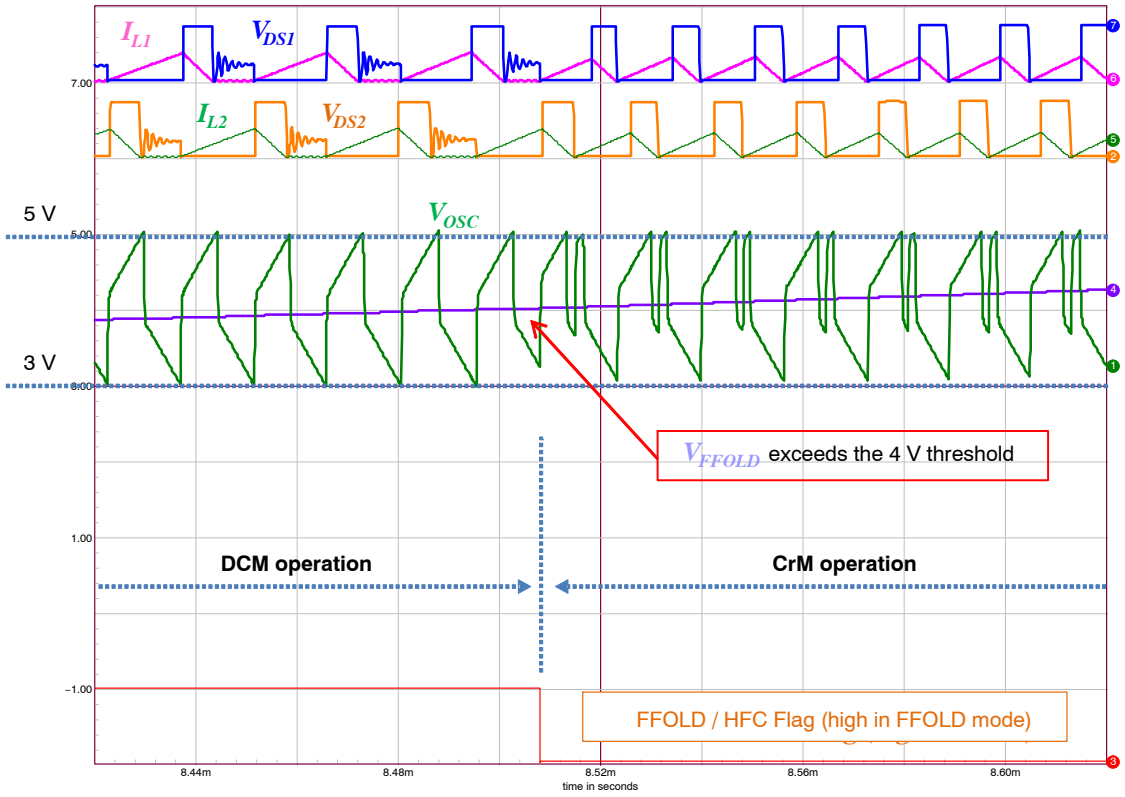


Figure 7. "Natural" Transition FFOLD to HFC Mode when V_{FFOLD} exceeds 4 V

Speeded−up HFC Recovery in case of an Abrupt Load Increase

Note that the FFOLD pin is heavily filtered, which causes long V_{FFOLD} settling phases. If while in very light−load conditions, the load abruptly rises, the FFOLD pin time constant may dramatically delay the HFC−mode recovery. During this delay, the PFC stage may not be able to provide the full power because of the DCM operation caused by the FFOLD mode. To solve this, the NCP1632 forces HFC operation whenever the DRE comparator trips [4] and remains in HFC mode until the output voltage recovers its regulation level. At that moment, the conduction mode is normally selected as a function of the FFOLD pin voltage.

4. The dynamic response enhancer (DRE) comparator trips when the output voltage drops below 95.5% of its regulation level.

PRACTICAL EXAMPLE

Figure 8 provides the practical schematic of the 300 W evaluation board of the NCP1631 detailed at http://www.onsemi.com/PowerSolutions/supportDoc.do?type=boards&rpn=NCP1631. Figure 9 shows the modifications necessary to have it controlled by the NCP1632.

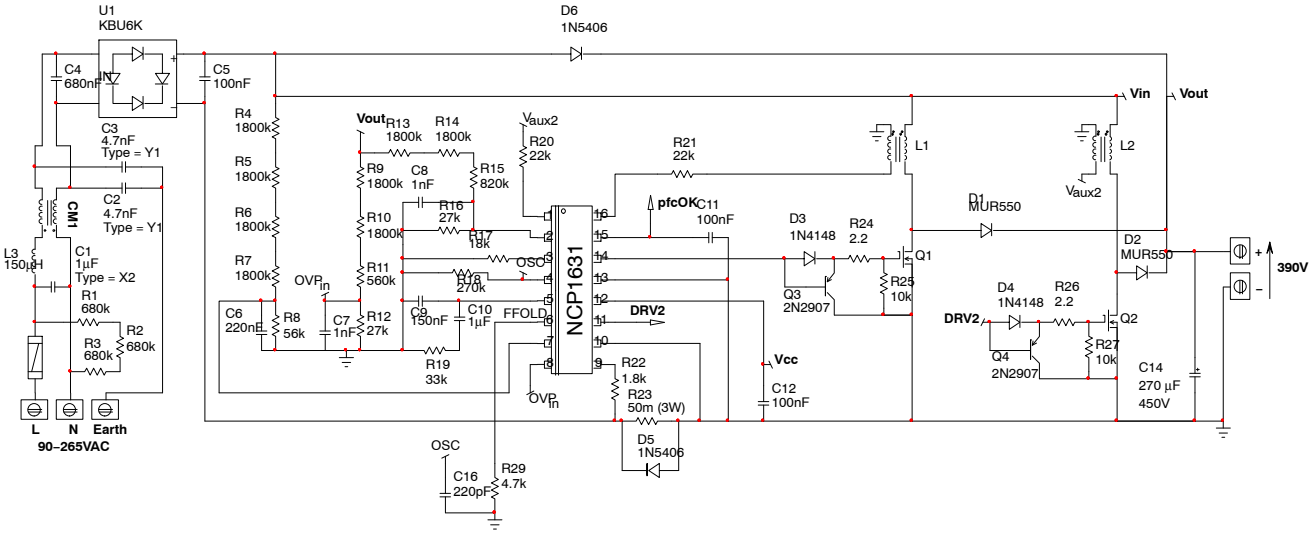


Figure 8. Application Schematic of a 300 W Interleaved PFC Stage Driven by the NCP1631

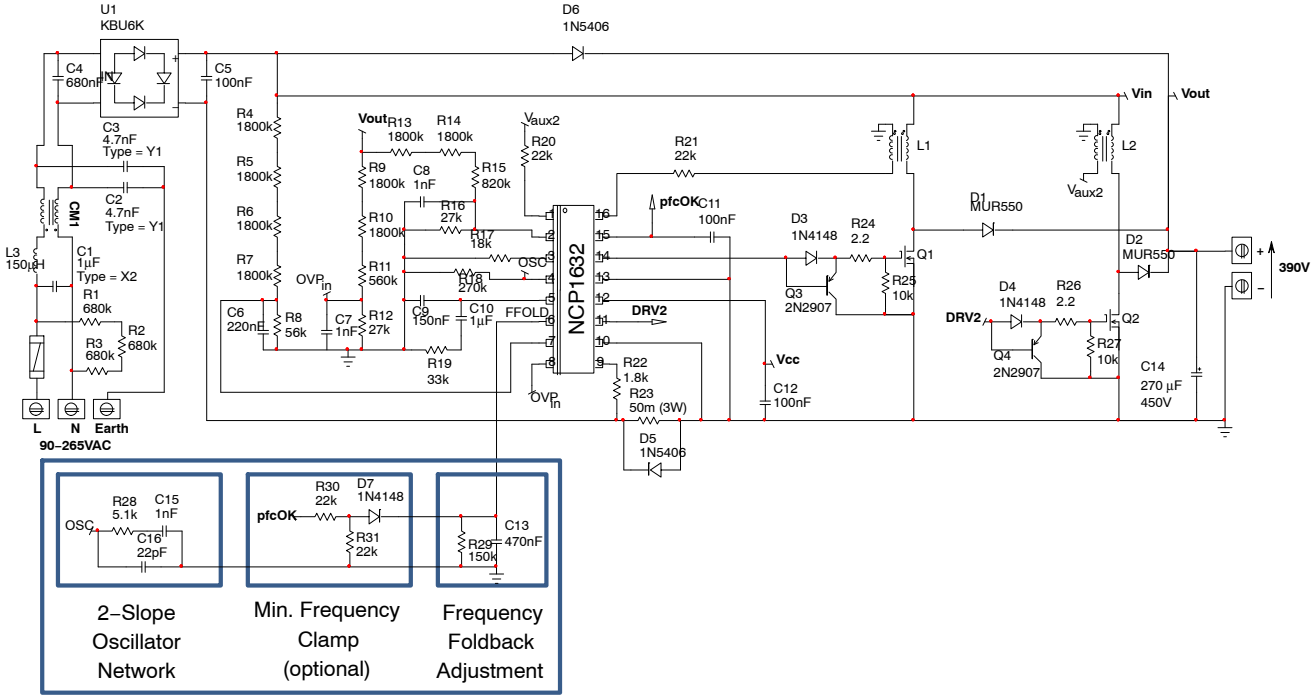


Figure 9. Application Schematic of the Figure 8 − Application Schematic of a 300 W Interleaved PFC Stage Driven by the NCP1631 Board, Tweaked to be NCP1632−driven

A first modification is the presence of a 2−slope oscillator. It consists of two capacitors (C_{15} and C_{16}) and of a resistor (R_{28}). This OSC network sets a high−frequency clamp when the input current magnitude (measured on the FFOLD pin) is large enough to disable the frequency foldback mode. This ensures pure CrM operation in heavy load condition.

When the FFOLD pin voltage drops below 3 V, the circuit enters the frequency foldback mode. In this case, the oscillator threshold is set by the FFOLD pin level while the OSC upper threshold remains fixed to $V_{OSC(high)}$ (5 V typically). When the input current decreases, V_{FFOLD} decays and the oscillator swing ($V_{OSC(high)}$−V_{FFOLD})

increases. The swing is maximum and equal to $V_{OSC(swing),max}$ (4 V typically) when (V_{FFOLD}=1V). In this case, the oscillator period is maximum and approximately equal to:

$$T_{OSC,\max} = \frac{(C_{15}+C_{16})\cdot\left(V_{OSC(swing),\max}-\left(R_{28}\cdot(I_{CH}+I_{DISCH})\right)\right)}{I_{CH}} + \frac{(C_{15}+C_{16})\cdot\left(V_{OSC(swing),\max}-\left(R_{28}\cdot(I_{CH}+I_{DISCH})\right)\right)}{I_{DISCH}} \quad \text{(eq. 1)}$$

Which simplifies as follows:

$$T_{OSC,\max} = \frac{I_{CH}+I_{DISCH}}{I_{CH}\cdot I_{DISCH}}\cdot(C_{15}+C_{16})\cdot\left(V_{OSC(swing),\max}-R_{28}\left(I_{CH}+I_{DISCH}\right)\right) \quad \text{(eq. 2)}$$

The minimum oscillator frequency is hence:

$$f_{OSC,\min} = \frac{\frac{I_{CH}\cdot I_{DISCH}}{I_{CH}+I_{DISCH}}}{C_{15}+C_{16}}\cdot\frac{1}{V_{OSC(swing),\max}-R_{28}\left(I_{CH}+I_{DISCH}\right)} \quad \text{(eq. 3)}$$

The branch frequency is half the oscillator one. Hence:

$$f_{branch,\min} = \frac{\frac{I_{CH}\cdot I_{DISCH}}{I_{CH}+I_{DISCH}}}{2\cdot(C_{15}+C_{16})}\cdot\frac{1}{V_{OSC(swing),\max}-R_{28}\left(I_{CH}+I_{DISCH}\right)} \quad \text{(eq. 4)}$$

In our case, it comes:

$$f_{branch,\min} = \frac{60\cdot10^{-6}}{2\cdot\left(22\cdot10^{-12}+1000\cdot10^{-12}\right)}\cdot\frac{1}{4-\left(5.1\cdot10^{3}\cdot(140+105)\cdot10^{-6}\right)} \cong 11\,kHz \quad \text{(eq. 5)}$$

Such a frequency is in the audible range. To increase it, R_{30}, R_{31} and D_7 of Figure 10 prevent the FFOLD pin from dropping below about 2 V (V_{pfcOK} is 5 V when in frequency foldback mode), thus, limiting oscillator swing to about ($V_{OSC(high)}$−2V), that is, nearly 3 V. The branch minimum frequency becomes:

$$f_{branch,\min} = \frac{60\cdot10^{-6}}{2\cdot\left(22\cdot10^{-12}+1000\cdot10^{-12}\right)}\cdot\frac{1}{3-\left(5.1\cdot10^{3}\cdot(140+105)\cdot10^{-6}\right)} \cong 17\,kHz \quad \text{(eq. 6)}$$

FFOLD to HFC line magnitude threshold:

The FFOLD pin sources a current proportional to the input current:

$$I_{FFOLD} = I_{CS} = i_{in}(t)\cdot\frac{R_{23}}{R_{22}} \quad \text{(eq. 7)}$$

Where:

- R_{23} is the current sense resistor
- R_{22} is the resistor placed between the CS pin and R_{23}.

Hence, the FFOLD average voltage is:

$$V_{FFOLD} = \frac{R_{29}\cdot R_{23}}{R_{22}}\cdot\left\langle i_{in}(t)\right\rangle_{T_{line}} = \frac{2\sqrt{2}}{\pi}\cdot\frac{R_{29}\cdot R_{23}}{R_{22}}\cdot I_{in,rms} \quad \text{(eq. 8)}$$

Where R_{29} is the resistor applied to the FFOLD pin.

Due to the FFOLD low−frequency ripple (at twice the line frequency), we can consider that the mode transition will occur when V_{FFOLD} is between the 3−V and 4−V threshold, that is, $(V_{FFOLD})_{th}$=3.5 V:

$$\left(I_{in,\mathrm{rms}}\right)_{th} = \left(I_{line,\mathrm{rms}}\right)_{th} \cong \frac{\pi}{2\sqrt{2}}\cdot\frac{(V_{FFOLD})_{th}\cdot R_{22}}{R_{29}\cdot R_{23}} \cong 3.9\cdot\frac{R_{22}}{R_{29}\cdot R_{23}} \quad \text{(eq. 9)}$$

With selected resistor (150 kΩ on the FFOLD pin, in particular), the line rms current threshold is 0.94 A. This will lead the system to transition at about 110 W at 115 V rms and 220 W at 230 V rms.

The hysteresis is modulated by the capacitor which filters the FFOLD pin (C_{13} of Figure 10). A good trade−off generally consists of selecting C_{13} so that the FFOLD pin is in the range of 4 times the line frequency:

$$C_{13} \cong \frac{4}{R_{29}\cdot f_{line}} \cong \frac{4}{150\cdot10^{3}\cdot60} = 444\,nF \quad \text{(eq. 10)}$$

We have selected 470 nF.

CONCLUSIONS

The NCP1632 is a direct successor of NCP1631 from which it has inherited most of the features including the accurate and robust interleaving technique or the protections for a rugged operation.

Like the NCP1631, it also controls the switching frequency variations and thus, both optimizes the efficiency over the line/load range and provides a significant reduction of the boost inductors' size.

However, the NCP1632 switching frequency method differs from the NCP1631 one. The NCP1631 permanently clamps the switching frequency, which can cause repeated critical to discontinuous conduction mode transitions and due to them, can lead to small line current bumps. The NCP1632 eliminates the current bumps by:

- Forcing critical conduction mode operation in heavy−load conditions and prevent DCM operation in this case
- Forcing deep discontinuous conduction operation in light− and medium−load conditions.

The NCP1632 also improves the startup sequence, features a longer brown−out blanking time and a lower threshold latching−off comparator.

REFERENCES

[1] NCP1632 data sheet, http://www.onsemi.com/pub/Collateral/NCP1632−D.PDF

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