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FAN3852 PCB Layout Guidelines & Application Notes

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APPLICATION NOTE

OVERVIEW

The ON Semiconductor FAN3852 microphone pre−amplifier with digital output is a high performance, low−power analog−to−digital converter with a serial pulse density modulation (PDM) output.

This application note is intended to provide the system−level information needed to successfully implement this device in your microphone or analog sensor design.

Getting the most of the FAN3852's features in your applications requires attention to PCB layout and design guidelines to achieve optimum performance and reliability. Accordingly, this application note will address the following key topics:

- Application usage guidelines
- Signal path gain mapping
- Board design guidelines
- Grounding layout & considerations
- Decoupling capacitor size and placement
- Input signal coupling
- Design for EMI considerations

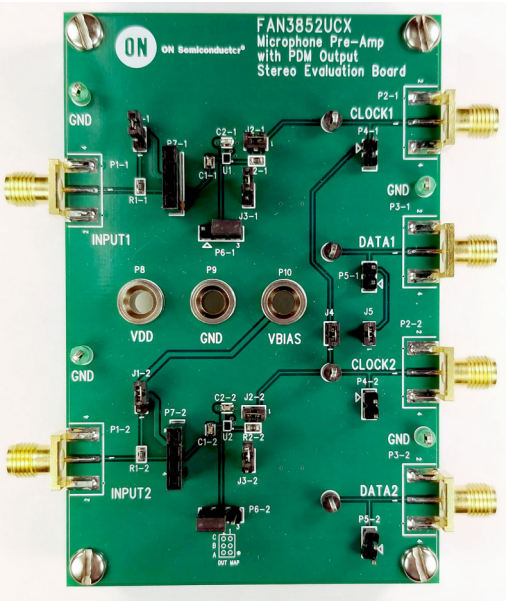


Figure 1. Evaluation Board

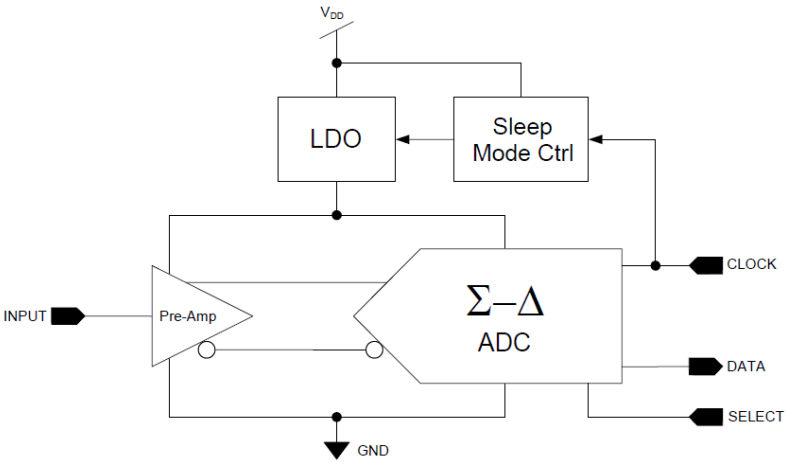


Figure 2. FAN3852 Simplified Block Diagram

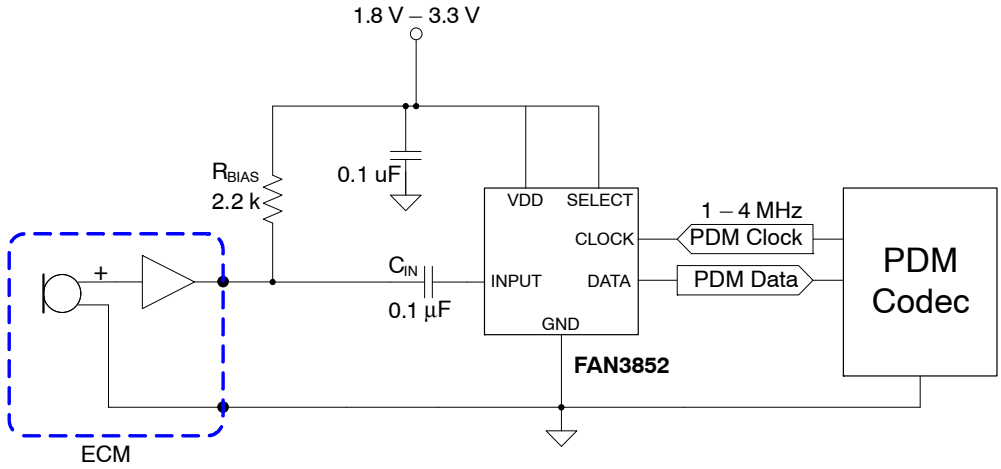


Figure 3. FAN3852 Simplified Applications Example (Mono)

APPLICATIONS GUIDELINES

The FAN3852 incorporates design features that improve the performance and power−efficiency of the device in application. This section explains these features and provides guidelines for proper implementation.

Low−Power Sleep−Mode

On removal of the PDM clock input, the FAN3852 automatically enters a power−saving sleep mode which reduces IDD current from 420 uA (typ) to 1.5 uA (typ). The FAN3852 automatically recovers to active mode once the PDM clock is again detected. This is an especially useful feature for mobile or other low−power applications.

When designing an application to use the sleep−mode feature, use the datasheet sleep and enable timing specs, t_{WAKEUP} & $t_{FALLASLEEP}$, to ensure PDM data integrity. Also note that the FAN3852 typically will sleep when f_{CLOCK} falls below ~70 kHz and wake when f_{CLOCK} is greater than ~300 kHz.

Clock−edge SELECT pin

The FAN3852 SELECT pin allows the user to select the PDM clock edge for transmission of the PDM output data on the DATA pin. Table 1 below shows the data−to−clock edge alignment for each SELECT pin state.

Table 1. SELECT Pin Function

SELECT State	PDM Clock Edge
Low	Falling
High	Rising

This function allows the multiplexing of two devices on a single PDM bus. In this configuration, one device would be set to have its SELECT pin tied to VDD; the second device would have SELECT tied to GND. Each device would then output its PDM data on opposite clock edges, allowing the DDR PDM codec input to receive digital data from both FAN3852 devices on a single shared data line. This configuration for a stereo ECM application is illustrated in the applications information section of the FAN3852 datasheet.

Automatic Input Signal Bias Control

The FAN3852 input incorporates an automatic DC bias tracking function that compensates for changes in the input signal offset over time. This allows the device to optimize the usable input signal amplitude range, regardless of the AC signal frequency content.

In addition to these features, two key application considerations are discussed below:

Input AC−Coupling Capacitor Selection

The input signal coupling scheme of the FAN3852 is different than typical signal−biasing schemes used for ECM audio or other analog signals. In those schemes, a resistor divider and AC coupling capacitor at the amplifier input are used to create the DC bias for the input signal and set the high−pass filter cutoff frequency.

While the FAN3852 also requires an input AC−coupling capacitor (C_{IN}), the auto−bias control feature requires that there are no ground−referenced components between the C_{IN} capacitor and ground. Instead, the high−pass signal corner of the FAN3852 input is set by C_{IN} and the 10 GΩ device input impedance. Calculation of cutoff frequency is, therefore:

$$F_c = \frac{1}{2\pi(R_{IN} \times C_{IN})} \quad \text{(eq. 1)}$$

Similarly, calculating the input capacitance for a desired cutoff frequency is:

$$C_{IN} = \frac{1}{2\pi(f_c \times R_{IN})} \quad \text{(eq. 2)}$$

Due to the input coupling and auto−bias control of the FAN3852 input, DC measurements are not recommended.

System Gain Calculation

Whether you use the FAN3852 as an ADC pre−amplifier for traditional analog microphone signals or for amplification and digitization of other low−level analog end−point signals in your system, calculation of the path gain is an important part of the design.

The FAN3852 datasheet performance specifications such as input sensitivity (IN_{NOM}), signal−to−noise ratio (SNR) & acoustic overload point (V_{OUT}) are intended for use with an electret condenser microphone (ECM) where the input signal is acoustic and measured in dB sound−pressure−level (SPL). For this type of application, the system signal mapping can be shown in Figure 4.

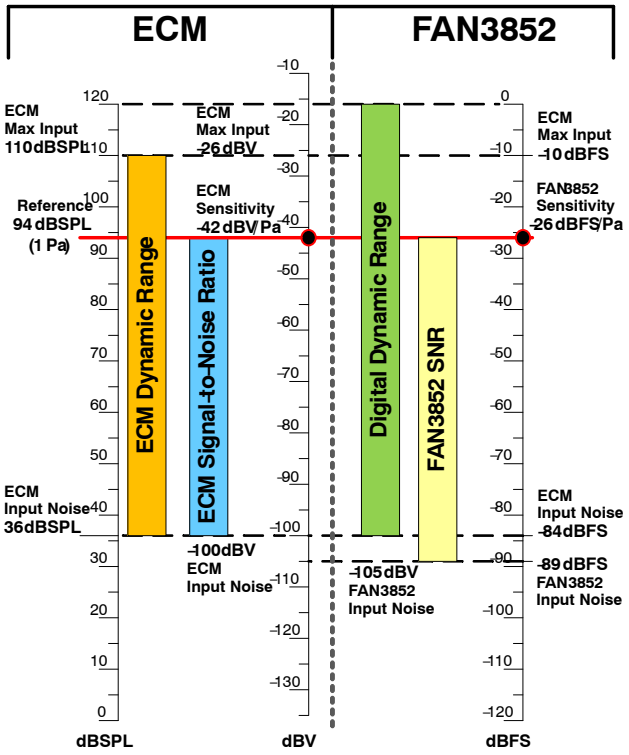


Figure 4. ECM−to−FAN3852 Signal Mapping

Figure 4 maps the input noise, dynamic range and signal−to−noise ratio of an example microphone from the acoustic (dBSPL) ECM input to the digital (dBFS) FAN3852 output. The key to this mapping is the sensitivity specifications of both the ECM and the FAN3852, which align the scales for conversion:

The ECM sensitivity specification of −42 dBV/Pa, measured at the reference level of 94 dBSPL, or 1 Pa, is the alignment point for mapping acoustic dBSPL sound level to RMS analog voltage for this particular ECM.

Similarly, the FAN3852 sensitivity of −26 dBFS/Pa allows the alignment of the dBFS scale to same reference point as the ECM.

Once the three scales are aligned by sensitivity, ECM datasheet specs such as the maximum input level and input noise can be mapped directly to dBV and dBFS. Others, such as dynamic range and SNR can be calculated per the equations below:

ECM e_N (dBSPL) = Reference − ECMSNR
ECM e_N (dBV) = ECM Sensitivity − ECM SNR
ECM Dynamic Range = ECM Max Input − ECM e_N

FAN3852 SNR (dB) = FAN3852 Sensitivity − FAN3852 e_N

Non−ECM Gain Mapping

When using the FAN3852 in a non−microphone application, use the device's nominal fixed internal analog−to−digital gain mapping of 16 dBFS/dBV to convert input signal amplitude to PDM output level.

This gain is derived from the datasheet spec for maximum input level (V_{IN}) of 448 mVpp which, when converted to decibels, equals −16 dBV. Therefore, the max full−scale PDM output of 0 dBFS equals −16 dBV.

BOARD DESIGN GUIDELINES

The FAN3852 is a versatile small−signal amplifier that can be incorporated into designs of various form−factors and layouts. The small footprint and minimal number of external components make it ideal for use in applications where PCB space and overall form−factor are as important as maintaining performance, such as in mobile devices, power−sensitive IoT devices and stand−alone sensor units. For best results, refer to the following guidelines and considerations when implementing the FAN3852 in your PCB design.

Grounding Layout & Consideration

FAN3852 grounding layout is important for proper operation and performance.

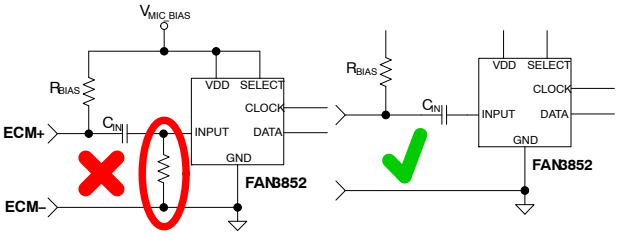
Connect the FAN3852 ground pin to a common ground bus or plane that includes the ECM or sensor ground and the PDM codec ground.

Decoupling Capacitors

A 0.1 μF low−ESR decoupling capacitor is recommended for VDD. This capacitor should be placed close to the FAN3852 and connected to GND through a low−impedance path. Refer to Figure 5.

Analog Input Signal Layout

Important: The FAN3852 analog input signal must be AC−coupled to the INPUT pin for proper operation. The FAN3852 generates a self−adjusting bias voltage at the INPUT pin to maintain optimum signal offset. Do not place any ground−referenced components between the input coupling capacitor and the INPUT pin; even high−impedance (MΩ) components can prevent the FAN3852 from maintaining the proper input offset voltage.



Refer also to Figure 5 for an example of top−layer trace routing and layout for power, output and signal traces.

PDM Digital Signal Layout

The FAN3852 PDM output is a 0V−to−V_{DD} digital signal running at 1−4 MHz, with rise & fall times of 10 ns or less. For stable device performance, guidelines for trace routing and impedance control for high−speed signals should be observed:

- Control DATA output trace impedance to within 20% of nominal (minimize discontinuities).
- Consider using a 100 Ω series termination resistor at the input to the PDM receiver if PCB design restrictions cause signal integrity issues.

EMI Considerations

Designing for effective EMI (Electro−Magnetic Interference) mitigation is a necessity for electronic devices. The FAN3852 requires consideration of both the input and output signals.

Due to the extremely high input impedance of the FAN3852 and the small analog signal amplitudes, care must be taken to prevent unwanted signals from coupling or radiating on to the input from other sources. This includes keeping analog signal traces short (<1”) and placing the device away from noisy sources or under a shielded housing.

Additionally, care must be taken to ensure the PDM output signal does not contribute to EMI.

The most effective methods for EMI management are incorporated in the board design and layout, as noted above in the PDM Digital Signal Layout guidelines.

Controlling Board Contaminants

Due to the extremely high input impedance of the INPUT pin (>10 GΩ), the performance of the FAN3852 can be compromised by the presence of residual contaminants from the assembly process.

A controlled process for removal of residual flux from between the device’s solder bumps, rinsing with de−ionized water, and baking the completed PCB to remove moisture is recommended to eliminate assembly−related performance issues.

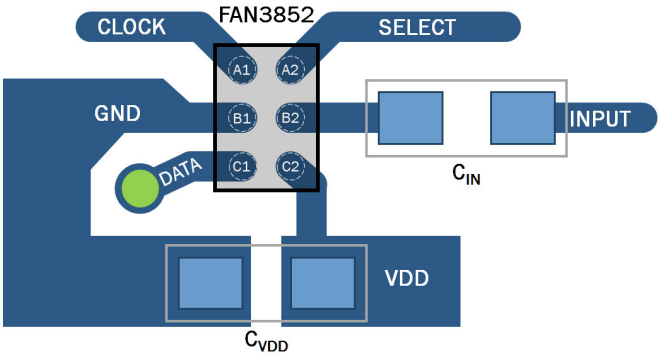


Figure 5. Example Top Layer Placement of Key Components & Traces

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