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AND9870

3-phase Inverter Power Module Application Note for the NFAP Series

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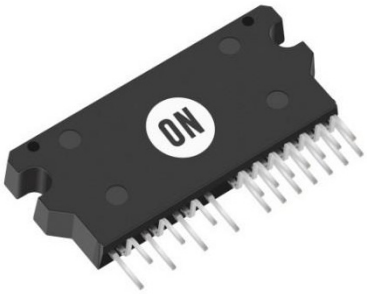
APPLICATION NOTE



Introduction

This application note provides practical guidelines for designing with the NFAP series power modules.

The NFAP series is an Intelligent Power Module (IPM) for 3−phase motor drives containing a three−phase inverter stage, gate drivers for the inverter stages and a thermistor. It uses ON Semiconductor's Insulated Metal Substrate (IMS) Technology.

Key Functions

- Highly Integrated Device Containing All High Voltage (HV) Control from HV−DC to 3−phase Outputs in a Single Small SIP Module
- Output Stage Uses IGBT/FRD Technology and Implements Under Voltage Protection (UVP) and Over−current Protection (OCP) with a Fault Detection Output Flag. Internal Bootstrap Diodes are Provided for the High−side Drivers
- Separate Pins for Each of the Three Low−side Emitter Terminals
- Thermistor for Substrate Temperature Measurement
- All Control Inputs and Status Outputs Have Voltage Levels Compatible with Microcontrollers
- Single V_{DD} Power Supply Due to Internal Bootstrap Circuit for High−side Gate Driver Circuit
- Mounting Holes for Easy Assembly of Heat Sink with Screws

A simplified block diagram of a motor control system is shown in Figure 1.

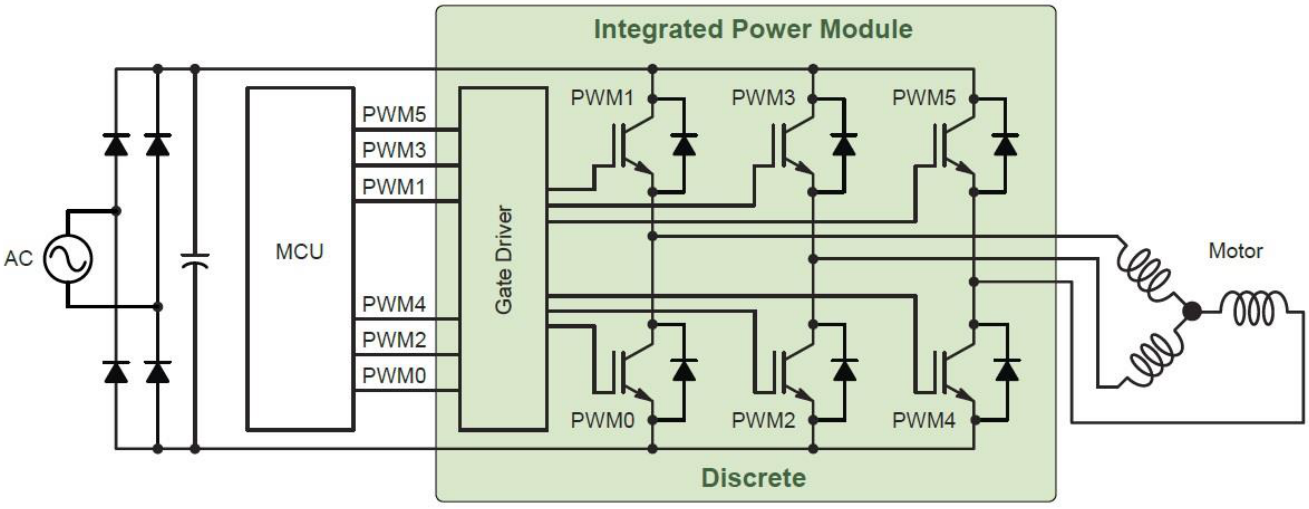


Figure 1. Motor Control System Block Diagram

Product Description

Table 1 gives an overview of the available devices in the NFAP series. For package drawing, please refer to Chapter Package Outline.

Table 1. DEVICE OVERVIEW

Device	**NFAP0560xxTT** (Note 1)	**NFAP1060L3TT**	**NFAP1560xxTT** (Note 1)
Package	SIP29 44.0x20.9 FP−1 − Vertical pins		
Voltage (VCEmax.)	600 V		
Current (Ic)	5 A	10 A	15 A
Peak Current (Ic)	10 A	20 A	30 A
Isolation Voltage	2000 V		
Input Logic	High−active		
Shunt Resistance	triple shunts / external		

1. Under development

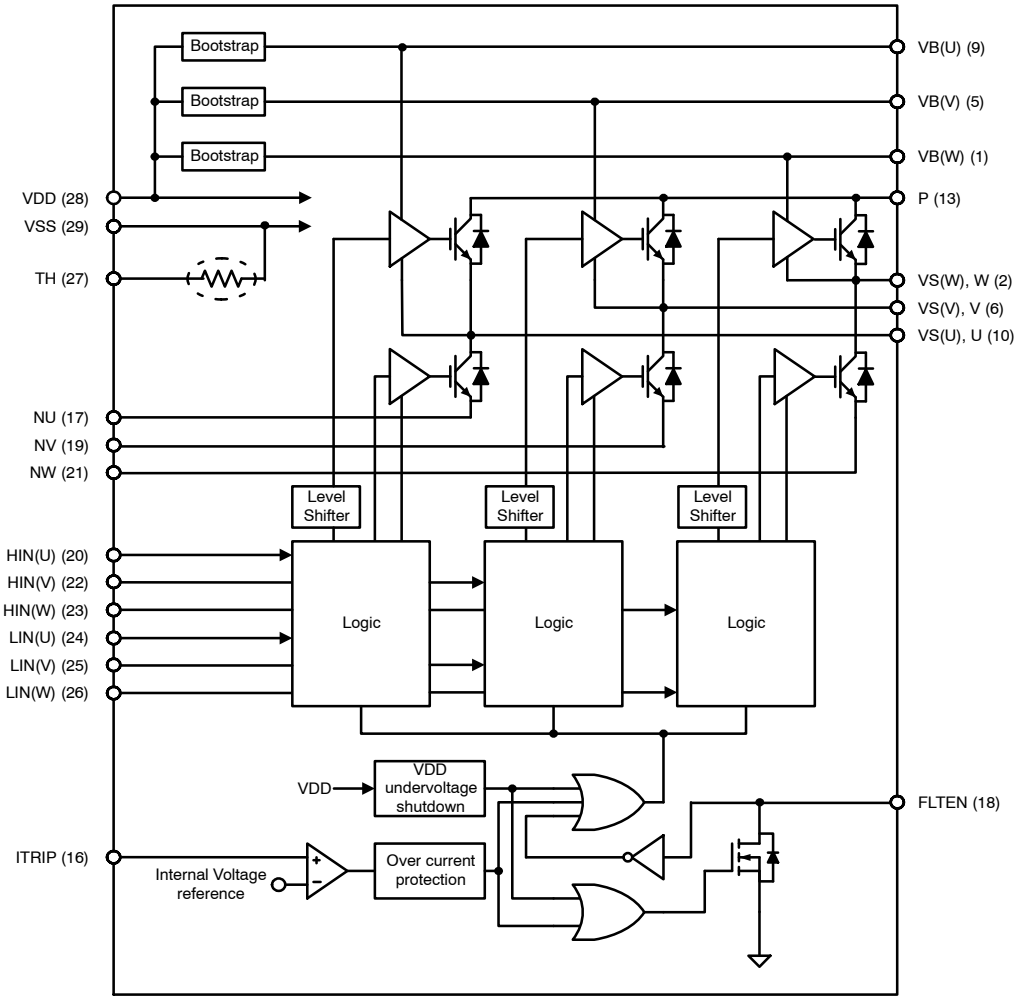


Figure 2. NFAP Series Internal Diagram

Three bootstrap circuits generate the voltage needed for driving the high−side IGBTs. The boost diodes are internal to the part and sourced from VDD (15 V). There is an internal level shift circuit for the high−side drive signals allowing all control signals to be driven directly from GND levels common with the control circuit such as the microcontroller without requiring external isolation with photo couplers.

Performance test guidelines

The methods used to test some datasheet parameters are shown in Figures 3 to 7.

Switching Time Definition and Performance Test Method

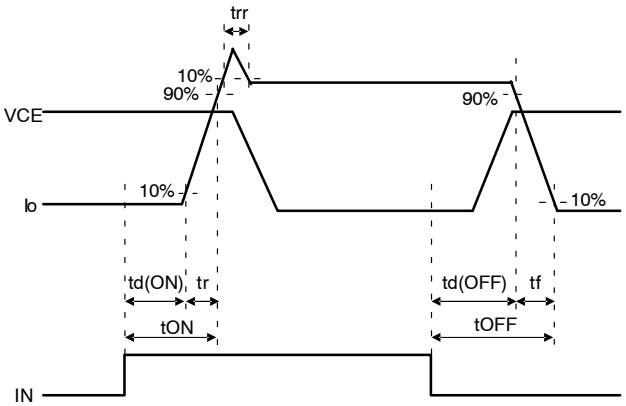


Figure 3. Switching Time Definition

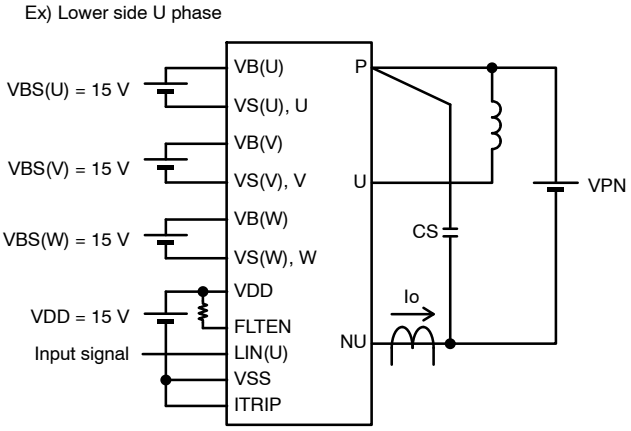


Figure 4. Evaluation Circuit (Inductive Load)

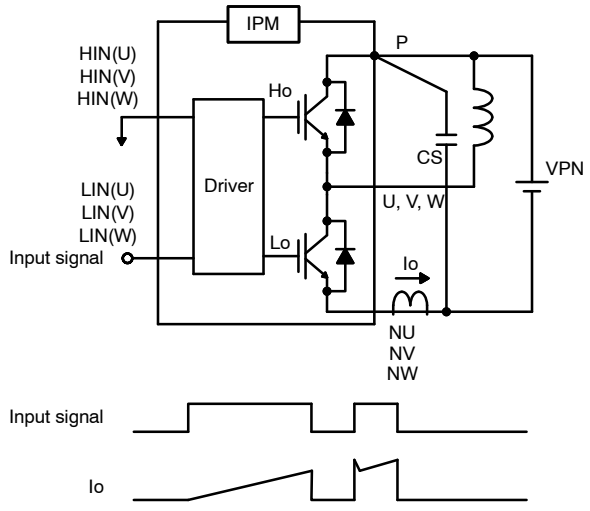


Figure 5. Switching Loss Measurement Circuit

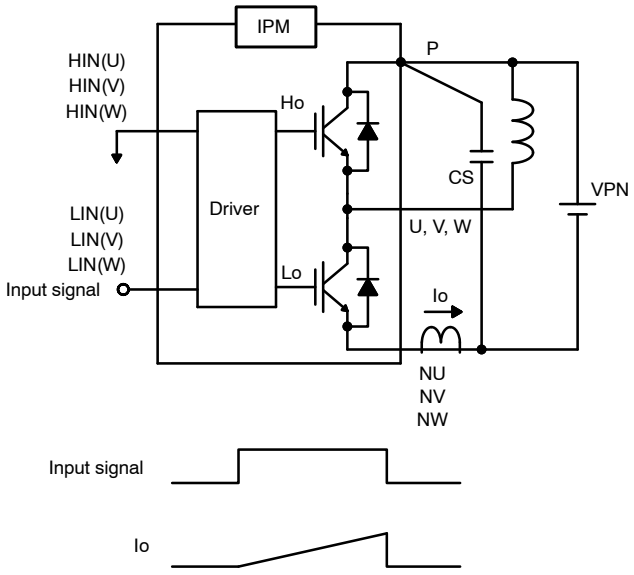


Figure 6. Reverse Bias Safe Operating Area Measurement Circuit

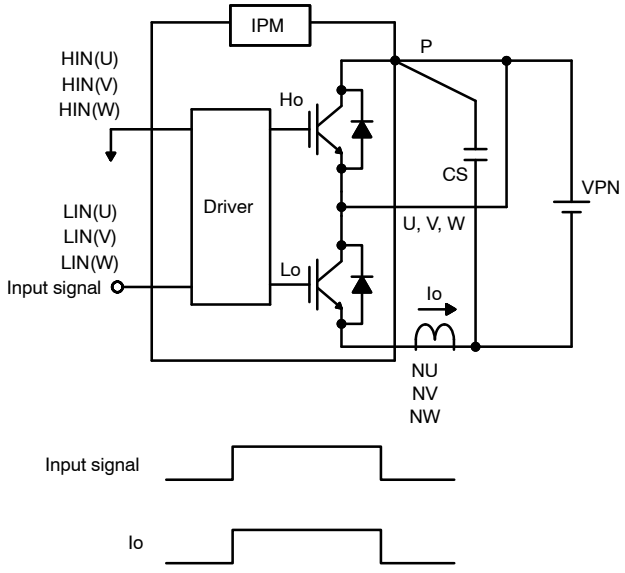


Figure 7. Short Circuit Safe Operating Area Measurement Circuit

Thermistor Characteristics

The TH pin are connected to a thermistor mounted on the module substrate. The thermistor is used to sense the internal substrate temperature. It has the following characteristics.

Table 2. NTC THERMISTOR SPECIFICATION

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{25}	Resistance	Tc = 25°C	45.59	47	48.41	kΩ
R_{125}	Resistance	Tc = 125°C	1.34	1.45	1.59	kΩ
B	B−Constant (25 to 50°C)		3953	4021	4033	K
	Temperature Range		−40	–	+125	°C

R_{25} is the value of the integrated NTC thermistor at Tc = 25°C. The resistance value is 47 kΩ ±3%. The temperature depended value is calculated as shown in the formula.

$$R(t) = R_{25} \times e^{B\left(\frac{1}{T} - \frac{1}{298}\right)} \quad \text{(eq. 1)}$$

The resulting in the NTC values over temperatures

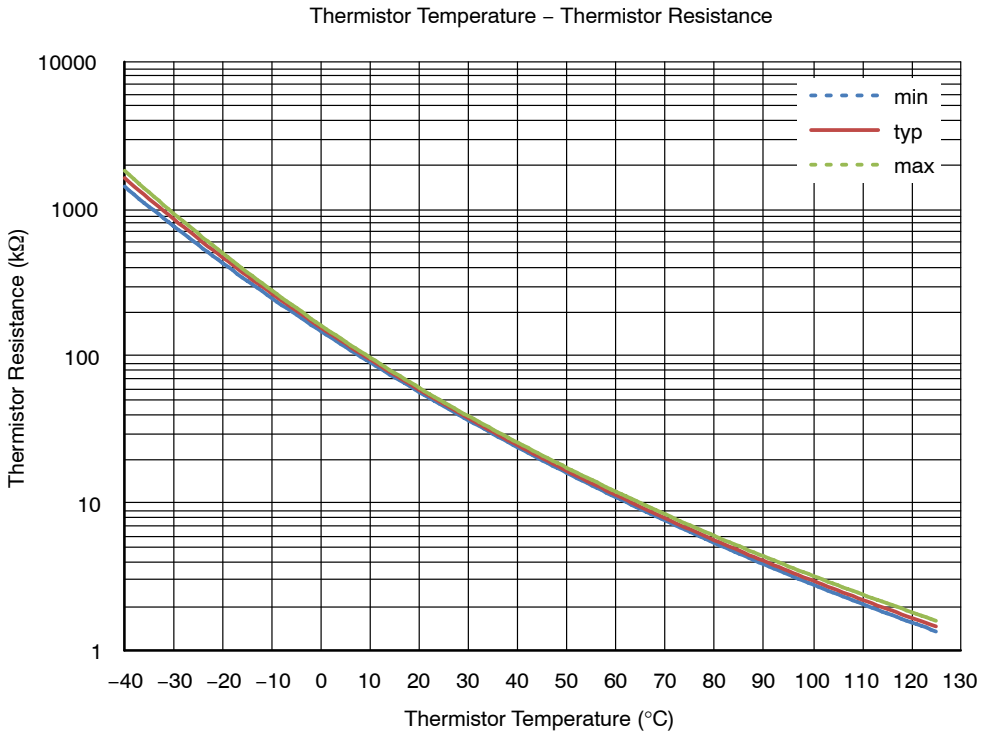


Figure 8. NTC Thermistor Resistance versus Temperature

Table 3. NTC THERMISTOR RESISTANCE VALUES

Tc [°C]	Resistance Value [kΩ]		
	Min	Typ	Max
−40	1422.2820	1633.0199	1830.4046
−39	1334.8310	1527.7671	1707.4947
−38	1253.2420	1429.9656	1593.6791
−37	1177.0910	1339.0418	1488.2255
−36	1105.9880	1254.4707	1390.4650

Tc [°C]	Resistance Value [kΩ]		
	Min	Typ	Max
−35	1039.5720	1175.7708	1299.7866
−34	977.5100	1102.4986	1215.6314
−33	919.4940	1034.2476	1137.4883
−32	865.2400	970.6439	1064.8893
−31	814.4840	911.3433	997.4057

Tc [°C]	Resistance Value [kΩ]		
	Min	Typ	Max
−30	766.9830	856.0292	934.6445
−29	722.5110	804.4110	876.2456
−28	680.8600	756.2195	821.8781
−27	641.8370	711.2076	771.2386
−26	605.2620	669.1465	724.0480
−25	570.9700	629.8266	680.0502
−24	538.8060	593.0528	639.0093
−23	508.6280	558.6461	600.7083
−22	480.3030	526.4404	564.9475
−21	453.7070	496.2825	531.5429
−20	428.7280	468.0303	500.3249
−19	405.2580	441.5531	471.1372
−18	383.1980	416.7295	443.8353
−17	362.4570	393.4462	418.2862
−16	342.9500	371.5997	394.3667
−15	324.5970	351.0934	371.9633
−14	307.3230	331.8372	350.9708
−13	291.0610	313.7487	331.2921
−12	275.7460	296.7499	312.8370
−11	261.3180	280.7698	295.5225
−10	247.7210	265.7416	279.2713
−9	234.9030	251.6033	264.0119
−8	222.8170	238.2976	249.6781
−7	211.4160	225.7708	236.2083
−6	200.6580	213.9733	223.5456
−5	190.5040	202.8586	211.6369
−4	180.9180	192.3762	200.4184
−3	171.8640	182.4947	189.8616
−2	163.3110	173.1763	179.9237
−1	155.2280	164.3860	170.5648
0	147.5870	156.0912	161.7480
1	140.3620	148.2606	153.4388
2	133.5290	140.8668	145.6051
3	127.0640	133.8826	138.2170
4	120.9450	127.2827	131.2466
5	115.1530	121.0447	124.6681
6	109.6680	115.1472	118.5350

Tc [°C]	Resistance Value [kΩ]		
	Min	Typ	Max
7	104.4730	109.5688	112.8090
8	99.5500	104.2909	107.3890
9	94.8860	99.2962	102.2580
10	90.4630	94.5679	97.3980
11	86.2700	90.0902	92.7940
12	82.2920	85.8485	88.4320
13	78.5190	81.8296	84.2960
14	74.9380	78.0202	80.3760
15	71.5380	74.4086	76.6580
16	68.3100	70.9834	73.1300
17	65.2440	67.7340	69.7840
18	62.3320	64.6508	66.6070
19	59.5640	61.7240	63.5910
20	56.9330	58.9454	60.7270
21	54.4320	56.3061	58.0070
22	52.0540	53.7994	55.4220
23	49.7910	51.4170	52.9660
24	47.6390	49.1528	50.6300
25	45.5900	47.0000	48.4100
26	43.6010	44.9530	46.3390
27	41.7090	43.0054	44.3670
28	39.9090	41.1528	42.4890
29	38.1950	39.3892	40.7000
30	36.5640	37.7101	38.9960
31	35.0110	36.1116	37.3710
32	33.5310	34.5886	35.8220
33	32.1210	33.1381	34.3450
34	30.7780	31.7552	32.9370
35	29.4970	30.4375	31.5930
36	28.2770	29.1812	30.3110
37	27.1120	27.9834	29.0870
38	26.0020	26.8410	27.9190
39	24.9430	25.7506	26.8040
40	23.9320	24.7104	25.7380
41	22.9670	23.7170	24.7210
42	22.0460	22.7688	23.7480
43	21.1660	21.8636	22.8190

Tc [°C]	Resistance Value [kΩ]		
	Min	Typ	Max
44	20.3260	20.9988	21.9310
45	19.5230	20.1719	21.0820
46	18.7560	19.3825	20.2690
47	18.0230	18.6276	19.4930
48	17.3220	17.9059	18.7490
49	16.6520	17.2156	18.0380
50	16.0110	16.5553	17.3570
51	15.3980	15.9238	16.7060
52	14.8110	15.3196	16.0820
53	14.2500	14.7408	15.4840
54	13.7130	14.1869	14.9120
55	13.1990	13.6568	14.3630
56	12.7060	13.1489	13.8380
57	12.2340	12.6623	13.3340
58	11.7820	12.1963	12.8510
59	11.3490	11.7496	12.3880
60	10.9340	11.3211	11.9440
61	10.5366	10.9109	11.5180
62	10.1508	10.5176	11.1090
63	9.7810	10.1403	10.7170
64	9.4265	9.7787	10.3400
65	9.0865	9.4315	9.9790
66	8.7603	9.0982	9.6320
67	8.4475	8.7786	9.2990
68	8.1472	8.4714	8.9790
69	7.8591	8.1768	8.6710
70	7.5825	7.8935	8.3760
71	7.3163	7.6209	8.0920
72	7.0606	7.3592	7.8190
73	6.8150	7.1080	7.5560
74	6.5791	6.8663	7.3040
75	6.3524	6.6342	7.0610
76	6.1352	6.4109	6.8280
77	5.9263	6.1963	6.6030
78	5.7256	5.9898	6.3870
79	5.5325	5.7918	6.1790
80	5.3468	5.6004	5.9790

Tc [°C]	Resistance Value [kΩ]		
	Min	Typ	Max
81	5.1688	5.4169	5.7860
82	4.9975	5.2404	5.6010
83	4.8326	5.0706	5.4220
84	4.6740	4.9070	5.2500
85	4.5213	4.7493	5.0840
86	4.3737	4.5968	4.9240
87	4.2317	4.4506	4.7700
88	4.0948	4.3095	4.6210
89	3.9630	4.1730	4.4780
90	3.8361	4.0419	4.3400
91	3.7137	3.9157	4.2070
92	3.5958	3.7937	4.0790
93	3.4821	3.6764	3.9550
94	3.3725	3.5632	3.8350
95	3.2668	3.4534	3.7200
96	3.1654	3.3483	3.6090
97	3.0675	3.2465	3.5010
98	2.9730	3.1485	3.3980
99	2.8819	3.0542	3.2980
100	2.7940	2.9630	3.2010
101	2.7091	2.8743	3.1070
102	2.6272	2.7892	3.0170
103	2.5481	2.7070	2.9300
104	2.4717	2.6277	2.8460
105	2.3979	2.5507	2.7640
106	2.3264	2.4763	2.6860
107	2.2572	2.4047	2.6100
108	2.1904	2.3353	2.5360
109	2.1258	2.2680	2.4650
110	2.0634	2.2033	2.3960
111	2.0034	2.1404	2.3300
112	1.9454	2.0799	2.2650
113	1.8893	2.0215	2.2030
114	1.8351	1.9650	2.1430
115	1.7827	1.9099	2.0840
116	1.7322	1.8573	2.0280
117	1.6834	1.8061	1.9730

Tc [°C]	Resistance Value [kΩ]		
	Min	Typ	Max
118	1.6361	1.7562	1.9200
119	1.5904	1.7086	1.8690
120	1.5461	1.6622	1.8190
121	1.5031	1.6169	1.7710
122	1.4613	1.5733	1.7250
123	1.4210	1.5309	1.6790
124	1.3819	1.4902	1.6360
125	1.3440	1.4500	1.5930

Protection Functions

This chapter describes the protection functions.

- Over−current protection
- Short circuit protection
- Under voltage lockout (UVLO) protection
- Cross conduction prevention

Over−current Protection

NFAP series modules use an external shunt resistor for the OCP functionality. As shown in Figure 9, the emitters of all three low−side IGBTs are brought out to module pins. The external OCP circuit consists of a shunt resistor and a RC filter network. If the application uses three separate shunts, an op−amp circuit or comparator circuit are used to monitor the three separate shunts and provide an over−current signal.

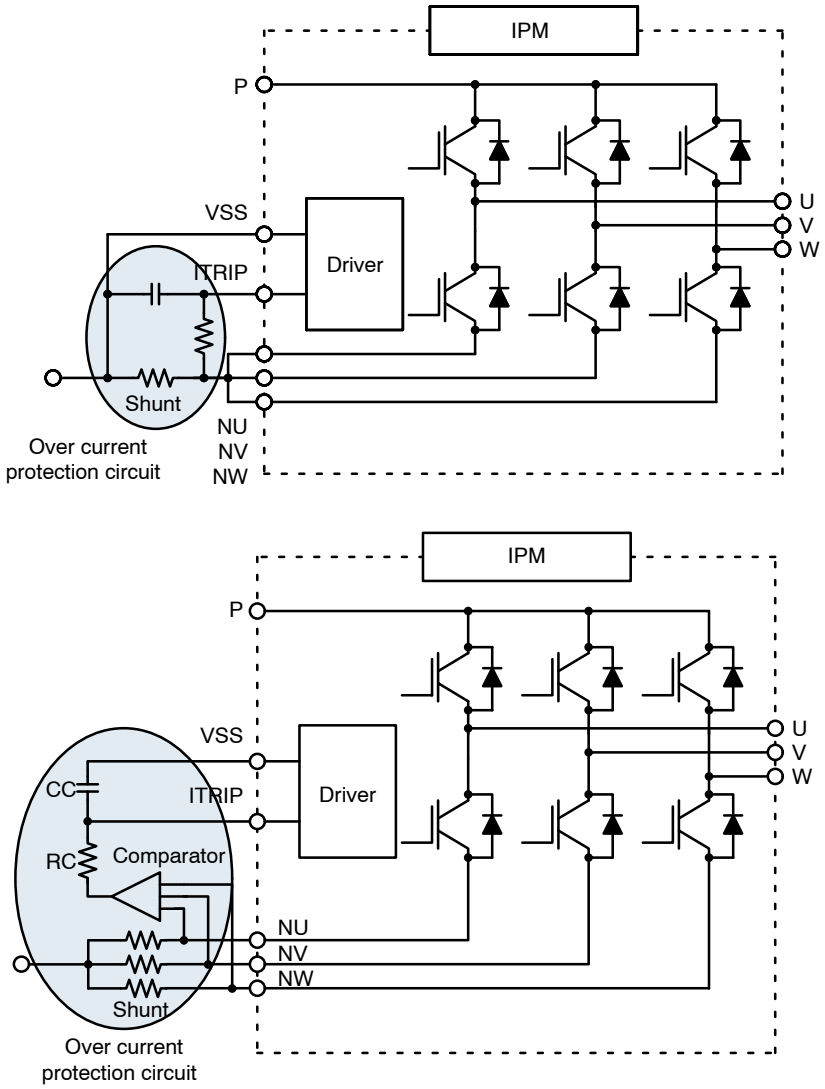


Figure 9. Over−current Protection Circuit, One Shunt R Type and Three Shunt R Type

The OCP function is implemented by comparing the ITRIP input voltage with an internal reference voltage of 0.49 V (typ). If the voltage on this terminal exceeds the trip level, an OCP fault is triggered. This voltage is the same as the voltage across the shunt resistor.

NOTE: The current value of the OCP needs to be set by correctly sizing the external shunt resistor to less than the module's maximum current rating.

When an OCP fault is detected, all internal gate drive signals for the IGBTs become inactive and the fault signal output is activated. The FLTEN signal has an open drain output, so when there is a fault, the output is pulled low.

A RC filter is used on the input to prevent an erroneous OCP detection due to normal switching noise or recovery diode current. The time constant of that RC filter should be set to a value between 1.5 μ to 2 μs. The recommended RC value for the time constant 2 μs is as RC = 100 Ω, CC = 20 nF. In any case the time constant must be shorter than the IGBTs short current safe operating area (SCSOA). Please refer to Data Sheet for SCSOA. The resulting OCP level due to the filter time constant is shown in Figure 10.

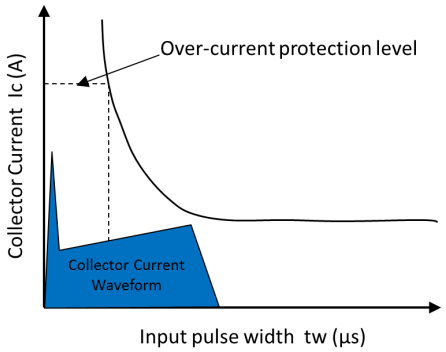


Figure 10. Filter Time Constant

For optimal performance all traces around the shunt resistor need to be kept as short as possible.

Figure 11 shows the sequence of events in case of an OCP event.

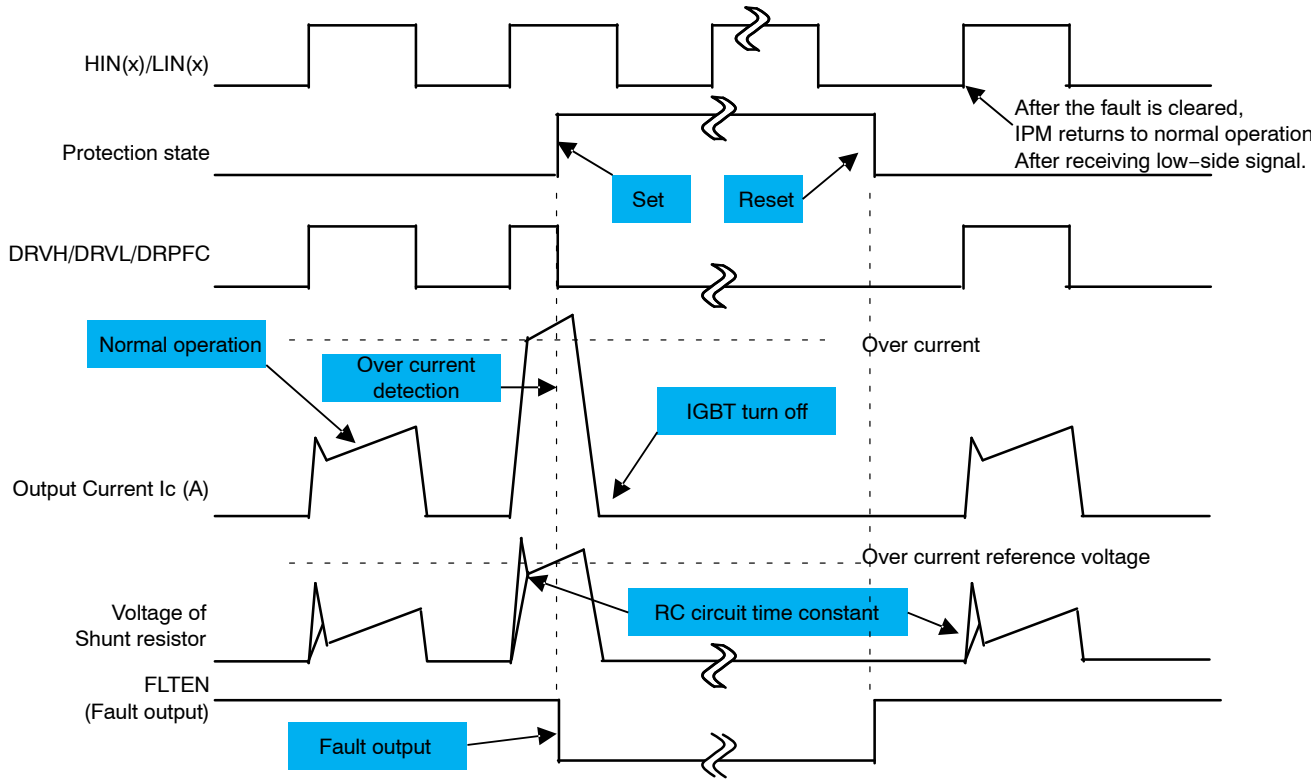


Figure 11. Overcurrent Protection Timing Diagram

Under Voltage Lockout Protection

The UVLO protection is designed to prevent unexpected operating behavior as described in Table 4. Both High−side and Low−side have under voltage protection. The low−side UVLO condition is indicated on the FAULT output. During the low−side UVLO state the FAULT output is continuously driven low. A high−side UVLO condition is not indicated on the FAULT output.

Table 4. MODULE OPERATION ACCORDING TO VDD VOLTAGE

VDD Voltage (Typ. Value)	Operation Behavior
<12.5 V	As the voltage is lower than the UVLO threshold the control circuit is not fully turned on. A perfect functionality cannot be guaranteed.
12.5 V – 14.0 V	IGBTs can work, however conduction and switching losses increase due to low voltage gate signal.
14.0 V – 16.5 V	Recommended conditions
16.5 V – 20.0 V	IGBTs can work. Switching speed is faster and saturation current higher, increasing short−circuit broken risk.
>20.0 V	Control circuit is destroyed. Absolute max. Rating is 20 V.

The sequence of events in case of a low−side UVLO event (IGBTs turned off and active fault output) is shown in Figure 12. Figure 13 shows the same for a high−side UVLO (IGBTs turned off but *no* fault output).

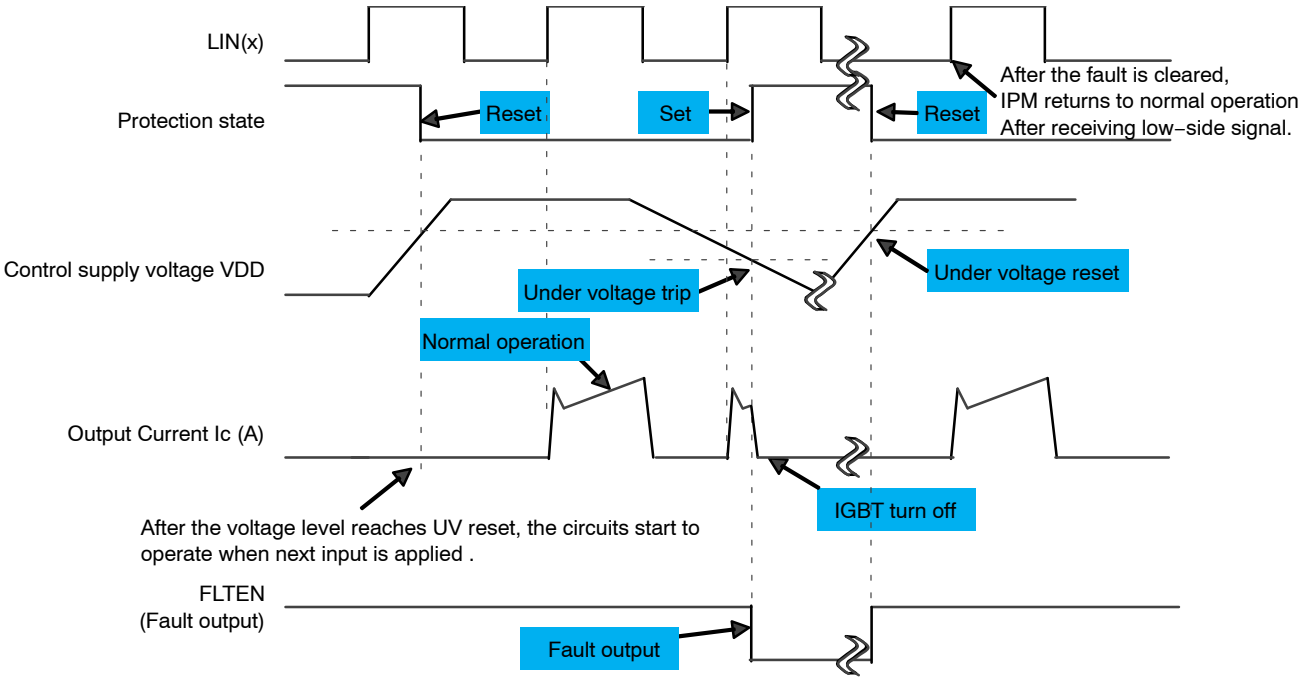


Figure 12. Low−side UVLO Timing Diagram

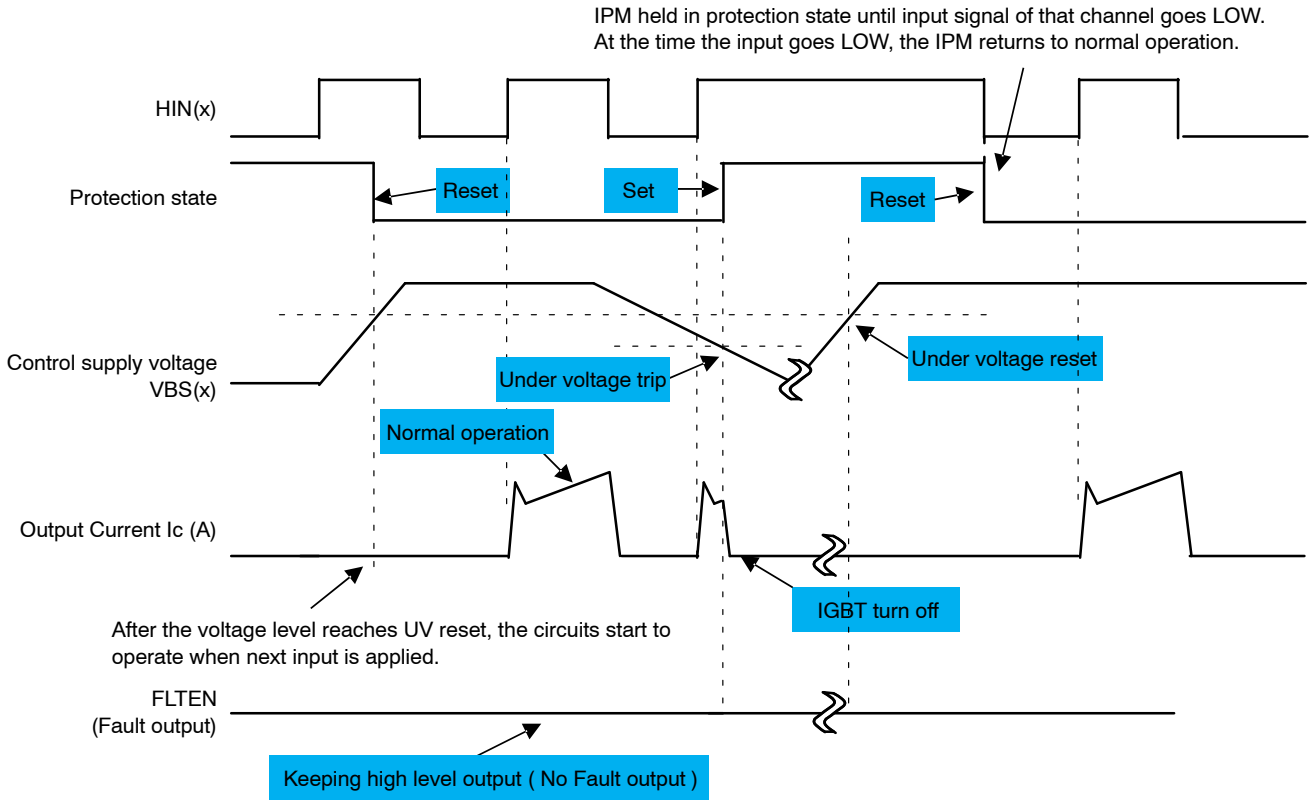


Figure 13. High−side UVLO Timing Diagram

Cross−conduction Prevention

The NFAP series implements cross−conduction prevention logic at the gate driver to avoid simultaneous drive of the low−side and high−side IGBTs as shown in Figure 14.

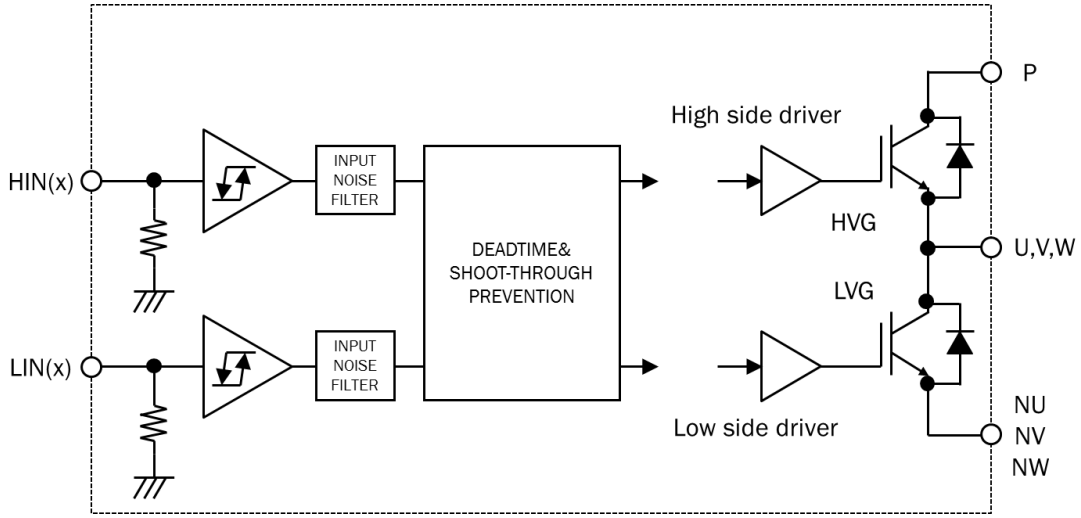


Figure 14. Cross−conduction Prevention

If both high−side and low−side drive inputs are active (HIGH) the logic prevents both gates from being driven as shown in Figure 15 below.

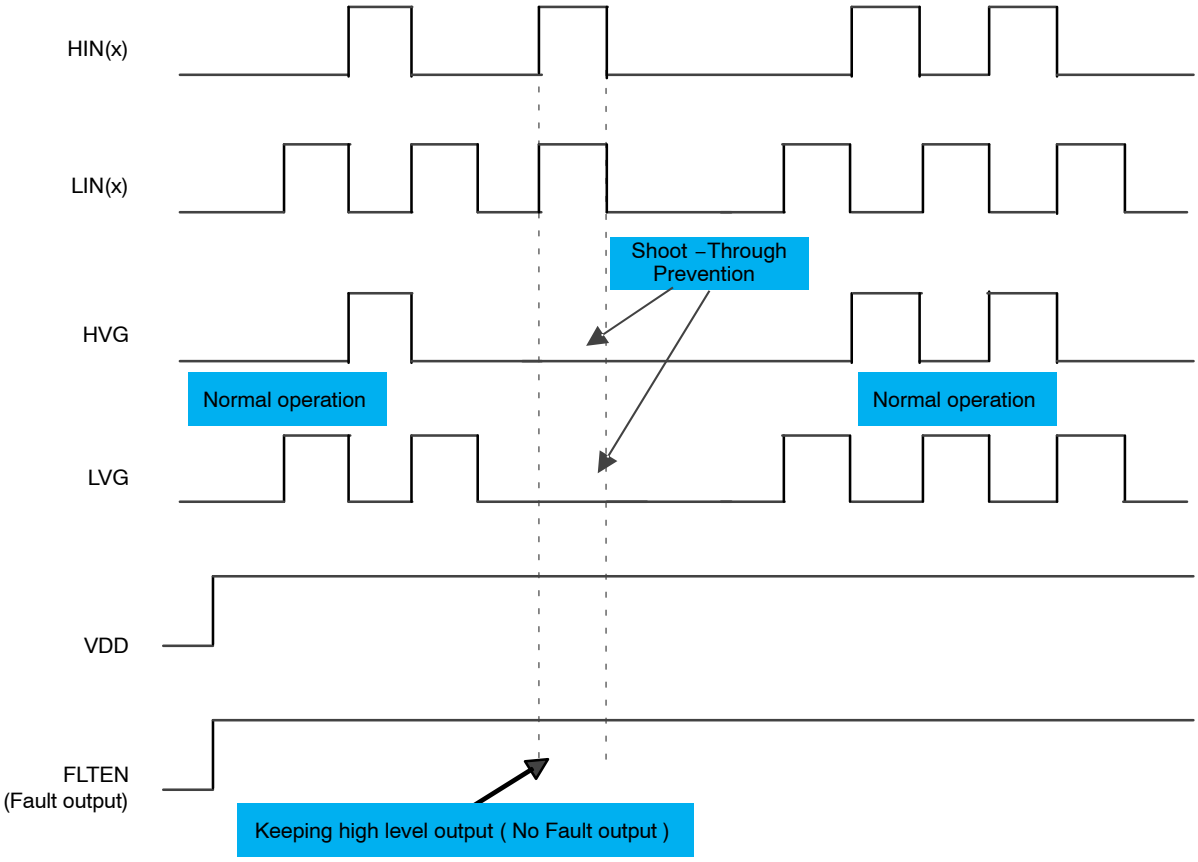


Figure 15. Cross−conduction Prevention Timing Diagram

Even if cross−conduction on the IGBTs due to incorrect external driving signals is prevented by the circuitry, the driving signals (HIN and LIN) need to include a “dead time”. This period where both inputs are inactive between either one becoming active is required due to the internal delays within the IGBTs.

Figure 16 shows the delay from the HIN−input via the internal high−side gate driver to high−side IGBT, the delay from the LIN−input via the internal low−side gate driver to low−side IGBT and the resulting minimum dead time which is equal to the potential shoot through period:

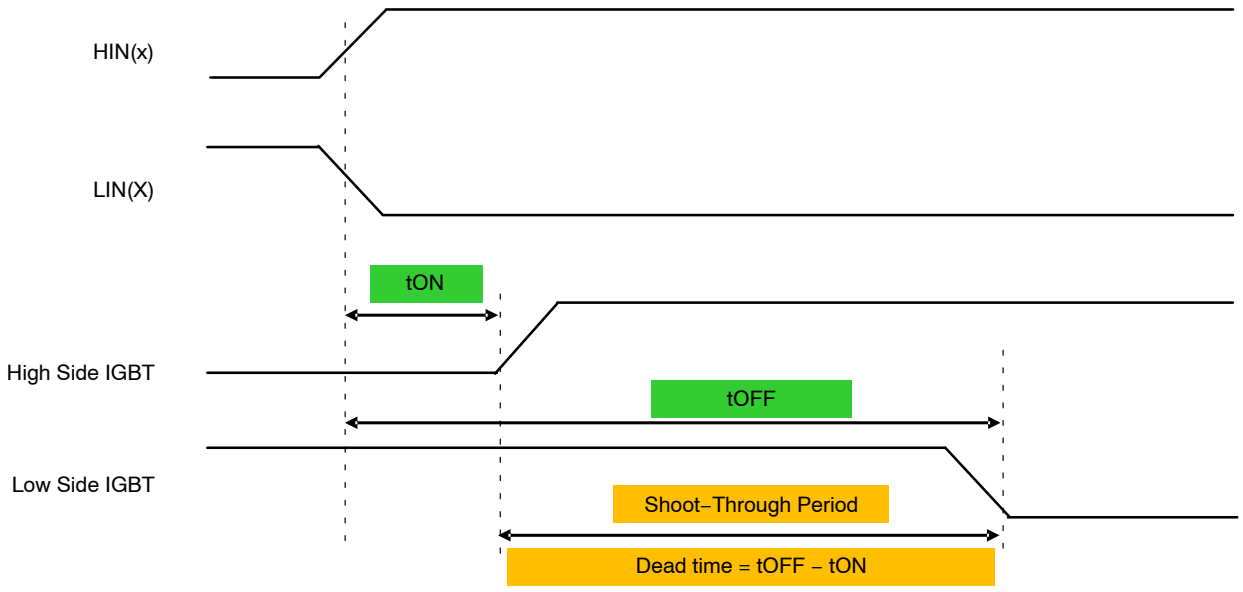


Figure 16. Shoot−through Period

PCB Design and Mounting Guidelines

This chapter provides guidelines for an optimized design and PCB layout as well as module mounting recommendations to appropriately handle and assemble the IPM.

Application (Schematic) Design

Figure 17 gives an overview of the external components and circuits when designing with the NFAP series modules.

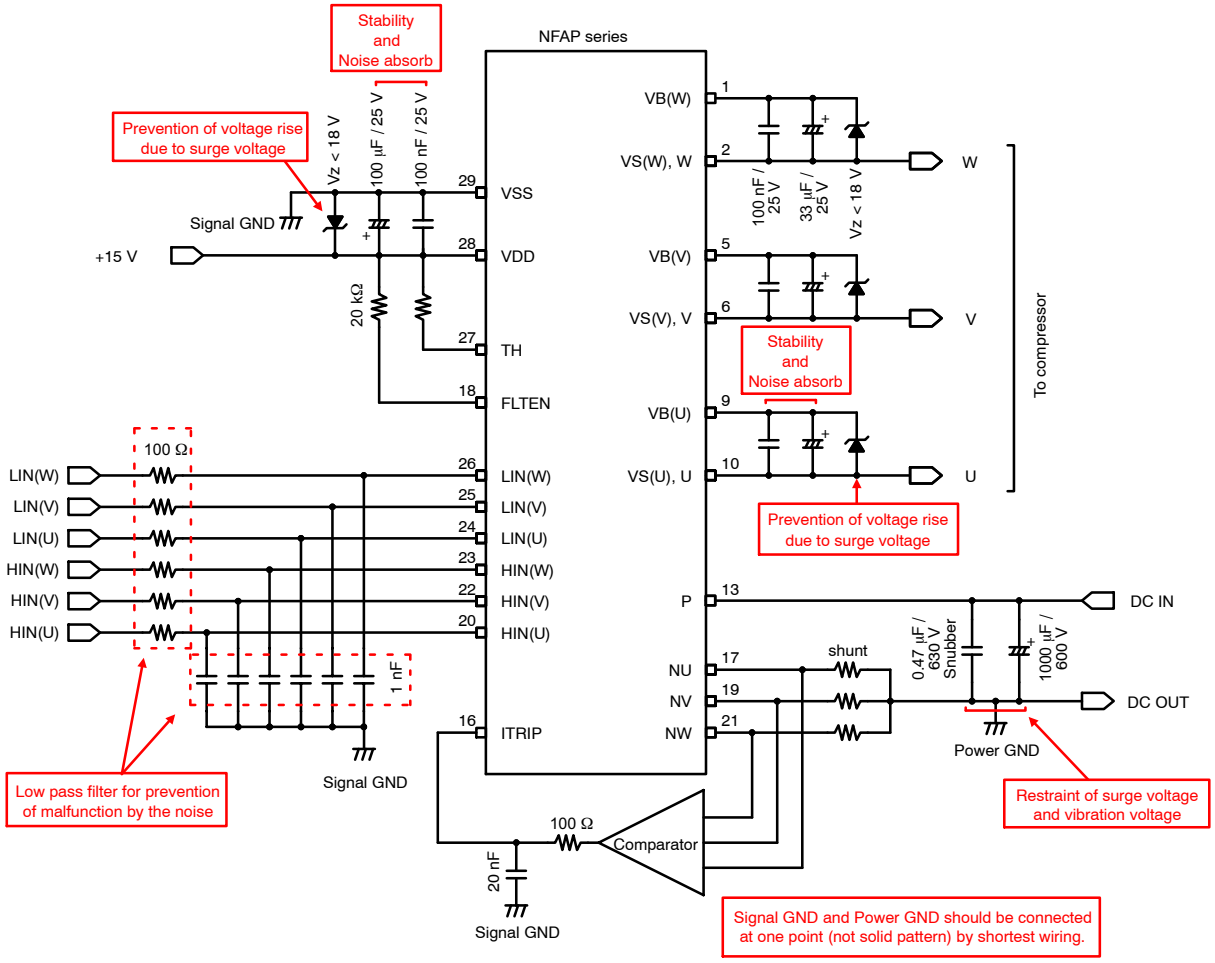


Figure 17. NFAP Series Application Circuit

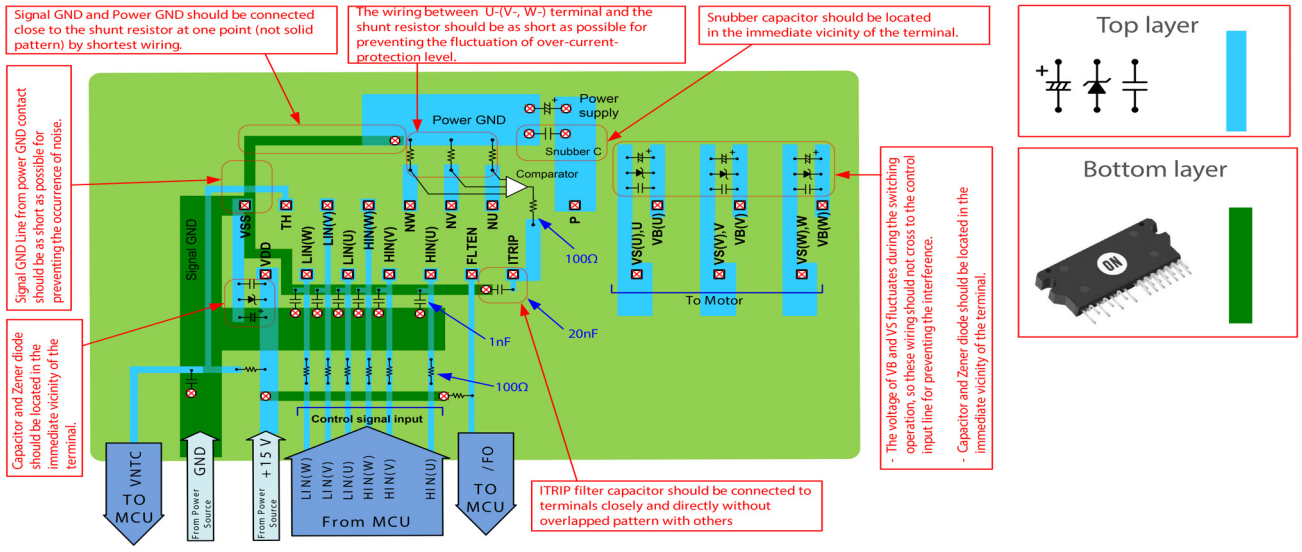


Figure 18. NFAP Recommended Layout

Pin by Pin Design and Usage Notes

This section provides pin by pin PCB layout recommendations and usage notes. A complete list of module pins is given in Chapter Package Outline.

- *P, NU, NV, NW:*
  These pins are connected with the main DC power supply. The applied voltage is up to the VPN level. Overvoltage on these pins could be generated by voltage spikes during switching at the floating inductance of the wiring. To avoid this behavior the wire traces need to be as short as possible to reduce the floating inductance. In addition a snubber capacitor needs to be placed as close as possible to these pins to stabilize the voltage and absorb voltage surges.
- *U, V, W:*
  These are the output pins for connecting the 3−phase motor. They share the same GND potential with each of the high−side control power supplies. Therefore they are also used to connect the GND of the bootstrap capacitors. These bootstrap capacitors should be placed as close to the module as possible.
- *VDD, VSS:*
  These pins provide power to the low−side gate drivers, the protection circuits and the bootstrap circuits. The voltage between these terminals is monitored by the UVLO circuit. The VSS terminal is the reference voltage for the input control signals.Since current flows instantaneously when switching IGBTs, place decoupling capacitor for ripple and surge noise as close as possible to the VDD terminal.
- *VB(U), VB(V), VB(W):*
  The VBx pins are internally connected to the positive supply of the high−side drivers. The supply needs to be floating and electrically isolated. The boot−strap circuit shown in Figure 19 forms this power supply individually for every phase. Due to integrated boot FET only an external boot capacitor (CB) is required.
  CB is charged when the following conditions are met.
  Motor terminal voltage is low level for low side IGBT or low side diode conducting.
  The capacitor is discharged while the high−side driver is activated.
  Thus CB needs to be selected taking the maximum on time of the high−side and the switching frequency into account.

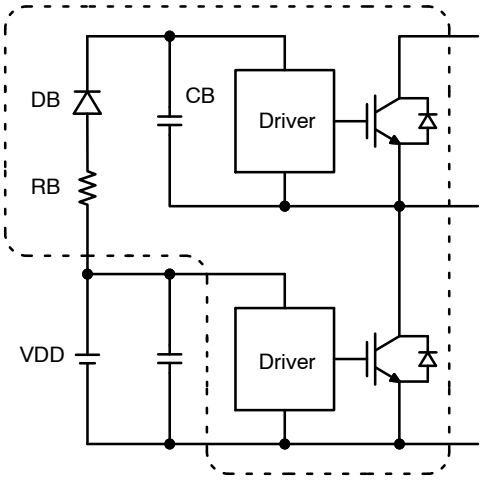


Figure 19. Bootstrap Circle

The voltages on the high−side drivers are individually monitored by the under voltage protection circuit. If there is a UVLO fault on any given phase, the output on that phase is disabled.

Typically a CB value of less or equal 47 μF (±20%) is used. In case the CB value needs to be higher, an external resistor (20 Ω or less) should be used in series with the capacitor to avoid high currents which can cause malfunction of the IPM.

- *HIN(U), LIN(U), HIN(V), LIN(V), HIN(W), LIN(W):*

  These pins are the control inputs for the power stages. The inputs on HIN(U) / HIN(V) / HIN(W) control the high−side transistors of U / V / W, and the inputs on LIN(U) / LIN(V) / LIN(W) control the low−side transistors of U/V/W respectively. The input logic is active HIGH. An external micro−controller can directly drive these inputs without need for isolation.

  Simultaneous activation of both low and high side is prevented internally to avoid shoot through at the power stage. However, due to IGBT switching delays the control signals must include a dead−time.

  The equivalent input stage circuit is shown in Figure 20.

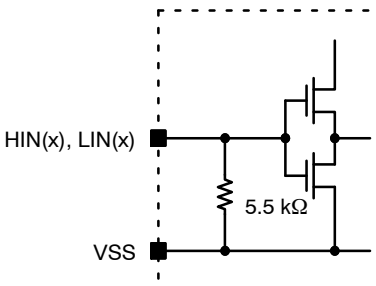


Figure 20. Internal Input Circuit

NOTE: *After applying VDD, it is necessary to input the low−side signal for starting the high−side operation.*

- *FLTEN:*

  The FLTEN pin is an active low output (open−drain output). It is used to indicate an internal fault condition of the module. The structure is shown in Figure 21. The sink current of IoSD during an active fault is nominal 2 mA @ 0.1 V. Depending on the interface supply voltage, the external pull−up resistor (RP) needs to be selected to set the low voltage below the VIL trip level.

  For the commonly used supplies:

  Pull up voltage = 15 V −> RP ≥ 20 kΩ

  Pull up voltage = 5 V −> RP ≥ 6.8 kΩ

  Pull up voltage = 3.3 V −> RP ≥ 3.9 kΩ

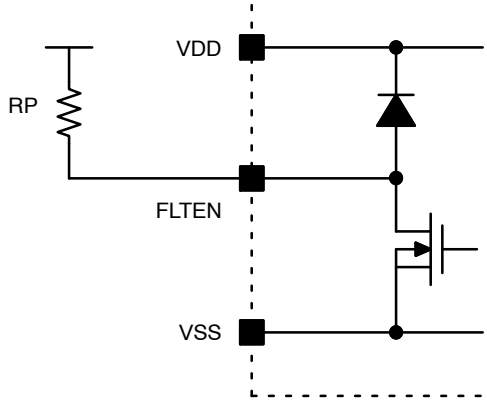


Figure 21. Fault Connection

For a detailed description of the fault operation refer to Chapter Protection Functions.

NOTE: The Fault signal does not permanently latch. After the protection event ended, and the fault clear time (20 μs) passed, the module's operation is re−started by inputting the low−side signal. Therefore the input needs to be driven low externally activated as soon as a fault is detected.

- *ITRIP:*

  This pin is used to enable an OCP function. When the voltage of this pin exceeds a reference voltage, the OCP function operates. For details of the OCP operation refer to Chapter Protection Functions.

- *TH:*

  An internal thermistor to sense the substrate temperature is connected between TH and VSS. By connecting an external pull−up resistor to arbitrary voltage, the module temperature can be monitored. Please refer to heading Thermistor Characteristics for details of the thermistor.

  NOTE: This is the only means to monitor the substrate temperature indirectly.

Heat Sink Mounting and Torque

If a heat sink is used, insufficiently secure or inappropriate mounting can lead to a failure of the heat sink to dissipate heat adequately.

The following general points should be observed when mounting IPM on a heat sink:

1. Verify the following points related to the heat sink:
   - There must be no burrs on aluminum or copper heat sinks.
   - Screw holes must be countersunk.
   - There must be no unevenness in the heat sink surface that contacts IPM.
   - There must be no contamination on the heat sink surface that contacts IPM.
2. Highly thermal conductive silicone grease needs to be applied to the whole back (substrate side) uniformly, and mount IPM on a heat sink. If the device is removed, grease must be applied again.
3. For a good contact between the IPM and the heat sink, the mounting screws should be tightened gradually and sequentially while a left/right balance in pressure is maintained. Either a bind head screw or a truss head screw is recommended. Please do not use tapping screw. We recommend using a flat washer in order to prevent slack.

The standard heat sink mounting condition of the NFAP series is as follows.

Table 5. HEAT SINK MOUNTING

Item	Recommended Condition
Pitch	40.6 ±0.1 mm (Please refer to Package Outline Diagram)
Screw	Diameter : M3 Bind machine screw, Truss machine screw, Pan machine screw
Washer	Plane washer The size is D: 7 mm, d: 3.2 mm and t: 0.5 mm JIS B 1256 (Figure 23)
Heat sink	Material: Aluminum or Copper Warpage (the surface that contacts IPM) : –50 to 100 μm Screw holes must be countersunk. No contamination on the heat sink surface that contacts IPM.
Torque	Final tightening : 0.6 to 0.9 Nm Temporary tightening : 20 to 30% of final tightening
Grease	Silicone grease. Thickness : 100 to 200 μm Uniformly apply silicon grease to whole back. (Figure 24)

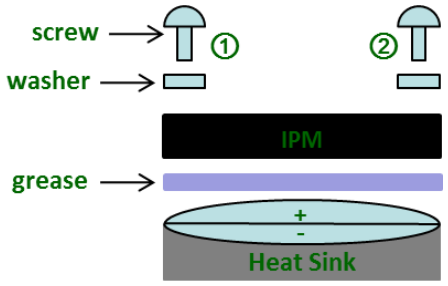


Figure 22. Mount IPM on a Heat Sink

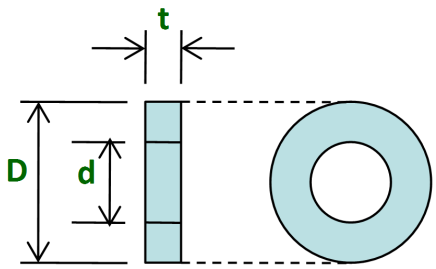


Figure 23. Size of Washer

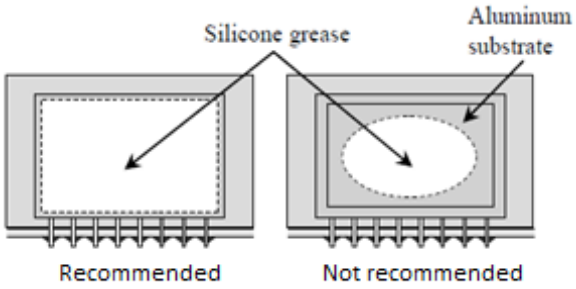


Figure 24. Uniform Application of Grease Recommended

Steps to mount an IPM on a heat sink

1st: Temporarily tighten maintaining a left/right balance.

2nd : Finally tighten maintaining a left/right balance.

Mounting and PCB Considerations

In designs in which the PCB and the heat sink are mounted to the chassis independently, use a mechanical design which avoids a gap between IPM and the heat sink, or which avoids stress to the lead frame of IPM by an assembly that slipping IPM is forcibly fixed to the heat sink with a screw.

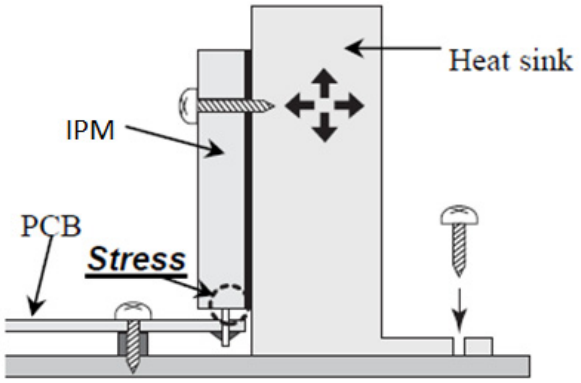


Figure 25. Fix to Heat Sink

Maintain a separation distance of at least 1.5 mm between the IPM case and the PCB. In particular, avoid mounting techniques in which the IPM substrate or case directly contacts the PCB. Do not mount IPM with a tilted condition for PCB. This can result in stress being applied to the lead frame and IPM substrate could short out tracks on the PCB. If stress is given by compulsory correction of a lead frame after the mounting, a lead frame may drop out.

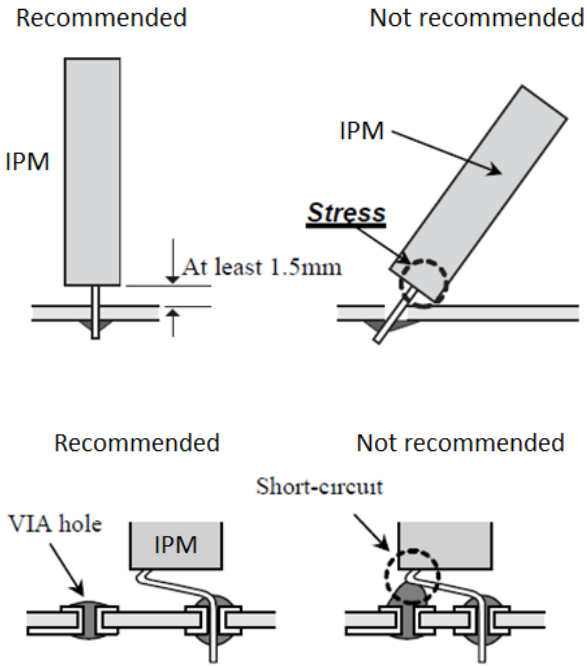


Figure 26. Mounting Position on PCB

Since the use of sockets to mount IPM can result in poor contact with IPM leads, we strongly recommend making direct connections to PCB.

Since the use of sockets to mount IPM can result in poor contact with IPM leads, we strongly recommend making direct connections to PCB.IPMs are flame retardant. However, under certain conditions, it may burn, and poisonous gas may be generated or it may explode. Therefore, the mounting structure of the IPM should also be flame retardant.

Mounting on a PCB

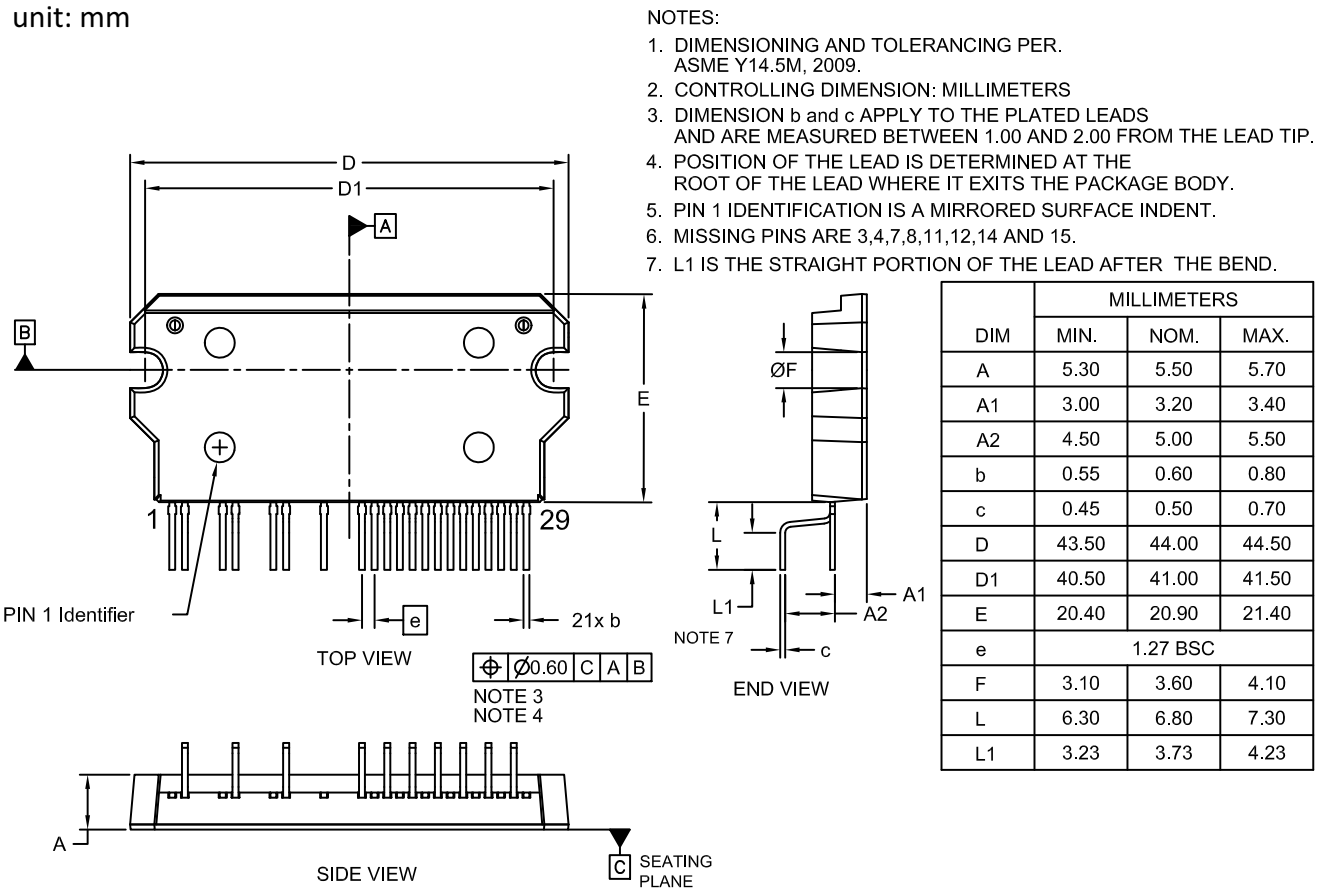
1. Align the lead frame with the holes in the PCB and do not use excessive force when inserting the pins into the PCB. To avoid bending the lead frames, do not try to force pins into the PCB unreasonably.
2. Do not insert IPM into PCB with an incorrect orientation, i.e. be sure to prevent reverse insertion. IPMs may be destroyed or suffer a reduction in their operating lifetime by this mistake.
3. Do not bend the lead frame.

Package Outline

NFAP series is single−inline−package.

Every second pin is bent forward to form two rows on the PCB see Figure 27.

Package Outline and Dimension
SIP29, 44.0x20.9 FP−1
CASE 127FB
ISSUE O



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	5.30	5.50	5.70
A1	3.00	3.20	3.40
A2	4.50	5.00	5.50
b	0.55	0.60	0.80
c	0.45	0.50	0.70
D	43.50	44.00	44.50
D1	40.50	41.00	41.50
E	20.40	20.90	21.40
e	1.27 BSC		
F	3.10	3.60	4.10
L	6.30	6.80	7.30
L1	3.23	3.73	4.23

Figure 27. Package Outline

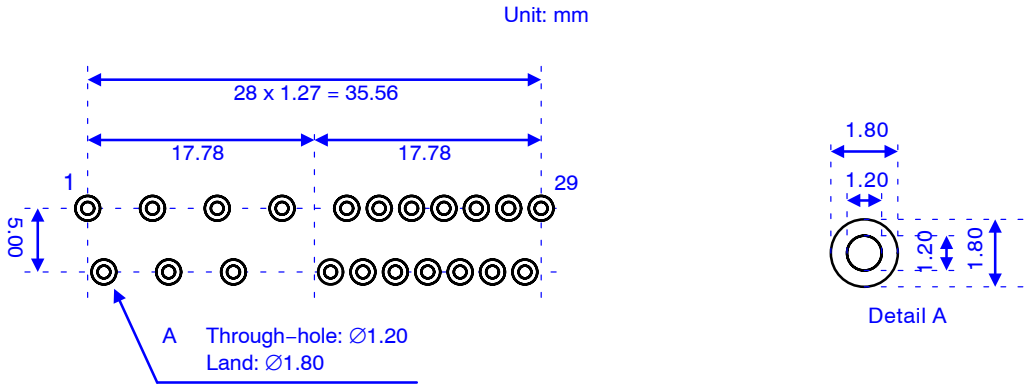


Figure 28. Recommended Land Pattern

Marking Diagram

NFAP1060L3TT = Specific Device Code
ZZZ = Assembly Lot Code
A = Assembly Location
T = Test Location
Y = Year
WW = Work Week
Device marking is on package top side

Figure 29. Marking Diagram

Pin Out Description

PIN OUT DESCRIPTION

Pin No.	Name	Description
1	VB(W)	High−Side Bias Voltage for W phase IGBT Driving
2	VS(W), W	High−Side Bias Voltage GND for W phase IGBT Driving, Output for W Phase
5	VB(V)	High−Side Bias Voltage for V phase IGBT Driving
6	VS(V), V	High−Side Bias Voltage GND for V phase IGBT Driving, Output for V Phase
9	VB(U)	High−Side Bias Voltage for U phase IGBT Driving
10	VS(U), U	High−Side Bias Voltage GND for U phase IGBT Driving, Output for U Phase
13	P	Positive DC−Link Input
16	ITRIP	Input for Current Protection
17	NU	Negative DC−Link Input for U Phase
18	FLTEN	Fault Output, Enable Input
19	NV	Negative DC−Link Input for V Phase
20	HIN(U)	Signal Input for High−Side U Phase
21	NW	Negative DC−Link Input for W Phase
22	HIN(V)	Signal Input for High−Side V Phase
23	HIN(W)	Signal Input for High−Side W Phase
24	LIN(U)	Signal Input for Low−Side U Phase
25	LIN(V)	Signal Input for Low−Side V Phase
26	LIN(W)	Signal Input for Low−Side W Phase
27	TH	Series Resister for Thermistor (Temperature Detection)
28	VDD	Low−Side Bias Voltage for IC and IGBTs Driving
29	VSS	Low−Side Common Supply Ground

NOTE: Pins 3, 4, 7, 8, 11, 12, 14 and 15 are not present.

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