AP0102AT Watchdog Error Handling and Recovery

AND9915/D

Monitoring

The AP0102 provides the operational status of the system in following fw variable:

0×8016 MON_WATCHDOG_STATUS [8:0]

The expected value is 0x0000. This variable is updated by firmware every 200 ms.

NOTE: The expected value and actual bit mask is depending on the system use case and configuration. Please discuss this with your **onsemi** representative.

Error Handling

In case of 08x016 MON_WATCHDOG_STATUS != 0 following procedure is recommended:

1. Hard Reset AP0102:
   It is recommended to do at least one reset cycle to recover from a sporadic failure. There is no time requirement before hard reset. Please refer to AP0102AT−D data−sheet for hard reset operation requirements including time before first I^2C commands.
2. Request System State (Optional):
   Send 0x8101 get_state host command. FW will respond within 80 ms after the hard−reset. FW sets 0x0040 COMMAND_REGISTER [15] is set to 0 when it is ready. The maximum time delay for the FW to boot up and to be able to answer to host commands is 10 ms. If the flash−config enables streaming automatically, the system will output images as per the configuration (normal use case).
3. Continue to monitor
   MON_WATCHDOG_STATUS to see if the failure is permanent or occurs again during the current camera power−cycle. The watchdog is updated every 200 ms. The first update will be available after more than 200 ms. If no other issues are reported by MON_WATCHDOG_STATUS during the active power−cycle, the reset successfully recovered the system from the failure. If another error is reported by MON_WATCHDOG_STATUS during the same power−cycle another reset cycle is recommended. The number of resets should be limited by a counter to avoid continuous resets. The minimum time between two hard reset cycles in this context is determined by the watchdog update interval of 200 ms. The host should only attempt another reset if MON_WATCHDOG_STATUS reports another error since the last reset. The minimum time is >200 ms (first update of watchdog), the maximum time is indeterminate.
4. If the reset counter for the active power−cycle reaches its limit, it should be assumed that the failure is permanent which can result in bad configuration or a hardware failure.
5. Store Chip Debug Information:
   0x8016 MON_WATCHDOG_STATUS[7:1]
   0x001C MCU_INFO_CODE[15:8]
   0x0060 ERRORS[7:0]
   MON_WATCHDOG_FAILURE_CODE_2[4:0]
   Store System Debug Information:
   Temperature, system state, latest action of host processor (e.g. STE or OVL load). Please provide debug information to **onsemi** representative.

ADDITIONAL INFORMATION

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