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PFC Converter + 3-phase Inverter IPM Application Note Using the NFCS1060L3TT

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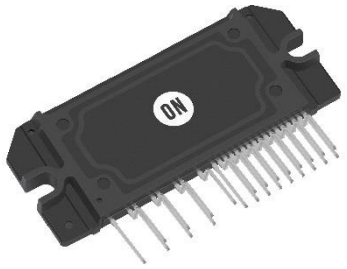
APPLICATION NOTE



Introduction

This application note provides practical guidelines for designing with the NFCS1060L3TT.

The NFCS1060L3TT is a fully−integrated PFC and inverter power stage consisting of a high−voltage driver, six motor drive IGBT's, one PFC SJ−MOSFET, one PFC SiC−SBD for rectifier and a thermistor, suitable for driving permanent magnet synchronous (PMSM) motors, brushless−DC (BLDC) motors and AC asynchronous motors. It uses ON Semiconductor's Insulated Metal Substrate (IMS) Technology.

Key Functions

- Highly Integrated Power Module Containing a Single Boost PFC Stage and Inverter power Stage for a High Voltage 3−phase Inverter in a Single In−line (SIP) Package
- Single Boost PFC Stage is Capable of High Carrier Switching over 100 MHz by Consisting of SiC−SBD and SJ−MOSFET
- Output Stage uses IGBT/FRD Technology and Implements Under Voltage Protection (UVP) and Over Current Protection (OCP) with a Fault Detection Output Flag. Internal Bootstrap Diodes are Provided for the High−side Drivers
- Separate Pins for Each of the Three Low−side Emitter Terminals
- Thermistor for Substrate Temperature Measurement
- All Control Inputs and Status Outputs have Voltage Levels Compatible with Microcontrollers
- Single VDD Power Supply Due to Internal Bootstrap Circuit for high−side Gate Driver Circuit
- Mounting Holes for Easy Assembly of Heat Sink with Screws

A simplified block diagram of a motor control system is shown in Figure 1.

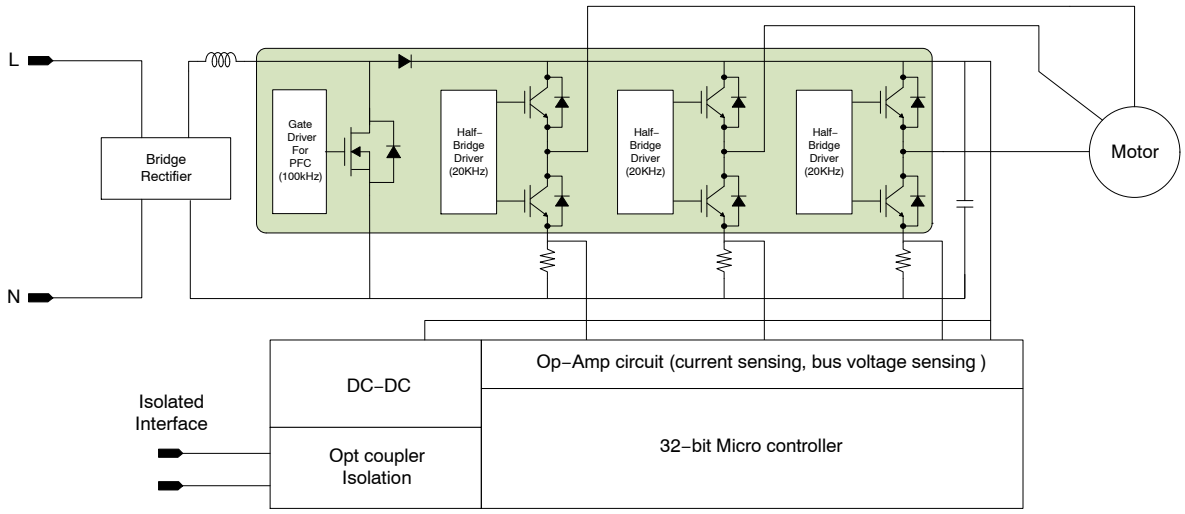


Figure 1. Motor Control System Block Diagram

PRODUCT DESCRIPTION

Table 1 gives an overview of the device. For package drawing, please refer to Chapter Package Outline.

Table 1. DEVICE OVERVIEW

Device	NFCS1060L3TT
Package	SIP35 56x25.8 / SIP2A−2 − Vertical Pins
Voltage (V_{CEmax})	600 V
Current (Ic)	10 A
Peak Current (Ic)	20 A
Isolation Voltage	2000 V
Input Logic	High−active
Shunt Resistor	Triple Shunts / External

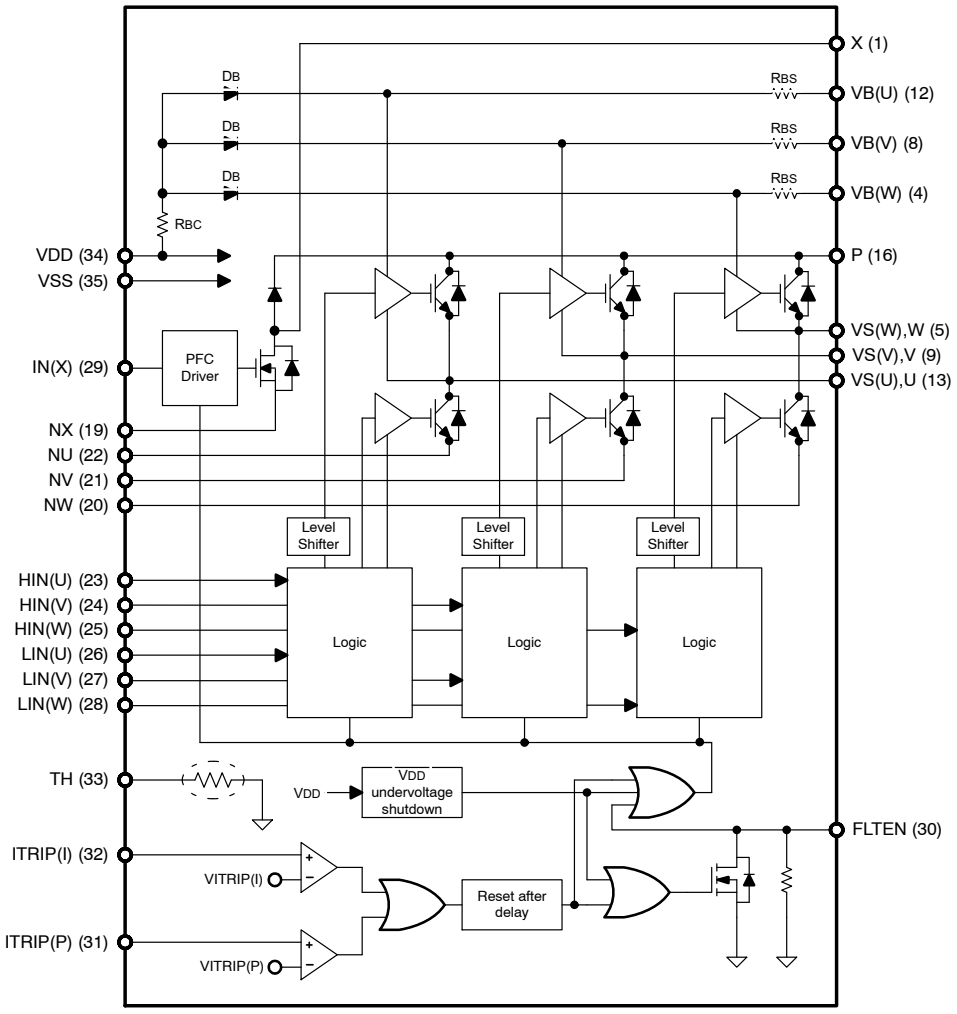


Figure 2. Internal Block Diagram

Three bootstrap circuits generate the voltage needed for driving the high−side IGBTs. The boost diodes are internal to the part and sourced from VDD (15 V). There is an internal level shift circuit for the high−side drive signals allowing all control signals to be driven directly from GND levels common with the control circuit such as the microcontroller without requiring external isolation with opt couplers.

PERFORMANCE TEST GUIDELINES

The methods used to test some datasheet parameters are shown in Figures 3 to 8.

Switching Time Definition and Performance Test Method

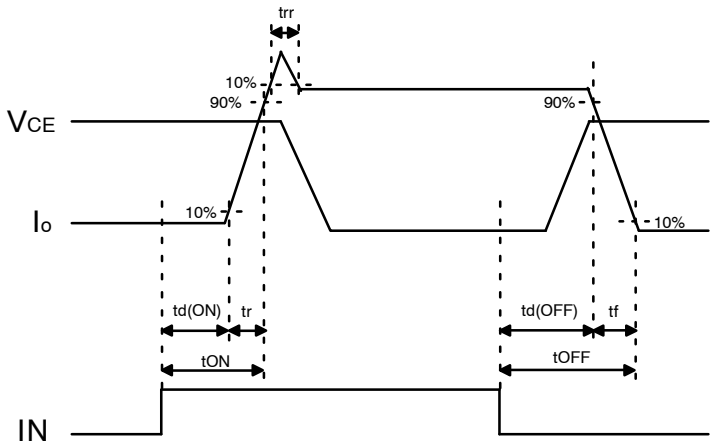


Figure 3. Switching Time Definition

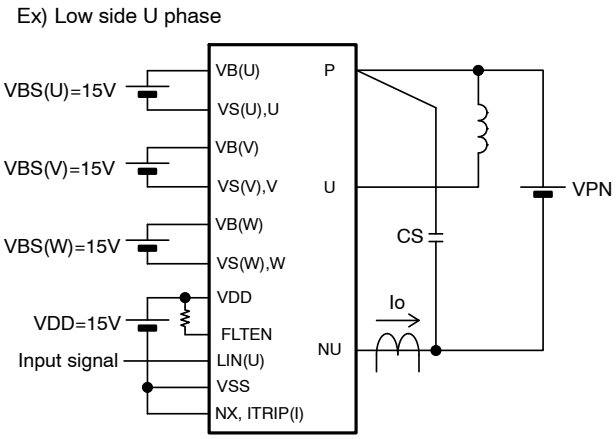


Figure 4. Evaluation Circuit (Inductive load)

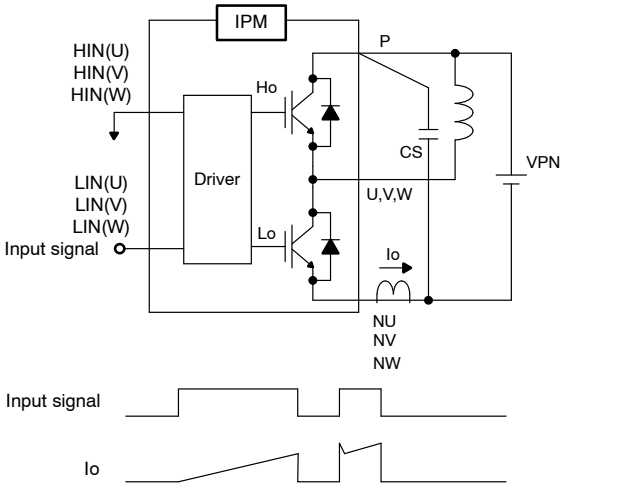


Figure 5. Switching Loss Measurement Circuit (INV)

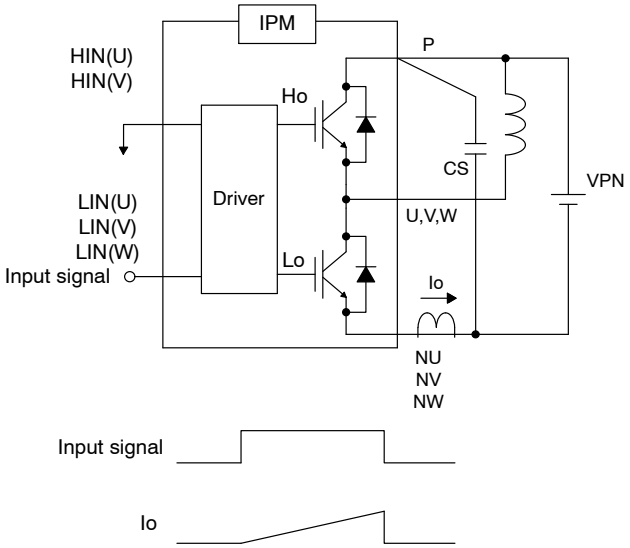


Figure 6. Reverse Bias Safe Operating Area Measurement Circuit

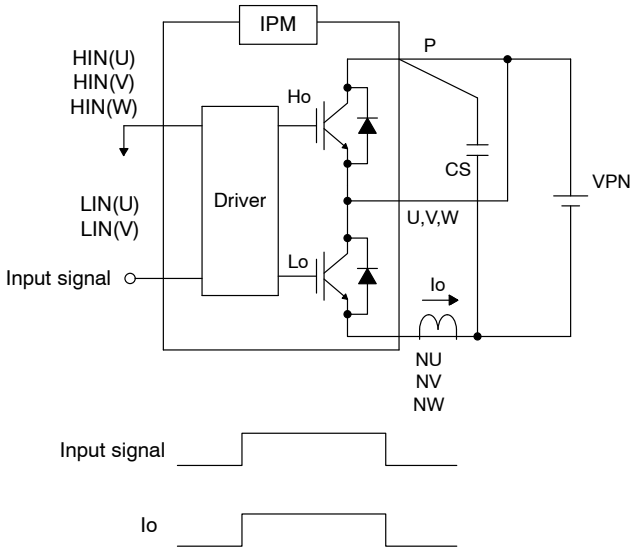


Figure 7. Short Circuit Safe Operating Area Measurement Circuit

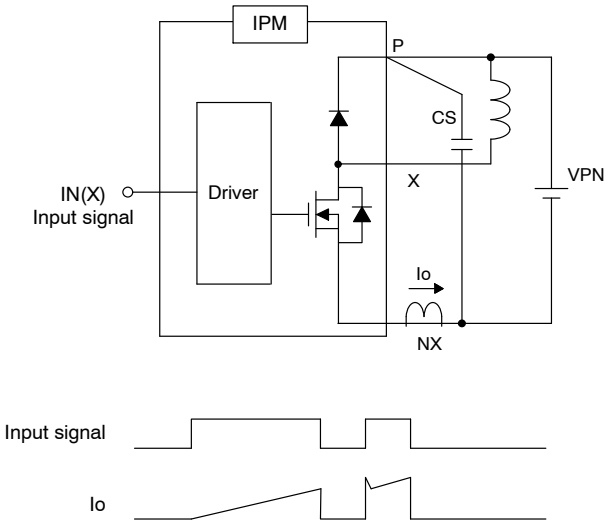


Figure 8. Switching Loss Measurement Circuit (PFC)

Thermistor Characteristics

The TH and VSS pins are connected to a thermistor mounted on the module substrate. The thermistor is used to sense the internal substrate temperature. It has the following characteristics

Table 2. NTC THERMISTOR SPECIFICATION

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resistance	R_{25}	Tc = 25°C	44.65	47	49.35	kΩ
	R_{125}	Tc = 125°C	1.29	1.41	1.53	kΩ
B−Constant (25−50°C)	–	B	4009.5	4050	4090.5	K
Temperature Range	–	–	−40	–	+125	°C

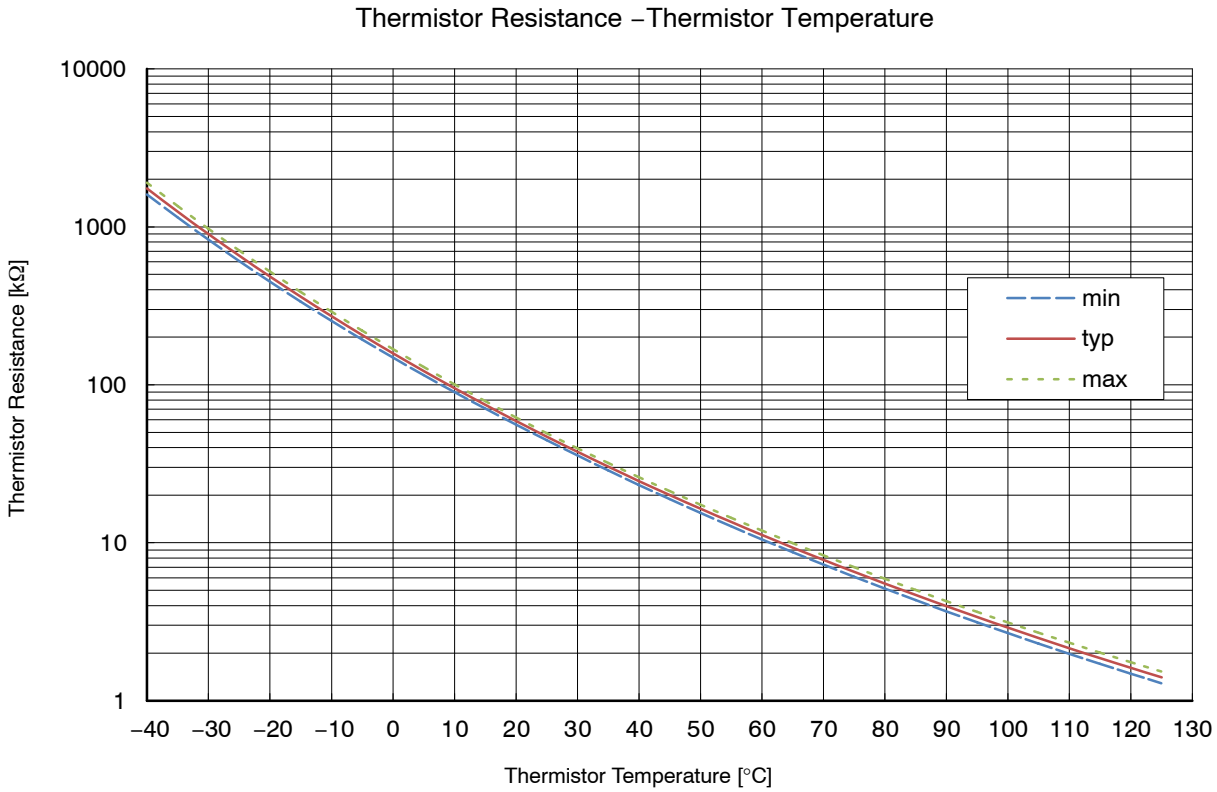


Figure 9. NTC Thermistor Resistance versus Temperature

Table 3. NTC THERMISTOR RESISTANCE VALUES

Tc [°C]	Resistance Value [kΩ]			Tc [°C]	Resistance Value [kΩ]			Tc [°C]	Resistance Value [kΩ]		
Tc [°C]	Min	Typ	Max	Tc [°C]	Min	Typ	Max	Tc [°C]	Min	Typ	Max
−40	1601.551	1747.920	1902.896	16	67.412	71.256	75.131	72	6.775	7.266	7.773
−39	1496.067	1631.671	1775.118	17	64.326	67.962	71.624	73	6.540	7.016	7.508
−38	1398.253	1523.950	1656.795	18	61.399	64.839	68.300	74	6.313	6.776	7.253
−37	1307.502	1424.076	1547.165	19	58.621	61.876	65.149	75	6.096	6.544	7.008
−36	1223.258	1331.424	1445.533	20	55.983	59.065	62.160	76	5.887	6.323	6.773
−35	1145.012	1245.428	1351.263	21	53.479	56.396	59.324	77	5.687	6.110	6.547
−34	1072.298	1165.564	1263.775	22	51.100	53.863	56.633	78	5.494	5.905	6.330
−33	1004.689	1091.357	1182.537	23	48.840	51.457	54.079	79	5.309	5.708	6.121
−32	941.795	1022.370	1107.063	24	46.692	49.172	51.654	80	5.131	5.518	5.919

Table 3. NTC THERMISTOR RESISTANCE VALUES (continued)

Tc [°C]	Resistance Value [kΩ]			Tc [°C]	Resistance Value [kΩ]			Tc [°C]	Resistance Value [kΩ]		
Tc [°C]	Min	Typ	Max	Tc [°C]	Min	Typ	Max	Tc [°C]	Min	Typ	Max
−31	883.257	958.202	1036.907	25	44.650	47.000	49.350	81	4.960	5.336	5.726
−30	828.744	898.485	971.660	26	42.670	44.936	47.204	82	4.796	5.161	5.540
−29	777.955	842.884	910.948	27	40.789	42.974	45.163	83	4.637	4.992	5.361
−28	730.613	791.088	854.428	28	39.000	41.108	43.221	84	4.485	4.830	5.188
−27	686.460	742.813	801.783	29	37.299	39.332	41.373	85	4.339	4.674	5.022
−26	645.263	697.798	752.723	30	35.682	37.643	39.613	86	4.197	4.523	4.861
−25	606.806	655.802	706.983	31	34.143	36.035	37.938	87	4.061	4.377	4.706
−24	570.888	616.605	664.317	32	32.678	34.504	36.342	88	3.929	4.237	4.557
−23	537.328	580.001	624.499	33	31.284	33.046	34.821	89	3.803	4.102	4.413
−22	505.955	545.805	587.322	34	29.956	31.657	33.372	90	3.681	3.972	4.275
−21	476.613	513.842	552.594	35	28.691	30.334	31.990	91	3.564	3.846	4.141
−20	449.159	483.954	520.140	36	27.487	29.073	30.674	92	3.451	3.725	4.012
−19	423.460	455.992	489.796	37	26.340	27.872	29.419	93	3.341	3.609	3.888
−18	399.393	429.822	461.413	38	25.247	26.726	28.221	94	3.236	3.496	3.768
−17	376.844	405.317	434.852	39	24.204	25.633	27.079	95	3.135	3.388	3.652
−16	355.709	382.362	409.985	40	23.210	24.591	25.988	96	3.038	3.284	3.541
−15	335.891	360.850	386.695	41	22.262	23.596	24.947	97	2.944	3.183	3.433
−14	317.299	340.680	364.871	42	21.358	22.647	23.953	98	2.853	3.086	3.330
−13	299.850	321.762	344.413	43	20.495	21.740	23.004	99	2.766	2.992	3.230
−12	283.468	304.011	325.227	44	19.671	20.875	22.097	100	2.681	2.902	3.133
−11	268.081	287.347	307.226	45	18.884	20.048	21.230	101	2.600	2.815	3.040
−10	253.623	271.697	290.332	46	18.133	19.258	20.402	102	2.521	2.730	2.950
−9	240.032	256.995	274.468	47	17.415	18.503	19.610	103	2.445	2.649	2.863
−8	227.251	243.176	259.566	48	16.729	17.782	18.853	104	2.372	2.570	2.778
−7	215.228	230.184	245.563	49	16.074	17.092	18.129	105	2.301	2.494	2.697
−6	203.912	217.963	232.399	50	15.448	16.433	17.436	106	2.232	2.421	2.618
−5	193.259	206.463	220.019	51	14.849	15.802	16.774	107	2.166	2.349	2.542
−4	183.212	195.624	208.356	52	14.276	15.198	16.139	108	2.102	2.281	2.468
−3	173.747	185.419	197.381	53	13.728	14.621	15.532	109	2.040	2.214	2.397
−2	164.828	175.808	187.049	54	13.204	14.068	14.950	110	1.980	2.150	2.328
−1	156.420	166.751	177.320	55	12.703	13.539	14.394	111	1.923	2.088	2.261
0	148.490	158.214	168.154	56	12.222	13.032	13.860	112	1.867	2.028	2.197
1	141.009	150.165	159.516	57	11.763	12.547	13.349	113	1.813	1.970	2.135
2	133.949	142.573	151.372	58	11.323	12.082	12.859	114	1.761	1.914	2.075
3	127.284	135.408	143.691	59	10.901	11.636	12.390	115	1.711	1.860	2.017
4	120.989	128.645	136.445	60	10.497	11.209	11.940	116	1.662	1.808	1.961
5	115.041	122.259	129.606	61	10.111	10.801	11.509	117	1.615	1.757	1.907
6	109.421	116.227	123.149	62	9.741	10.409	11.096	118	1.570	1.708	1.854
7	104.107	110.528	117.051	63	9.386	10.034	10.699	119	1.526	1.661	1.803
8	99.082	105.140	111.289	64	9.046	9.673	10.319	120	1.484	1.615	1.754
9	94.328	100.045	105.844	65	8.719	9.328	9.954	121	1.442	1.571	1.706
10	89.829	95.227	100.697	66	8.406	8.996	9.604	122	1.402	1.528	1.660
11	85.570	90.667	95.828	67	8.106	8.678	9.267	123	1.364	1.486	1.615
12	81.537	86.352	91.223	68	7.818	8.373	8.944	124	1.326	1.445	1.571
13	77.717	82.266	86.864	69	7.542	8.080	8.634	125	1.290	1.406	1.529
14	74.097	78.396	82.738	70	7.276	7.798	8.336				
15	70.665	74.730	78.831	71	7.021	7.527	8.049				

PROTECTION FUNCTIONS

This chapter describes the protection functions.

- Over−current protection
- Short circuit protection
- Under voltage lockout (UVLO) protection
- Cross conduction prevention

Over−current protection (OCP)

The NFCS1060L3TT module uses an external shunt resistor for the OCP functionality. As shown in Figure 10 the emitters of all three low−side IGBTs are brought out to module pins. The external OCP circuit consists of a shunt resistor and a RC filter network. If the application uses three separate shunts, an op−amp circuit is used to monitor the three separate shunts and provide an over-current signal.

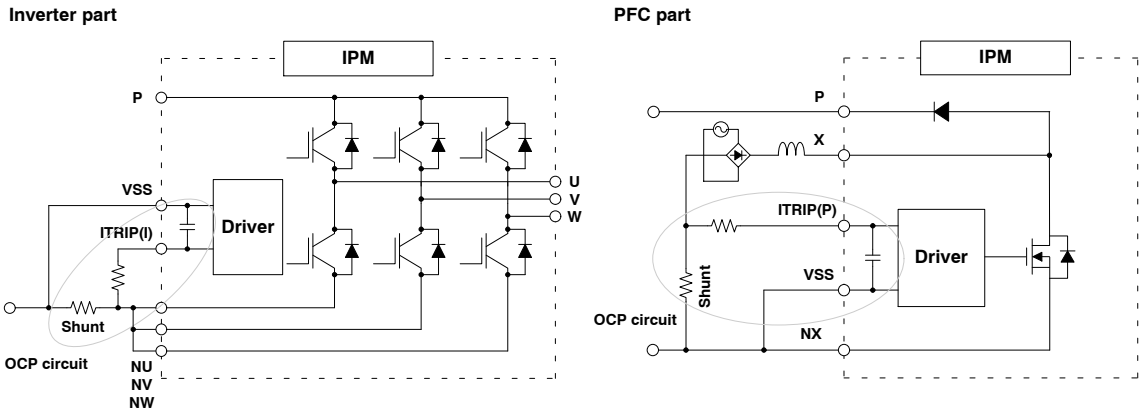


Figure 10. Over−current Protection Circuit

The OCP function is implemented by comparing the ITRIP(I) and ITRIP(P) input voltages with an internal reference voltage of 0.49 V (typ) for inverter part and −0.31 V (typ) for PFC part. If the absolute value of the voltage on either terminal exceeds the trip levels, an OCP fault is triggered. For single shunt applications, this voltage is the same as the voltage across the respective shunt resistors.

NOTE: The current value of the OCP needs to be set by correctly sizing the external shunt resistor to be less than the module's maximum current rating.

When an OCP fault is detected, all internal gate drive signals for the IGBTs become inactive and the fault signal output is activated. The FLTEN signal has an open drain output, so when there is a fault, the output is pulled low.

A RC filter is used on the ITRIP(I) and ITRIP(P) inputs to prevent an erroneous OCP detection due to normal switching noise or recovery diode current. The time constant of the RC filter should be set to a value between 1.5 μ to 2 μs. In any case the time constant must be shorter than the IGBTs short current safe operating area (SCSOA). Please refer to data sheet for SCSOA. The resulting OCP level due to the filter time constant is shown in Figure 11.

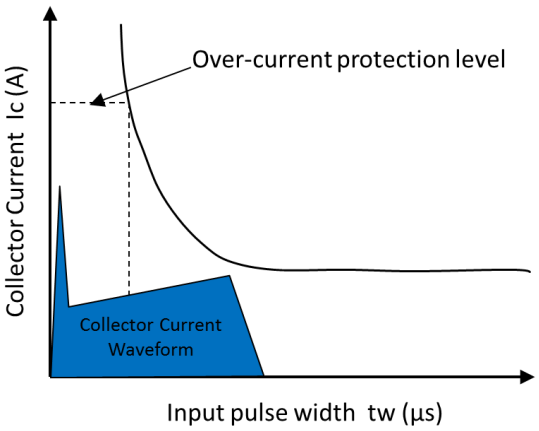


Figure 11. Filter Time Constant

For optimal performance all traces around the shunt resistor need to be kept as short as possible.

Figure 12 shows the sequence of events in case of an OCP event.

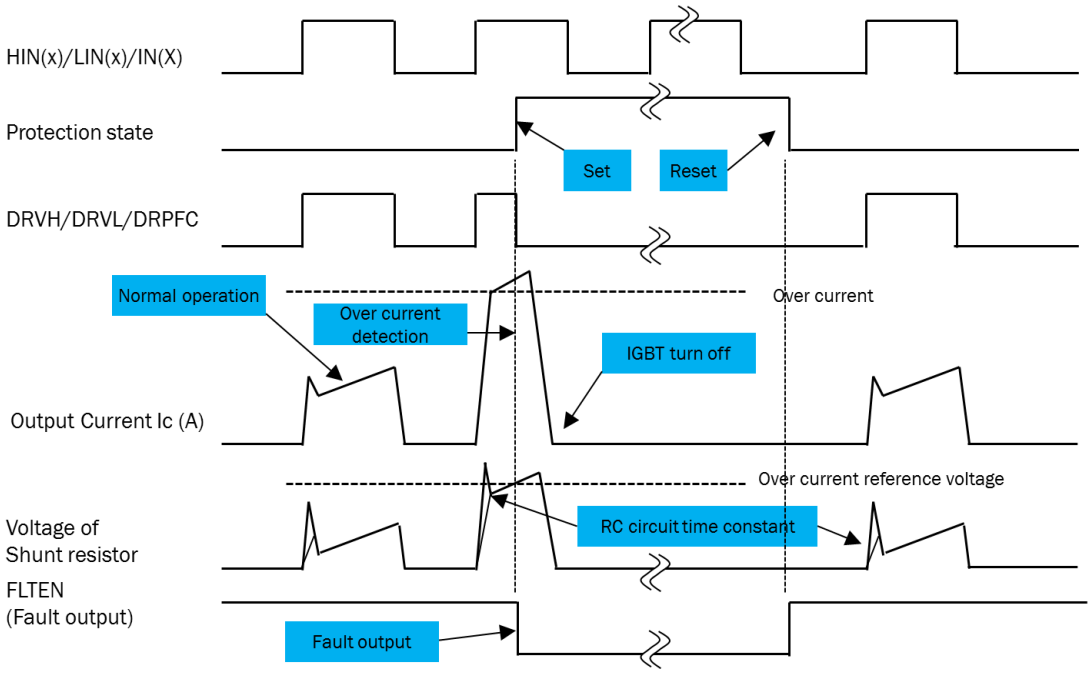


Figure 12. Over−current Protection Timing Diagram

Under Voltage Lockout Protection

The UVLO protection is designed to prevent unexpected operating behavior as described in Table 4. Both High−side and Low−side have under voltage protection. The low−side UVLO condition is indicated on the FLTEN output. During the low−side UVLO state the FLTEN output is continuously driven low. A high−side UVLO condition is not indicated on the FLTEN output.

Table 4. MODULE OPERATION ACCORDING TO VDD VOLTAGE

VDD Voltage (Typ. Value)	Operation Behavior
<12.5 V	As the voltage is lower than the UVLO threshold the control circuit is not fully turned on. A perfect functionality cannot be guaranteed
12.5 V – 14.0 V	IGBTs can work, however conduction and switching losses increase due to low voltage gate signal
14.0 V – 16.5 V	Recommended conditions
16.5 V – 20.0 V	IGBTs can work. Switching speed is faster and saturation current higher, increasing short−circuit broken risk
>20.0 V	Control circuit is destroyed. Absolute max. Rating is 20 V

The sequence of events in case of a low−side UVLO event (IGBTs turned off and active fault output) is shown in Figure 13 Figure 14 shows the same for a high−side UVLO (IGBTs turned off and no fault output).

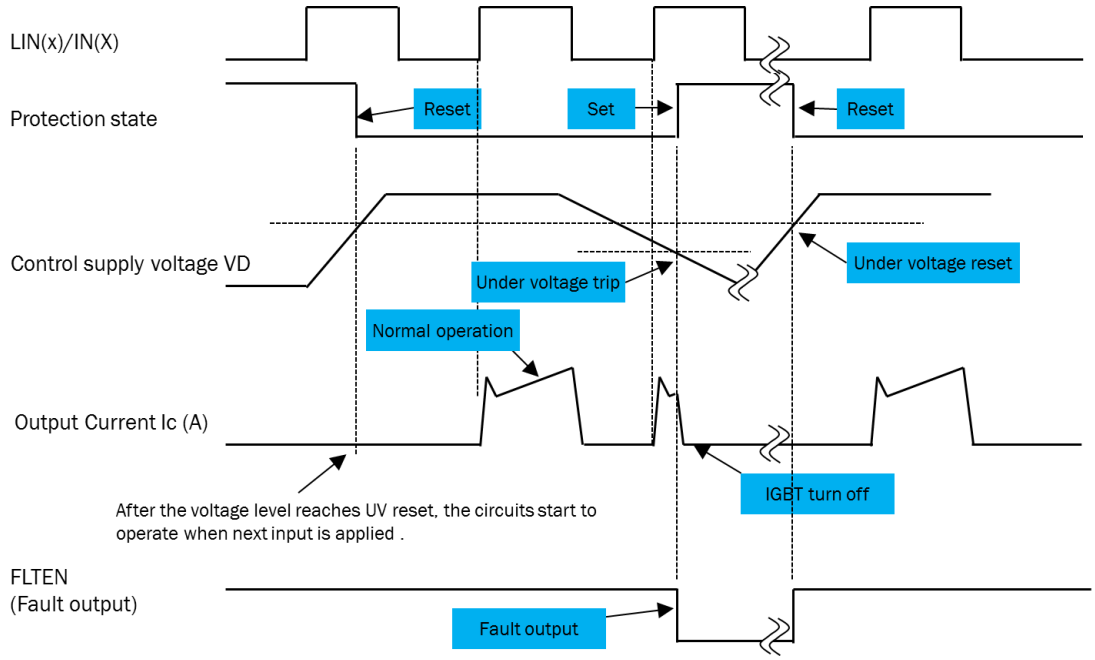


Figure 13. Low−side UVLO Timing Diagram

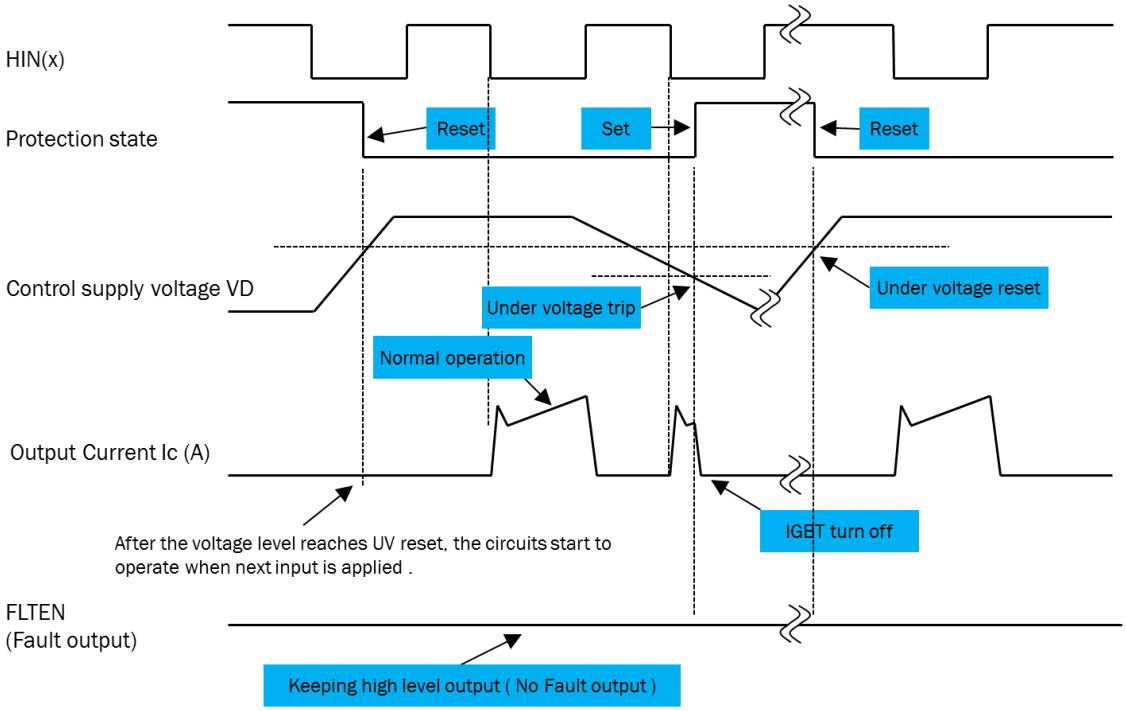


Figure 14. High−side UVLO Timing Diagram

Cross−conduction Prevention

The NFCS1060L3TT module implements cross−conduction prevention logic at the gate driver to avoid simultaneous drive of the low−side and high−side IGBTs as shown in Figure 15.

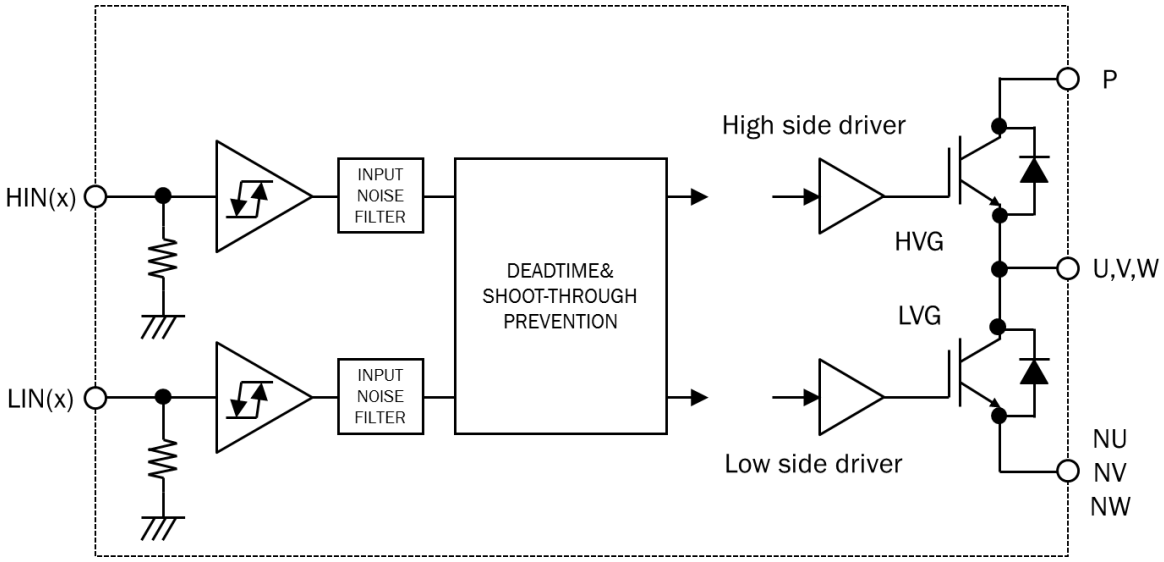


Figure 15. Cross−conduction Prevention

If both high−side and low−side drive inputs are active (HIGH) the logic prevents both gates from being driven as shown in Figure 16 below.

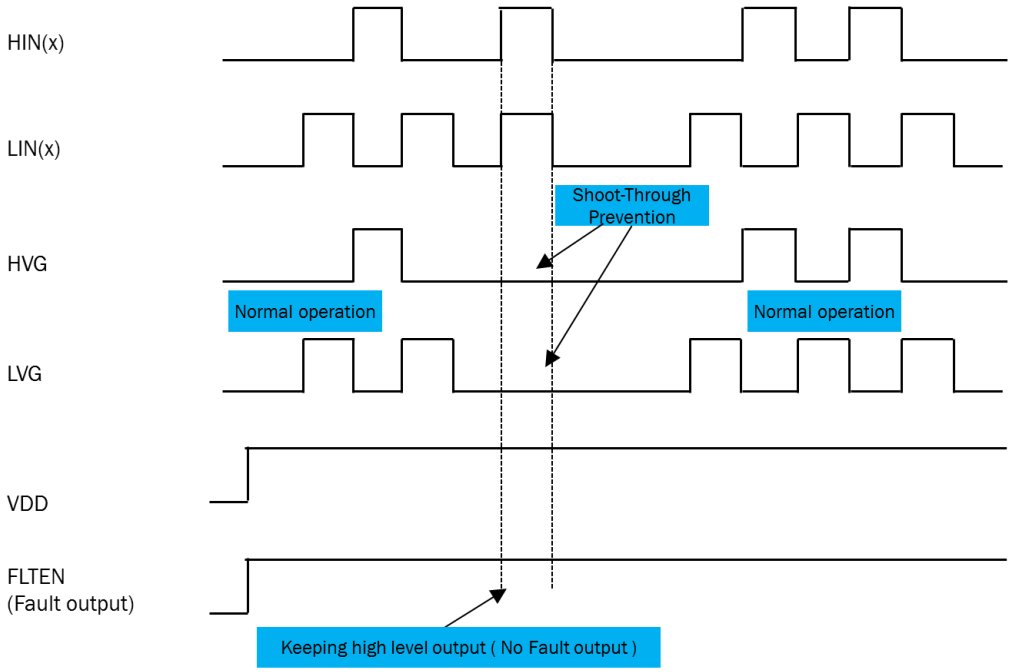


Figure 16. Cross−conduction Prevention Timing Diagram

Even if cross−conduction on the IGBTs due to incorrect external driving signals is prevented by the circuitry, the driving signals (HIN(x) and LIN(x)) need to include a “dead time”. This period where both inputs are inactive between either one becoming active is required due to the internal delays within the IGBTs.

Figure 17 shows the delay from the HIN−input via the internal high−side gate driver to high−side IGBT, the delay from the LIN−input via the internal low−side gate driver to low−side IGBT and the resulting minimum dead time which is equal to the potential shoot through period:

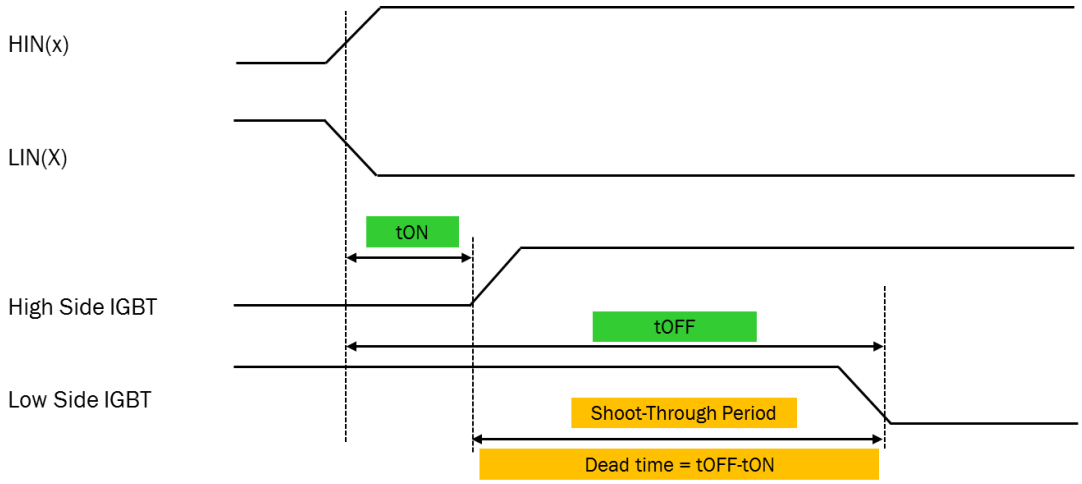


Figure 17. Shoot−through Period

PCB DESIGN AND MOUNTING GUIDELINES

This chapter provides guidelines for an optimized design and PCB layout as well as module mounting recommendations to appropriately handle and assemble the IPM.

Application (Schematic) Design

Figure 18 gives an overview of the external components and circuits.

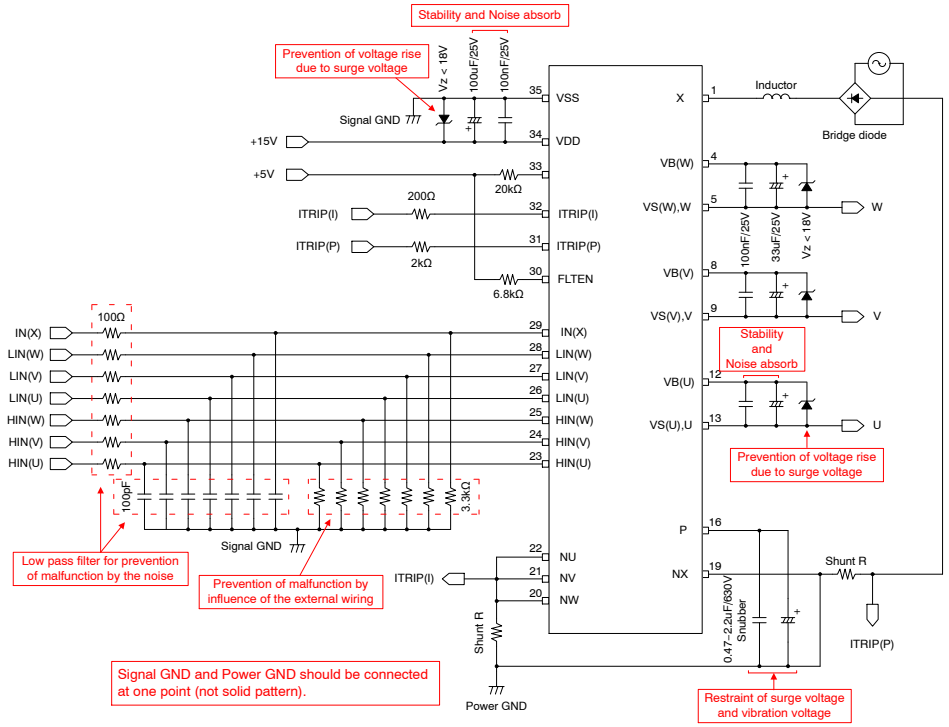


Figure 18. Application Circuit

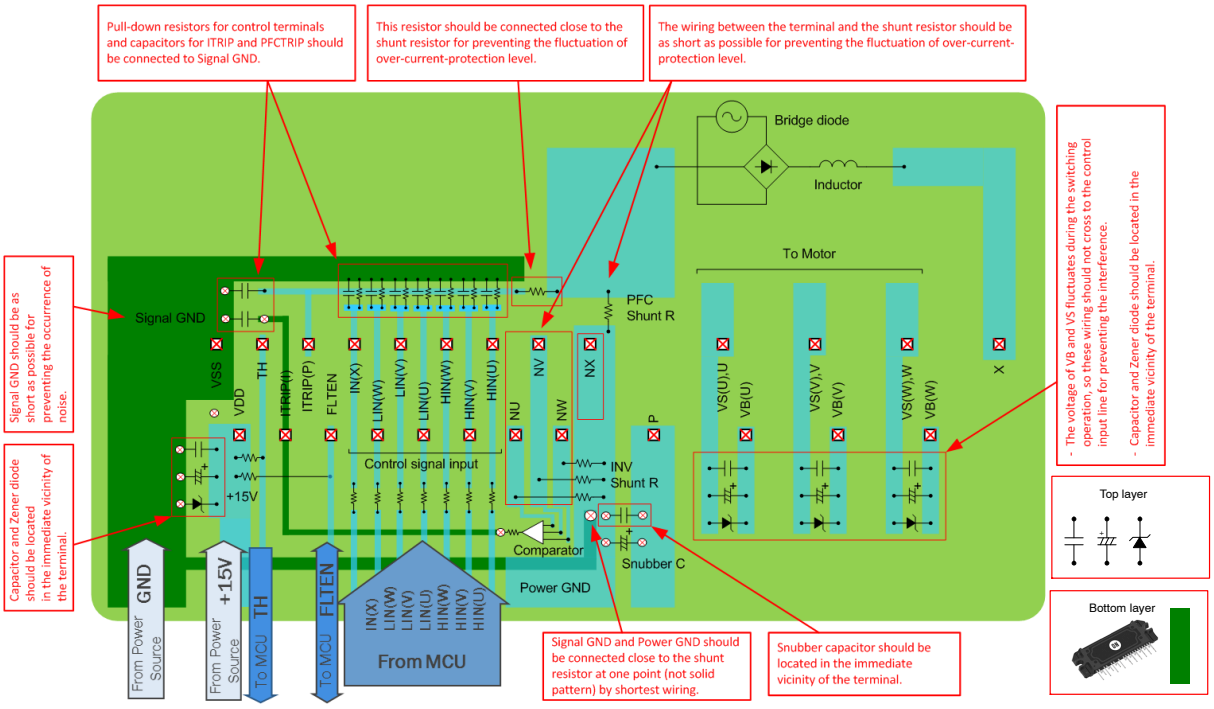


Figure 19. NFCS1060L3TT RecommenDed layout

Pin by Pin Design and Usage Notes

This section provides pin by pin PCB layout recommendations and usage notes. A complete list of module pins is given in Chapter Package Outline.

P
NU
NV
NW

DC Power supply terminal for the inverter block. Voltage spikes could be caused by longer traces to these terminals due to the trace inductance, therefore traces are recommended to be as short as possible. In addition a snubber capacitor should be connected as close as possible to the VP terminal to stabilize the voltage and absorb voltage surges.

NX

This pin is connected to the emitter of the PFC boost IGBT.

X

This is the connection for the switched end of the boost inductor. This pin is connected to the collector of the PFC IGBT and the anode of the PFC rectifier. The other end of the boost inductor is connected to the rectified AC mains input.

VS(U),U
VS(V),V
VS(W),W

These are the output pins for connecting the 3−phase motor. They share the same GND potential with each of the high−side control power supplies. Therefore they are also used to connect the GND of the bootstrap capacitors. These bootstrap capacitors should be placed as close to the module as possible.

VDD
VSS

These pins provide power to the low−side gate drivers, the protection circuits and the bootstrap circuits. The voltage between these terminals is monitored by the UVLO circuit. The VSS terminal is the reference voltage for the input control signals.

VB(U)
VB(V)
VB(W)

The VB(x) pins are internally connected to the positive supply of the high−side drivers. The supply needs to be floating and electrically isolated. The bootstrap circuit shown in Figure 20 forms this power supply individually for every phase. Due to integrated boot resistor and diode (RB & DB) only an external boot capacitor (CB) is required.

CB is charged when the following conditions are met.

Motor terminal voltage is low level for low side IGBT or low side diode conducting

The capacitor is discharged while the high−side driver is activated.

Thus CB needs to be selected taking the maximum on time of the high−side and the switching frequency into account.

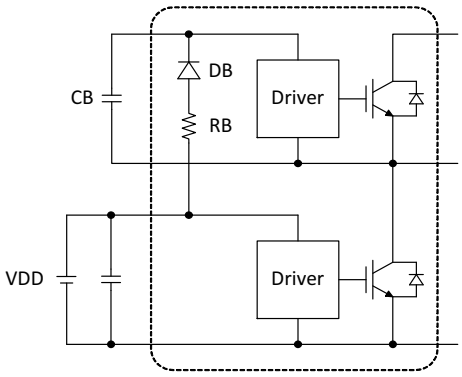


Figure 20. Bootstrap Circuit

The voltages on the high-side drivers are individually monitored by the under voltage protection circuit. If there is a UVLO fault on any given phase, the output on that phase is disabled.

Typically a CB value of less or equal 47 μF (±20%) is used. If the CB value needs to be higher, an external resistor (20 Ω or less) should be used in series with the capacitor to avoid high currents which can cause malfunction of the IPM.

HIN(U)
HIN(V)
HIN(W)
LIN(U)
LIN(V)
LIN(W)

These pins are the control inputs for the power stages. The inputs on HIN(U)/HIN(V)/HIN(W) control the high−side transistors of U/V/W, the inputs on LIN(U)/LIN(V)/LIN(W) control the low−side transistors of U/V/W, and the input on IN(X) controls the transistors of PFC respectively. The input logic is active HIGH. An external microcontroller can directly drive these inputs without need for isolation.

IN(X)

Simultaneous activation of both low−side and high−side is prevented internally to avoid shoot−through at the power stage. However, due to IGBT switching delays the control signals must include a dead−time.

The equivalent input stage circuit is shown in Figure 21.

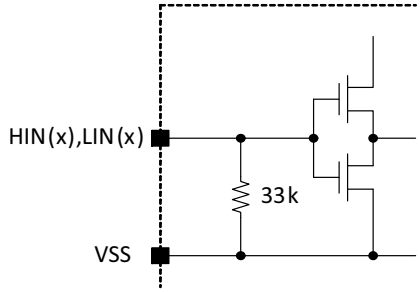


Figure 21. Internal Input Circuit

For fail safe operation the control inputs are internally tied to GND via a 33 kΩ (typ) resistor. An additional external low−ohmic pull−down resistor with a value of 2.2 kΩ−3.3kΩ is recommended to prevent erroneous switching caused by noise induced in the wiring. The output might not respond when the width of the input pulse is less than 1 μs (both ON and OFF).

FLTEN

This pin serves both as an enable input and an active low fault output (open−drain). It is used to indicate an internal fault condition of the module and also can be used to disable the module operation. The gate driver operates when the voltage of this pin is at 2.5 V or more, and stops at 0.8 V or less. The I/O structure is shown in Figure 22.

The internal sink current IoSD during an active fault is nominal 2 mA @ 0.1 V. Depending on the interface supply voltage the external pull−up resistor (RP) needs to be selected as shown below.

For the commonly used supplies :

Pull up voltage = 15 V → RP ≥ 20 kΩ
Pull up voltage = 5 V → RP ≥ 6.8 kΩ
Pull up voltage = 3.3 V → RP ≥ 3.9 kΩ

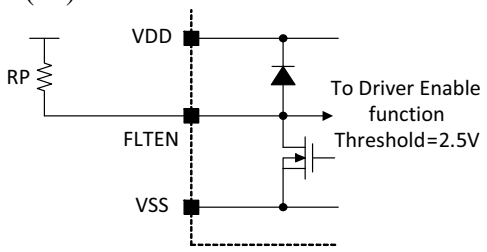


Figure 22. FLTEN Connection

For a detailed description of the fault operation refer to Chapter Protection Function.

Note: The Fault signal does not permanently latch. After the protection event ended and the fault clear time (min. 1 ms) passed, the module's operation is automatically re−started. Therefore the input needs to be driven low externally as soon as a fault is detected.

ITRIP(I)
ITRIP(P)

These pins are used to enable an OCP function. The ITRIP(I) is for inverter part, the ITRIP(P) is for PFC part. When the voltage of these pins exceeds a reference voltage, the OCP function operates. For details of the OCP operation refer to Chapter Protection Function.

TH An internal thermistor to sense the substrate temperature is connected between TH and VSS. By connecting an external pull−up resistor and measuring the midpoint voltage, the module temperature can be monitored. Please refer to heading Chapter Thermistor Characteristics for details of the thermistor.

Note: This is the only means to monitor the substrate temperature indirectly.

Heat Sink Mounting and Torque

If a heat sink is used, insufficiently secure or inappropriate mounting can lead to a failure of the heat sink to dissipate heat adequately.

The following general points should be observed when mounting IPM on a heat sink:

1. Verify the following points related to the heat sink:
   - There must be no burrs on aluminum or copper heat sinks
   - Screw holes must be countersunk
   - There must be no unevenness in the heat sink surface that contacts IPM
   - There must be no contamination on the heat sink surface that contacts IPM
2. Highly thermal conductive silicone grease needs to be applied to the whole back (aluminum substrate side) uniformly, and mount IPM on a heat sink. If the device is removed, grease must be applied again
3. For a good contact between the IPM and the heat sink, the mounting screws should be tightened gradually and sequentially while a left/right balance in pressure is maintained. Either a bind head screw or a truss head screw is recommended. Please do not use tapping screw. We recommend using a flat washer in order to prevent slack

The standard heat sink mounting condition of the NFCS1060L3TT is as follows.

Table 5. HEAT SINK MOUNTING

Item	Recommended Condition
Pitch	56.0±0.1 mm (Please refer to Package Outline Diagram)
Screw	Diameter: M3 Screw head types: pan head, truss head, binding head
Washer	Plane washer The size is D: 7 mm, d: 3.2 mm and t: 0.5 mm JIS B 1256
Heat sink	Material: Aluminum or Copper Warpage (the surface that contacts IPM): −50 to 100 μm Screw holes must be countersunk. No contamination on the heat sink surface that contacts IPM.
Torque	Temporary tightening: 20 to 30 % of final tightening on first screw Temporary tightening: 20 to 30 % of final tightening on second screw Final tightening: 0.6 to 0.9 Nm on first screw Final tightening: 0.6 to 0.9 Nm on second screw
Grease	Silicone grease. Thickness: 100 to 200 μm Uniformly apply silicone grease to whole back. Thermal foils are only recommended after careful evaluation. Thickness, stiffness and compressibility parameters have a strong Influence on performance.

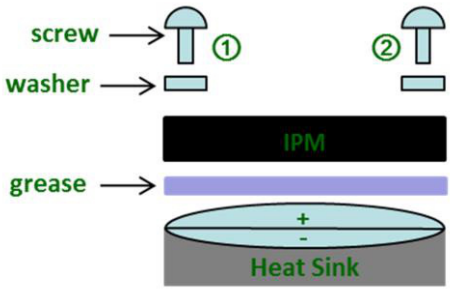


Figure 23. Mount IPM on a Heat Sink

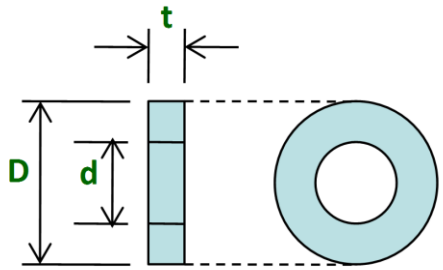


Figure 24. Size of Washer

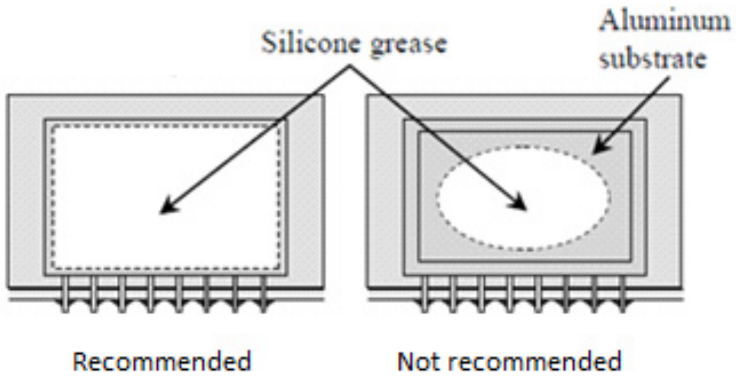


Figure 25. Uniform Application of Grease Recommended

Steps to mount an IPM on a heat sink
1st: Temporarily tighten maintaining a left/right balance.
2nd : Finally tighten maintaining a left/right balance.

Mounting and PCB Considerations

In designs in which the PCB and the heat sink are mounted to the chassis independently, use a mechanical design which avoids a gap between IPM and the heat sink, or which avoids stress to the lead frame of IPM by an assembly that slipping IPM is forcibly fixed to the heat sink with a screw.

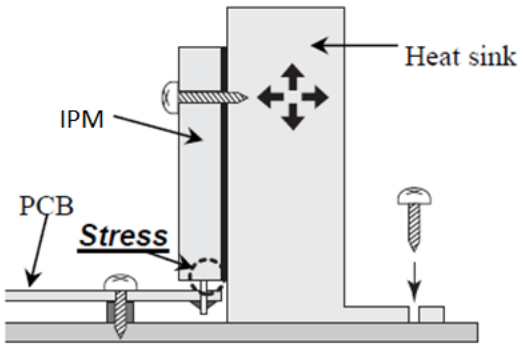


Figure 26. Fix to Heat Sink

Maintain a separation distance of at least 1.5 mm between the IPM case and the PCB. In particular, avoid mounting techniques in which the IPM substrate or case directly contacts the PCB. Do not mount IPM with a tilted condition for PCB. This can result in stress being applied to the lead frame and IPM substrate could short out tracks on the PCB. If stress is given by compulsory correction of a lead frame after the mounting, a lead frame may drop out.

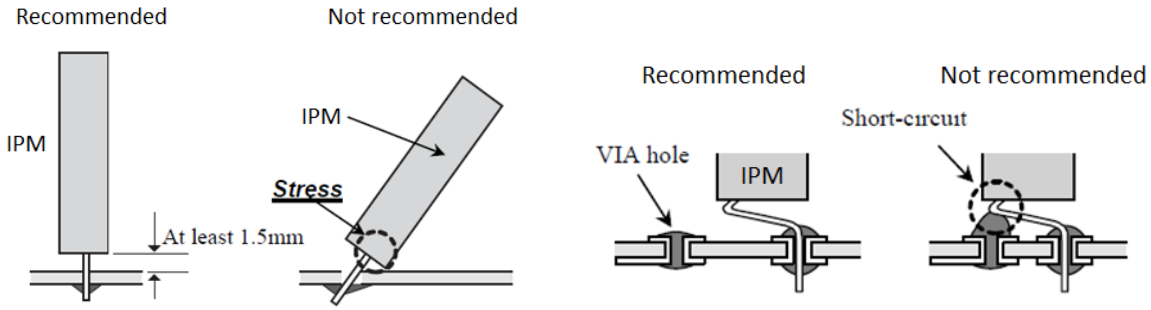


Figure 27. Mounting position on PCB

Since the use of sockets to mount IPM can result in poor contact with IPM leads, we strongly recommend making direct connections to PCB.

Since the use of sockets to mount IPM can result in poor contact with IPM leads, we strongly recommend making direct connections to PCB.IPMs are flame retardant. However, under certain conditions, it may burn, and poisonous gas may be generated or it may explode. Therefore, the mounting structure of the IPM should also be flame retard−ant.

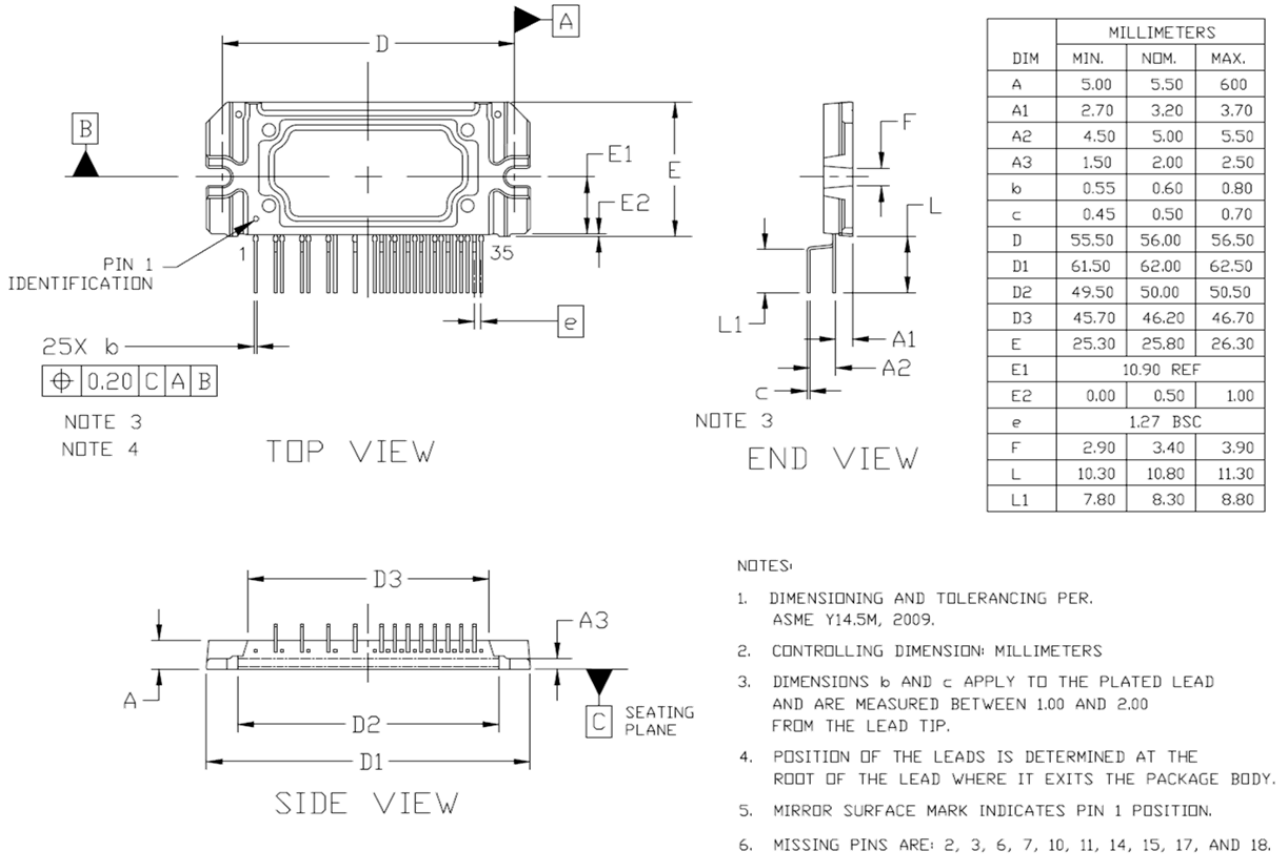
Mounting on a PCB

1. Align the lead frame with the holes in the PCB and do not use excessive force when inserting the pins into the PCB. To avoid bending the lead frames, do not try to force pins into the PCB unreasonably
2. Do not insert IPM into PCB with an incorrect orientation, i.e. be sure to prevent reverse insertion. IPMs may be destroyed or suffer a reduction in their operating lifetime by this mistake
3. Do not bend the lead frame

PACKAGE OUTLINE

The package of NFCS1060L3TT is single−inline−package.

Package Outline and Dimension



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	5.00	5.50	600
A1	2.70	3.20	3.70
A2	4.50	5.00	5.50
A3	1.50	2.00	2.50
b	0.55	0.60	0.80
c	0.45	0.50	0.70
D	55.50	56.00	56.50
D1	61.50	62.00	62.50
D2	49.50	50.00	50.50
D3	45.70	46.20	46.70
E	25.30	25.80	26.30
E1	10.90 REF		
E2	0.00	0.50	1.00
e	1.27 BSC		
F	2.90	3.40	3.90
L	10.30	10.80	11.30
L1	7.80	8.30	8.80

NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS b AND c APPLY TO THE PLATED LEAD AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP.
4. POSITION OF THE LEADS IS DETERMINED AT THE ROOT OF THE LEAD WHERE IT EXITS THE PACKAGE BODY.
5. MIRROR SURFACE MARK INDICATES PIN 1 POSITION.
6. MISSING PINS ARE: 2, 3, 6, 7, 10, 11, 14, 15, 17, AND 18.

Figure 28. Package Outline

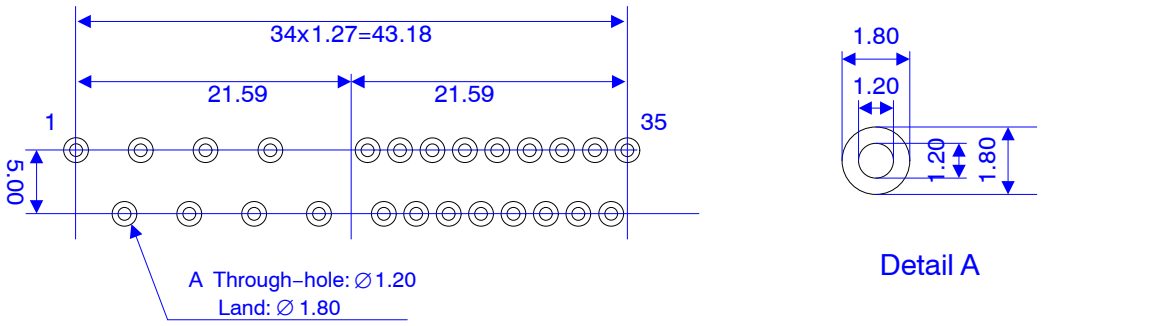


Figure 29. Recommended Land Pattern

Marking Diagram

NFCS1060L3TT = Specific Device Code
ZZZ = Assembly Lot code
A = Assembly Location
T = Test Location
Y = Year
WW = Work Week
Device marking is on package top side

PIN OUT DESCRIPTION

Pin	Name	Description
1	X	X Phase MOSFET Drain for PFC Inductor Connection
4	VB(W)	High−Side Bias Voltage for W Phase IGBT Driving
5	VS(W),W	Output for W Phase and High−Side Bias Voltage GND for W Phase IGBT Driving
8	VB(V)	High−Side Bias Voltage for V Phase IGBT Driving
9	VS(V),V	Output for V Phase and High−Side Bias Voltage GND for V Phase IGBT Driving
12	VB(U)	High−Side Bias Voltage for U Phase IGBT Driving
13	VS(U),U	Output for U Phase and High−Side Bias Voltage GND for U Phase IGBT Driving
16	P	Positive DC−Link Input / Positive PFC Output Voltage
19	NX	X Phase MOSFET Source for PFC
20	NW	Negative DC−Link Input for W Phase
21	NV	Negative DC−Link Input for V Phase
22	NU	Negative DC−Link Input for U Phase
23	HIN(U)	Signal Input for High−Side U Phase
24	HIN(V)	Signal Input for High−Side V Phase
25	HIN(W)	Signal Input for High−Side W Phase
26	LIN(U)	Signal Input for Low−Side U Phase
27	LIN(V)	Signal Input for Low−Side V Phase
28	LIN(W)	Signal Input for Low−Side W Phase
29	IN(X)	Signal Input for PFC X Phase
30	FLTEN	Fault Output / Enable
31	ITRIP(P)	Input for Over Current Protection for PFC
32	ITRIP(I)	Input for Over Current Protection for Inverter
33	TH	Thermistor Bias Voltage
34	VDD	Low−Side Bias Voltage for IC and IGBTs Driving
35	VSS	Low−Side Common Supply Ground

NOTE: Pins 2, 3, 6, 7, 10, 11, 14, 15, 17 and 18 are not present.

PUBLICATION ORDERING INFORMATION

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