3-phase Inverter Power Module 650 V SPM® 49 Series Application Note

AND9944/D

INTRODUCTION

This application note provides practical guidelines for designing with the SPM 49 Series power modules. This series of Intelligent Power Modules (IPM) for 3−phase motor drives contains a three−phase inverter stage, gate drivers and a thermistor (Optional).

Design Concept

The SPM 49 design objective is to provide a minimized package and a low power consumption module with improved reliability. This is achieved by applying new gate−driving High−Voltage Integrated Circuit (HVIC), a new Insulated−Gate Bipolar Transistor (IGBT) of advanced silicon technology, and improved Direct Bonded Copper (DBC) substrate based on transfer mold package. The SPM 49 achieves reduced board size and improved reliability compared to existing discrete solutions. Target applications are inverter motor drives for industrial use, such as commercial air conditioners, general−purpose inverters and servo motors. The temperature sensing function of SPM 49 products are implemented in the LVIC to enhance the system reliability and isolated optional thermistor is available as well. The analog voltage proportional to the temperature of the LVIC and integrated thermistor temperature in module are provided for monitoring the module temperature and necessary protections against over−temperature situations. Figure 1 shows the package outline structure.

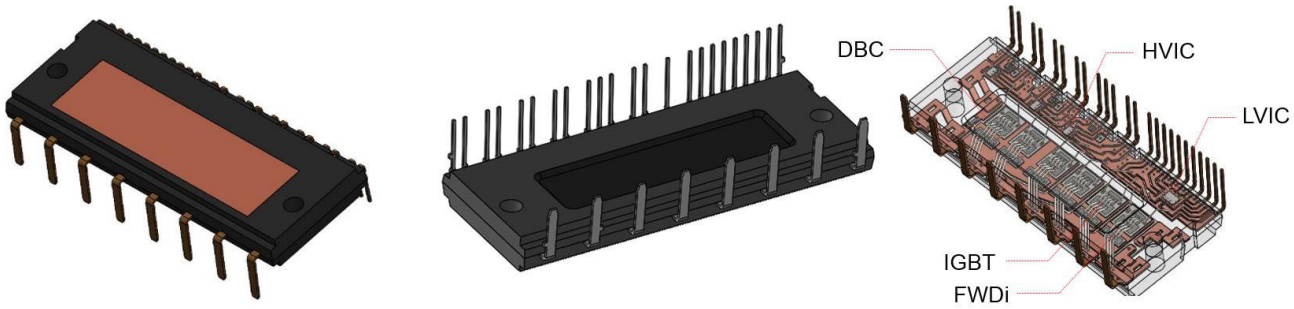


Figure 1. External View and Internal Structure of SPM 49

Key Features

- 650 V / 30, 50, 75 A, three phase IGBT inverter including control ICs for gate driving and protections
- Very low thermal resistance by adopting DBC substrate
- Easy PCB layout thanks to built−in bootstrap circuits
- Open emitter configuration for easy monitoring of each phase current sensing
- Sense IGBT technology is applied for low side to provide over current protection
- Single−grounded power supply thanks to built−in HVICs and bootstrap operations
- Built−in temperature sensing function by LVIC and optional NTC
- Isolation rating of 2500 Vrms / min

PRODUCT DESCRIPTION

Ordering Information

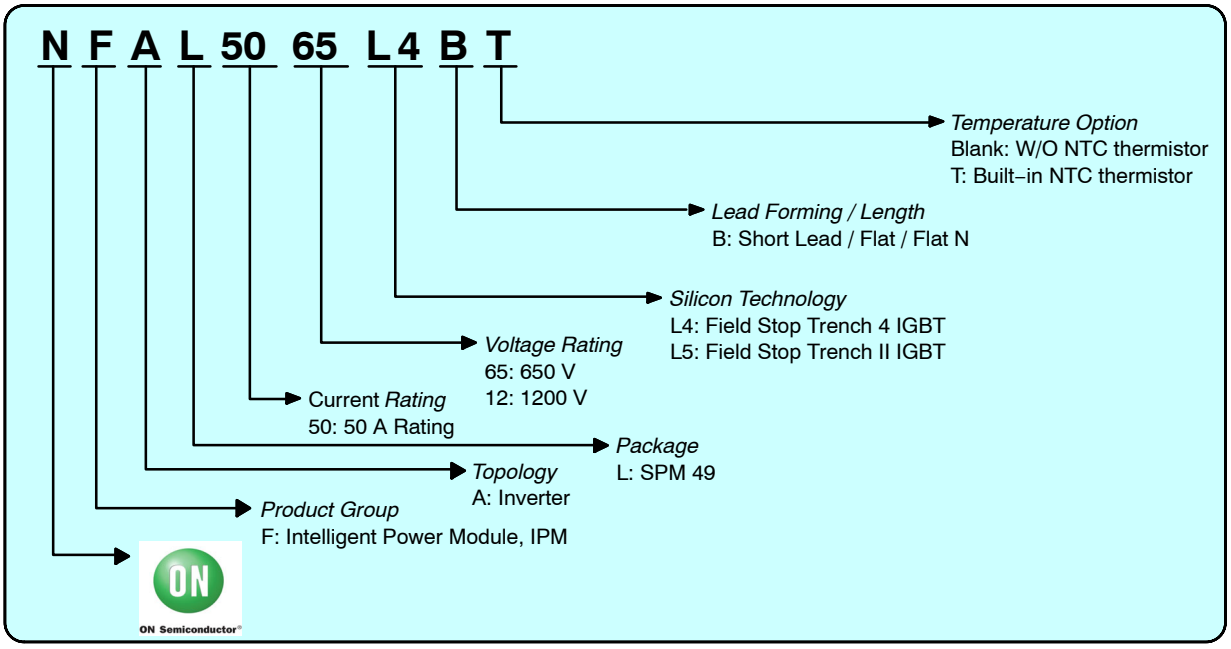


Figure 2. Ordering Information

Product Line−up

Table 1 shows the basic line up without package variations. Online loss and temperature simulation tool, Motion Control Design Tool is recommended to find out the right IPM product for the desired application. For package drawing, please refer to Chapter Package Outline.

Table 1. PRODUCT LINE−UP

Target Application	Device	IGBT Rating	Motor Rating (Note 1)	Isolation Voltage
Air Conditioners, Industrial Motor, General−purpose Inverters, Servo Motors	NFAL3065L4B(T) (Note 2)	30 A / 650 V	2.2 kW	V_{ISO} = 2500 Vrms (Sine 60 Hz, 1−min All Shorted Pins Heat Sink)
	NFAL5065L4B(T)	50 A / 650 V	3.7 kW	
	NFAL7565L4B(T)	75 A / 650 V	5.5 kW	

1. These motor ratings are general ratings, so it can be changed by the operating conditions.
2. Under development.

Internal Circuit Diagram

Three bootstrap circuits generate the voltage needed for driving the high−side IGBTs. The boost diodes are internal to the part and sourced from VDD (15 V). There is an internal level shift circuit for the high−side drive signals allowing all control signals to be driven directly from GND levels common with the control circuit such as the microcontroller without requiring external isolation with opto−couplers.

Major differences between SPM 49 −T version and normal version are shown on pins 38 and 39 of the internal circuit diagram as shown in Figure 3. The −T version has built−in NTC which senses the temperature of the power chip. Normal version NTC is not built in. Both −T version and Normal version function as conventional functions LVIC temperature sensing signal is output from the VTS pin.

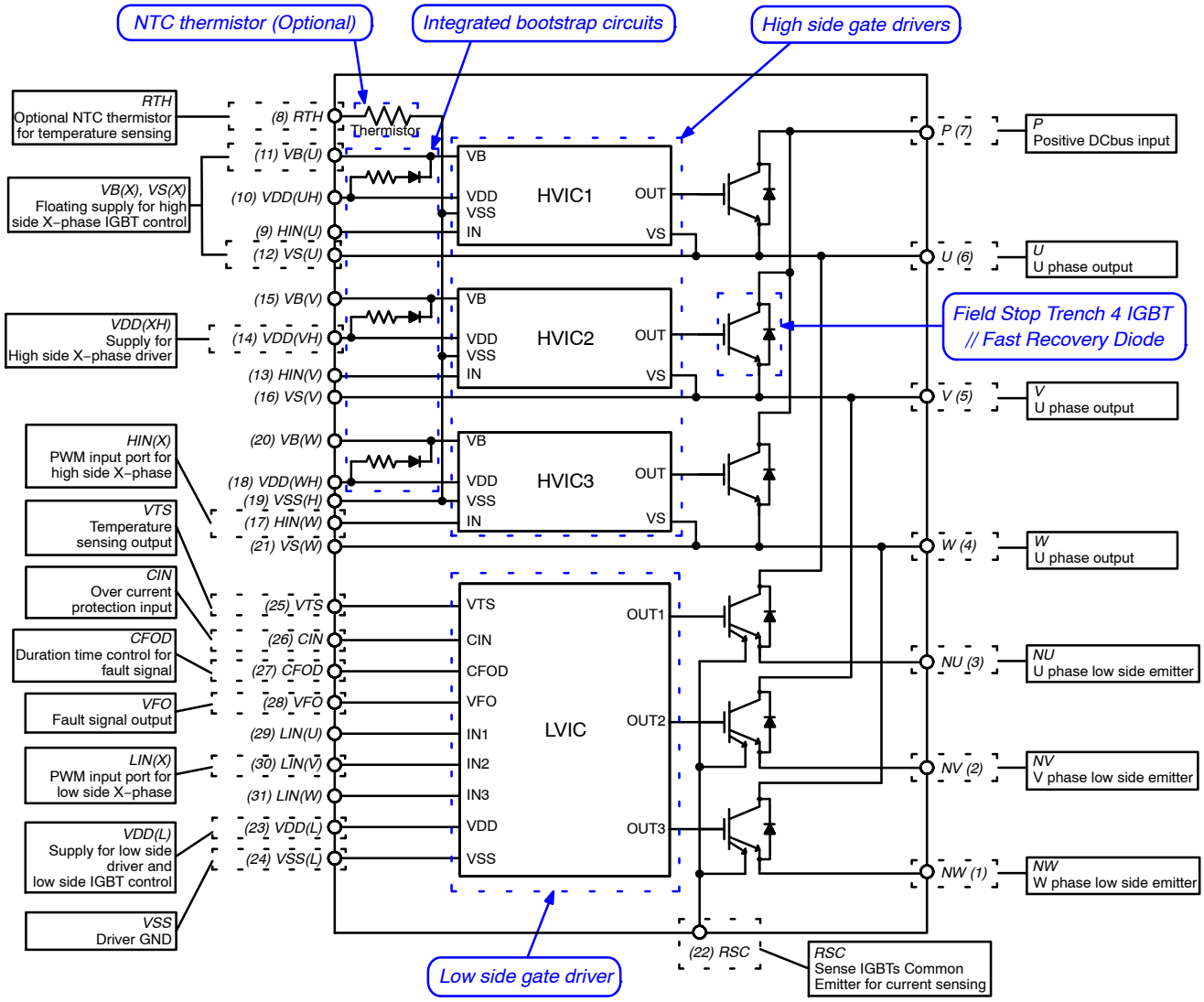


Figure 3. Internal Equivalent Circuit Diagram

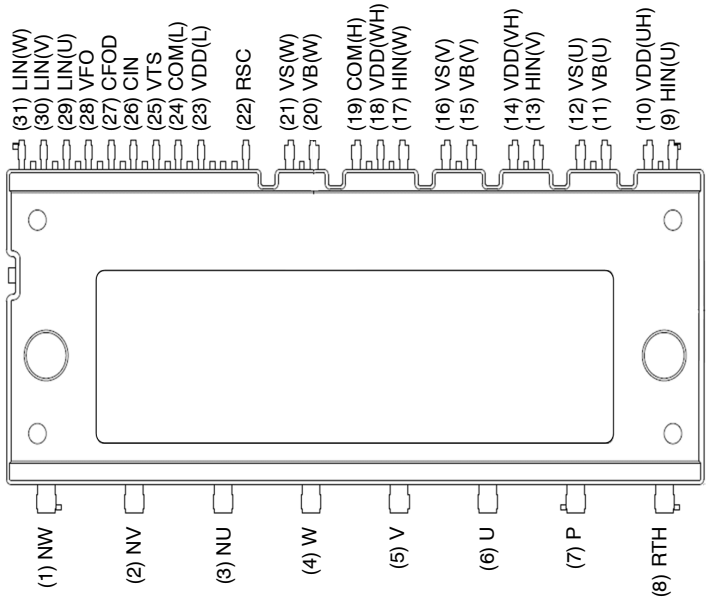


Figure 4. Package Top−View and Pin Assignment

Table 2. NUMBERS, NAMES AND DUMMY PINS

Pin Number	Name	Description
1	NW	Negative DC−Link Input for W Phase
2	NV	Negative DC−Link Input for V Phase
3	NU	Negative DC−Link Input for U Phase
4	W	Output for W Phase
5	V	Output for V Phase
6	U	Output for U Phase
7	P	Positive DC−Link Input
8	RTH	Series Resister for Thermistor (Temperature Detection)
9	HIN(U)	Signal Input for High−Side U Phase
10	VDD(UH)	High−Side Bias Votage for U Phase IC
11	VB(U)	High−Side Bias Voltage for U Phase IGBT Driving
12	VS(U)	High−Side Bias Voltage GND for U Phase IGBT Driving
13	HIN(V)	Signal Input for High−Side V Phase
14	VDD(VH)	High−Side Bias Votage for V Phase IC
15	VB(V)	High−Side Bias Voltage for V Phase IGBT Driving
16	VS(V)	High−Side Bias Voltage GND for V Phase IGBT Driving
17	HIN(W)	Signal Input for High−Side W Phase
18	VDD(WH)	High−Side Bias Votage for W phase IC
19	VSS(H)	Low−Side Common Supply Ground, Connected to HVIC
20	VB(W)	High−Side Bias Voltage for W Phase IGBT Driving
21	VS(W)	High−Side Bias Votage GND for W phase IGBT Driving
22	RSC	Resistor for Over and Short−Circuit Current Detection
23	VDD(L)	Low−Side Bias Votage for IC and IGBTs Driving
24	VSS(L)	Low−Side Common Supply Ground, Connected to LVIC
25	VTS	Voltage Output for LVIC Temperature Sensing Unit
26	CIN	Input for Over Current Protection
27	CFOD	Capacitor for Fault Output Duration Selection
28	VFO	Fault Output
29	LIN(U)	Signal Input for Low−Side U Phase
30	LIN(V)	Signal Input for Low−Side V Phase
31	LIN(W)	Signal Input for Low−Side W Phase

Detailed Pin Definition and Notification

Pins: VB(U) − VS(U), VB(V) − VS(V), VB(W) − VS(W)

High−side bias voltage pins for driving the IGBT / high−side bias voltage ground pins for driving the IGBTs.

VB(U), VB(V), VB(W) are integrated bootstrap diode cathode pins.

These are drive power supply pins for providing gate drive power to the high−side IGBTs.

The virtue of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high−side IGBTs. Each bootstrap capacitor is charged from the VDD supply during ON state of the corresponding low−side IGBT and Diode.

To prevent malfunctions caused by noise and ripple in the supply voltage, a low−ESR, a low−ESL filter capacitor should be mounted very close to these pins.

Pins: VDD(UH), VDD(VH), VDD(WH), VDD(L)

Low−side bias voltage pin / high−side bias voltage pins.

This is control supply pins for the built−in ICs.

These four pins should be connected externally.

To prevent malfunctions caused by noise and ripple in the supply voltage, a low−ESR, low−ESL filter capacitor should be mounted very close to these pins.

Pin: VSS(H), VSS(L)

Control signal ground pin.

This is supply ground pin for the built−in ICs.

Important! To avoid noise influences, the main power circuit current should not be allowed to blow through this pin.

Pins: HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W)

Signal input pins.

These pins control the operation of the built−in IGBTs.

They are activated by voltage input signals. The terminals are internally connected to a Schmitt−trigger circuit composed of 5 V−class CMOS.

The signal logic of these pins is active high. The IGBT associated with each of these pins is turned on.

ON when a sufficient logic voltage is applied to these pins.

The wiring of each input should be as short as possible to protect the SPM 49 against noise influences.

To prevent signal oscillations, an RC coupling as illustrated in Figure 32 is recommended.

Pin: CIN

Over−current and short−circuit detection input pin.

The current sensing shunt resistor should be connected between the pin CIN and the low−side ground

Pin VSS to detect over or short circuit current.

The shunt resistor should be selected to meet the detection levels matched for the specific application.

An RC filter should be connected to the CIN pin to eliminate noise.

The connection length between the shunt resistor and CIN pin should be minimized.

Pin: RSC

Low−side sense IGBT current flows through this pin. Short−circuit and over current can be detected at

this pin through an external resistor. If using three shunt resistors at N terminal for OCP and SCP without sensing from RSC, RSC pin should be connected to VSS pin.

Pin: VFO

Fault output pin.

This is the fault output alarm pin. An active low output is given on this pin for a fault state condition in the SPM 49.

The alarm conditions are: Short−Circuit Current Protection (SCP), and low−side bias Under−Voltage Lock Out (UVLO).

The VFO output is open drain configured. The VFO signal line should be pulled to the 5 V logic power supply with approximately 4.7 kΩ resistance.

Pin: CFOD

Fault output duration time control pin.

The fault−out pulse width time depends on the capacitance value of CFOD.

Pin: RTH (Optional for −T type)

For case temperature (Tc) detection, this pin should be connected to an external series resistor.

The external series resistor should be selected to meet the detection range matched for the specification of each application (for details, refer to Figure 26).

Pin: VTS

Analog temperature sensing output pin.

This is to indicate the temperature of LVIC with analog voltage. LVIC itself creates some power loss, but mainly heat generated from the IGBTs will increase the temperature of the LVIC.

VTS versus temperature characteristics is illustrated in Figure 22.

Pin: P

Positive DC−link pin.

This is the DC−link positive power supply pin of the inverter.

It is internally connected to the collectors of the high−side IGBTs.

To suppress surge voltage caused by the DC−link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin (tip: metal film capacitor is typically used).

Pins: NU, NV, NW

Negative DC−link pins.

These are the DC−link negative power supply pins (power ground) of the inverter.

These pins are connected to the low−side IGBT emitters of the each phase.

These pins are used to one shunt or three shunt resistor.

Pins: U, V, W

Inverter power output pins.

Inverter output pins for connecting to the inverter load (e.g. motor).

PACKAGE

Package Structure

Since heat dissipation is an important factor limiting the power module's current capability, the heat dissipation characteristics of a package are important in determining the performance. A trade−off exists among heat dissipation characteristics, package size, and isolation characteristics. The key to good package technology lies in the optimization package size while maintaining outstanding heat dissipation characteristics without compromising the isolation rating.

In SPM 49, technology was developed with DBC substrate that resulted in good heat dissipation characteristics. Power chips are attached directly to the DBC substrate. This technology is applied SPM 49, achieving improved reliability and heat dissipation.

Figure 5 shows the internal package structure and cross−sections including the lead frame and boding wires.

Figure 6 shows each creepage and clearance distance of the SPM 49 package.

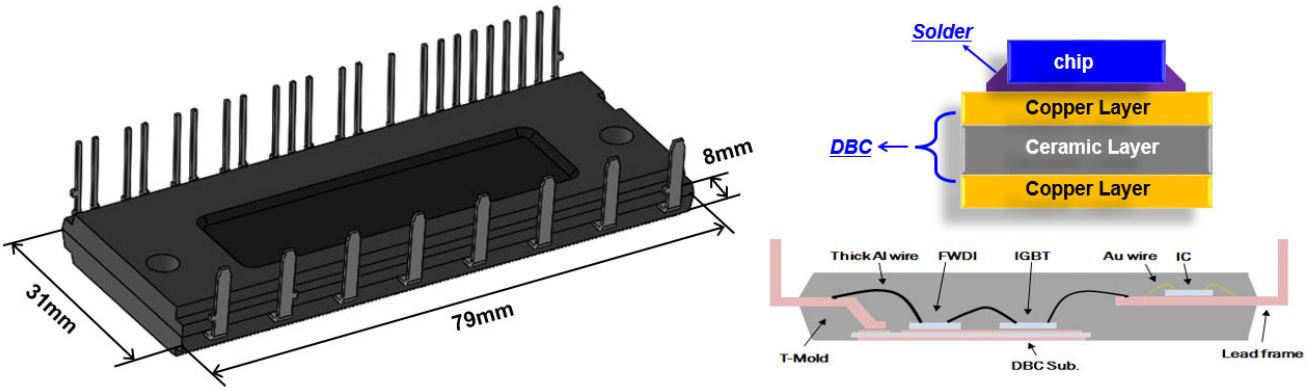


Figure 5. External View, Vertical Structure for Heat Dissipation and Cross Section of SPM 49

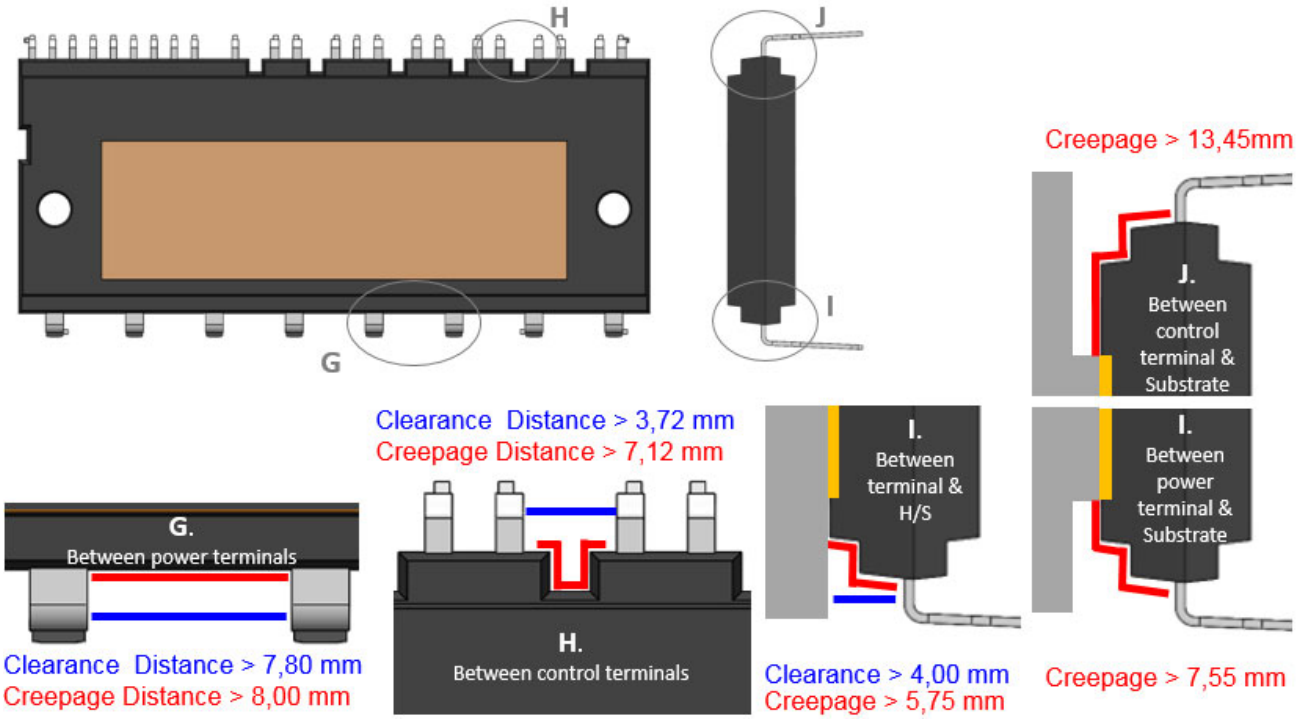


Figure 6. Isolation Distance of SPM 49

Package Outline

Unit: mm

NOTES:
1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b and c APPLY TO THE PLATED LEADS AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP.
4. POSITION OF THE LEAD IS DETERMINED AT THE BASE OF THE LEAD WHERE IT EXITS THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	8.40	8.60	8.80
A1	0.40	0.60	0.80
A2	7.90	8.00	8.10
A3	2.30	2.40	2.50
A4	3.90	4.00	4.10
A5	1.65	1.75	1.85
A6	3.40	3.50	3.60
A7	1.00 REF		
b	1.90	2.00	2.10
b1	---	---	2.80
b2	1.40 REF		
b3	---	---	2.20
b4	0.50	0.60	0.70
b5	---	---	0.80
c	0.45	0.50	0.60
D	78.80	79.00	79.20
D1	49.50	49.70	49.90
D2	69.85	70.00	70.15
D3	34.80	35.00	35.20
D4	37.60	37.80	38.00
D5	35.66	35.86	36.06

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E	30.80	31.00	31.20
E1	12.30	12.50	12.70
E2	35.75	36.20	36.65
E3	35.17 REF		
E4	26.60	26.80	27.00
E5	12.55	12.70	12.85
E6	6.80	7.00	7.20
e	10.00 BSC		
e1	2.54 BSC		
F	4.40	4.50	4.60
L	7.40 REF		
M	---	---	5.0°
R	0.50 REF		

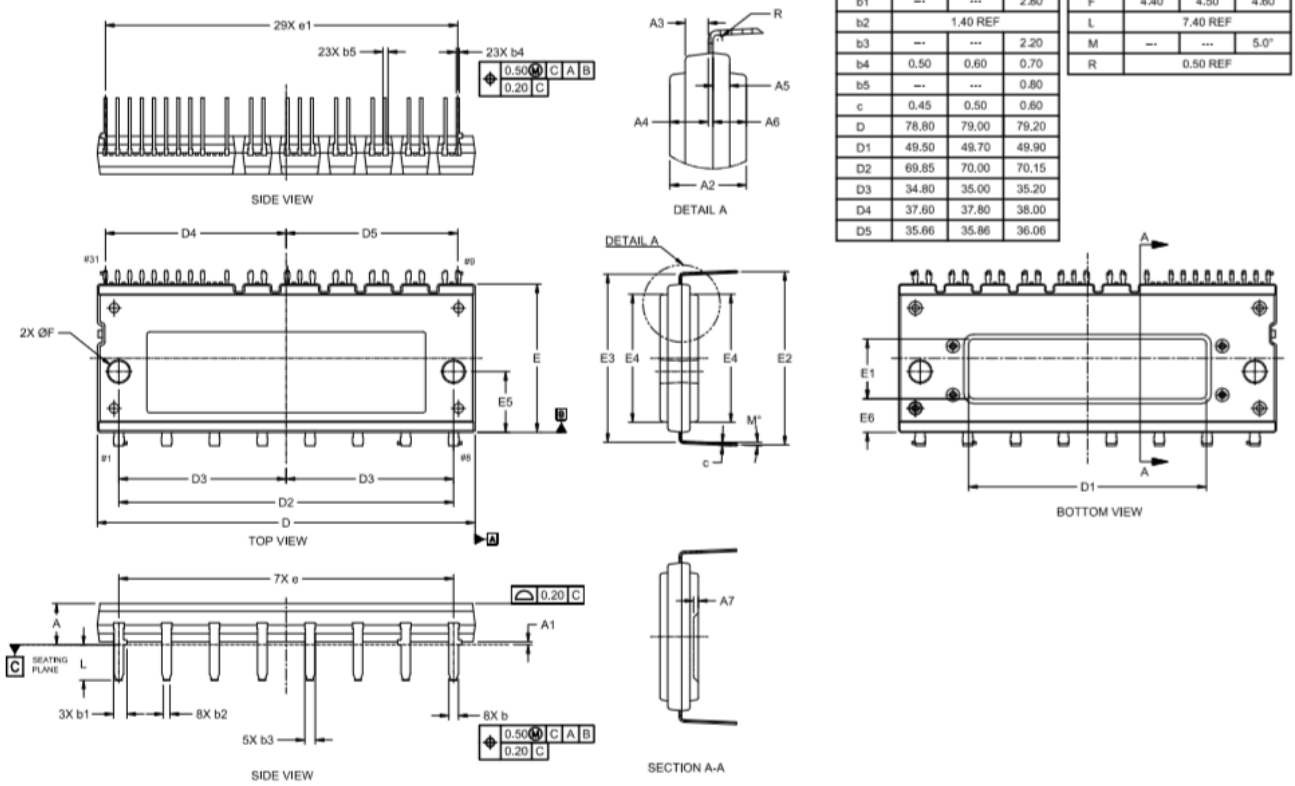


Figure 7. NFALxx65L4BT

Unit: mm

NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b and c APPLY TO THE PLATED LEADS AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP.
4. POSITION OF THE LEAD IS DETERMINED AT THE ROOT OF THE LEAD WHERE IT EXITS THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	8.40	8.60	8.80
A1	0.40	0.60	0.80
A2	7.90	8.00	8.10
A3	2.30	2.40	2.50
A4	3.90	4.00	4.10
A5	1.65	1.75	1.85
A6	3.40	3.50	3.60
A7	1.00 REF		
b	1.90	2.00	2.10
b1	---	---	2.80
b2	1.40 REF		
b3	---	---	2.20
b4	0.50	0.60	0.70
b5	---	---	0.80
c	0.45	0.50	0.60
D	78.80	79.00	79.20
D1	49.50	49.70	49.90
D2	69.85	70.00	70.15
D3	34.80	35.00	35.20
D4	37.60	37.80	38.00
D5	35.66	35.86	36.06

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E	30.80	31.00	31.20
E1	12.30	12.50	12.70
E2	35.75	36.20	36.65
E3	35.17 REF		
E4	26.60	26.80	27.00
E5	12.55	12.70	12.85
E6	6.80	7.00	7.20
e	10.00 BSC		
e1	2.54 BSC		
F	4.40	4.50	4.60
L	7.40 REF		
M	—	—	5.0°
R	0.50 REF		

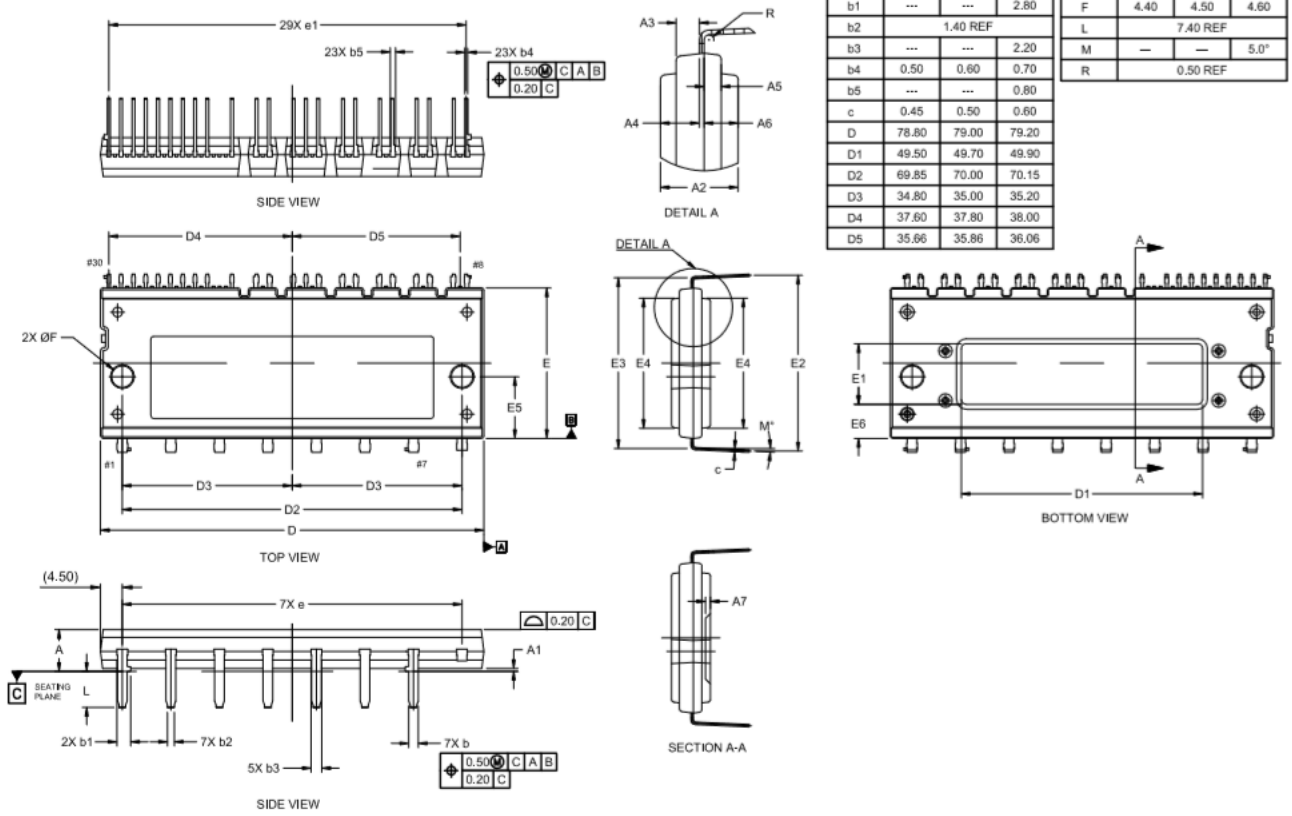
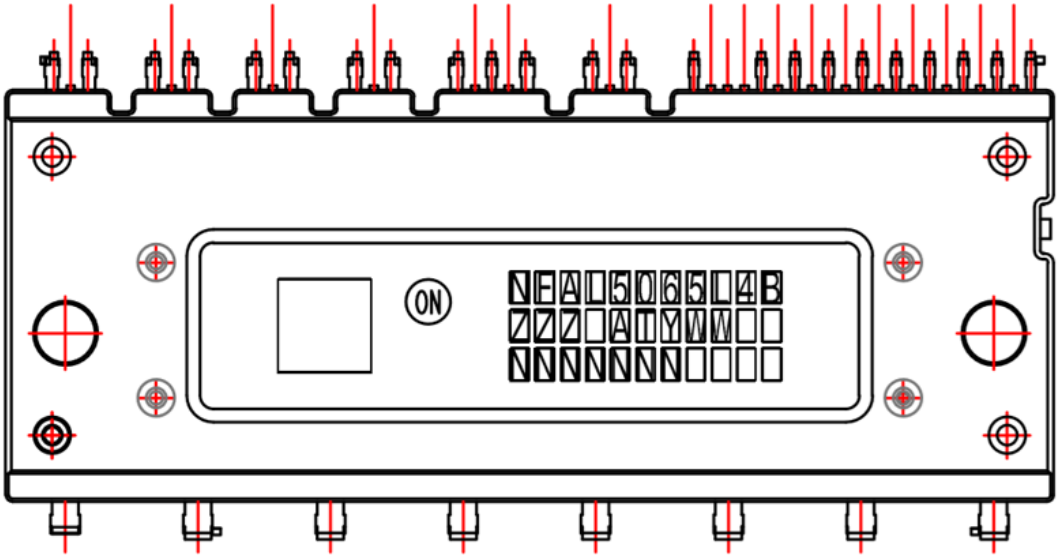


Figure 8. NFALxx65L4B

Marking Specification



* 2D CODE

NFAL5065L4Bzzz11K24A0000001

Orderable Part Number
Lot Number
Assembly & Test Site
Date Code
Marking Machine ID
Serial Number

* NOTE
1. ON : COMPANY LOGO
2. NFAL~ : OPN
3. ZZZ : LAST 3 DIGITS OF LOT NO
4. AT : ASSEMBLY & TEST SITE (SUZHOU : 1)
5. YWW : DATE CODE (Y : YEAR-SEE THE TABLE, WW : WORK WEEK)
6. NNNN : SERIAL NUMBER

Y	Alphabet
2017	J
2018	K
2019	L
2020	M
2021	N
2022	O
2023	P
2024	Q
2025	R
2026	S
2027	T

Figure 9. Marking Specification

PRODUCT SYNOPSIS

This section discusses electrical specification, characteristics and mechanical characteristics.

Absolute Maximum Rating

(Tj = 25°C, unless otherwise specified)

ABSOLUTE MAXIMUM RATING (Tj = 25°C, unless otherwise specified)

Symbol	Parameter	Conditions	Rating	Unit
INVERTER PART (BASE ON NFAL5065L4B(T))				
VPN	Supply Voltage	Applied between P − NU, NV, NW	450	V
$VPN_{(Surge)}$	Supply Voltage (Surge)	Applied between P − NU, NV, NW	500	V
Vces	Collector − Emitter Voltage		650	V
±Ic	Each IGBT Collector Current	Tc = 25°C, Tj ≤ 150°C (Note 3)	50	A
±Icp	Each IGBT Collector Current (Peak)	Tc = 25°C, Tj ≤ 150°C, Under 1 ms Pulse Width	100	A
Pc	Collector Dissipation	Tc = 25°C per One Chip	192	W
Tj	Operating Junction Temperature (Note 3)		−40~150	°C
CONTROL PART				
VDD	Control Supply Voltage	Applied between VDD(XX) − VSS	20	V
VBS	High−Side Control Bias Voltage	Applied between VB(X) − VS(X)	20	V
VIN	Input Signal Voltage	Applied between HIN(X), LIN(X) − VSS	−0.5~VDD + 0.5	V
VFO	Fault Output Supply Voltage	Applied between VFO − VSS	−0.5~VDD + 0.5	V
IFO	Fault Output Current	Sink Current at VFO Pin	5	mA
VCIN	Current Sensing Input Voltage	Applied between CIN − VSS	−0.5~VDD + 0.5	V
Tj	Operating Junction Temperature		−40~150	°C
BOOTSTRAP DIODE PART				
VRRM	Maximum Repetitive Reverse Voltage		650	V
CBOOT	Load Capacitor for Bootstrap supply	Tc = 25°C, Tj ≤ 150°C, VDD < 20 V	470	μF
Tj	Operating Junction Temperature		−40~150	°C
TOTAL SYSTEM				
VPN(PROT)	Self−Protection Supply Voltage Limit (Short−Circuit Protection Capability)	VDD(L), VB(X) = 13.5~ 6.5 V, Tj = 150°C, (Non−Repetitive, < 2 μs)	400	V
Tc	Module Case Operation Temperature	See Figure 10	−40~125	°C
Tstg	Storage Temperature		−40~125	°C
Viso	Isolation Voltage	60 Hz, Sinusoidal, 1−Minute, Connect Pins to Heat Sink	2500	Vrms

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. These values had been made on acquisition by the calculation considered to design factor. The maximum junction temperature rating of power chips integrated within the SPM 49 products are 150°C.

THERMAL RESISTANCE (BASE ON NFAL5065L4B(T))

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Rth(j−c)Q	Junction to Case Thermal Resistance (Note 4)	Inverter IGBT Part (per 1/6 Module)	−	−	0.65	°C/W
Rth(j−c)F		Inverter FWDi Part (per 1/6 Module)	−	−	0.96	

4. For the measurement point of case temperature (T_C), please refer Figure 10.

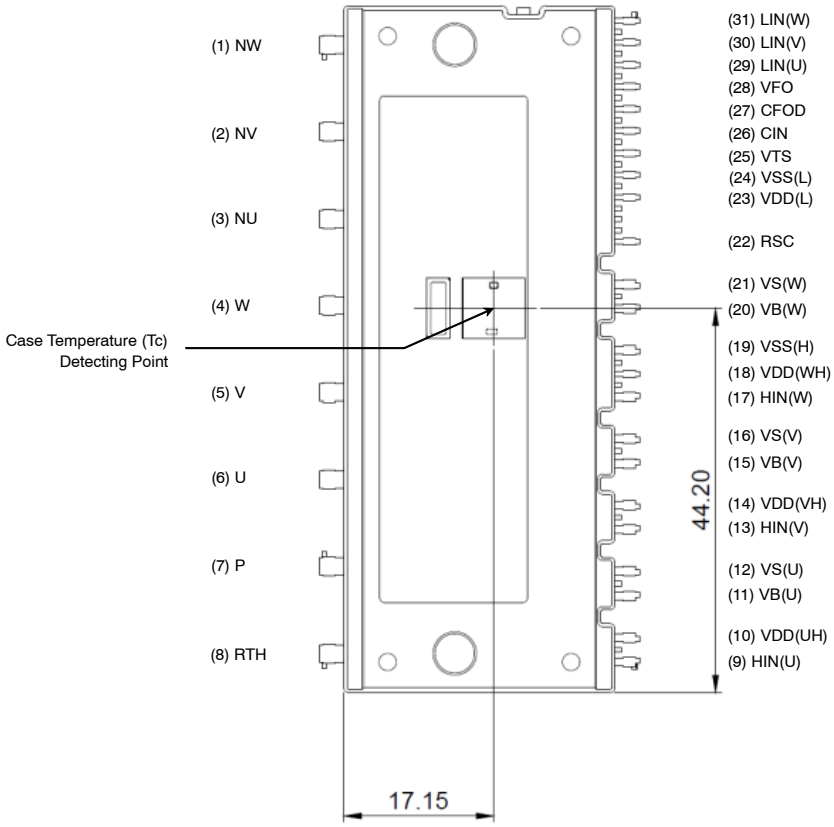


Figure 10. Case Temperature (Tc) Detecting Point

Electrical Characteristic

(Tj = 25°C, unless otherwise specified)

ELECTRICAL CHARACTERISTIC (T_J = 25°C unless otherwise noted)

Symbol		Parameter	Test Condition	Test Condition	Min	Typ	Max	Unit
INVERTER PART (BASE ON NFAL5065L4B(T))								
VCE(sat)		Collector–Emitter Saturation Voltage	VDD, VBS = 15 V, yIN(X) = 5 V	Ic = 50 A	–	1.55	2.05	V
VF		FWDi Forward Voltage	yIN(X) = 5 V	If = 50 A	–	1.7	2.2	
High Side	ton	Switching Times (Note 5)	VPN = 300 V, VDD = 15 V, VBS = 15 V, Ic = 50 A, V_{IN} = 0 V ↔ 5 V, Inductive Load See Figure 11		1.10	1.70	2.30	μs
	tc(on)				–	0.25	0.55	
	toff				–	1.70	2.30	
	tc(off)				–	0.16	0.46	
	trr				–	0.1	–	
Low Side	ton				1.00	1.60	2.20	
	tc(on)				–	0.25	0.55	
	toff				–	2.00	2.60	
	tc(off)				–	0.18	0.48	
	trr				–	0.10	–	
BOOTSTRAP CIRCUIT PART								
VF		Forward Voltage		If = 0.1 A, Tj = 25°C	2.1	2.5	2.9	V
RBOOT		Bootstrap Resistor		If = 0.1 A, Tj = 25°C	12.5	15.5	18.5	Ω

ELECTRICAL CHARACTERISTIC (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Test Condition	Min	Typ	Max	Unit
CONTROL PART (BASE ON NFAL5065L4B(T))							
IQDDH	Quiescent VDD Supply Current	VDD(XH) = 15 V, HIN(X) = 0 V	VDD(XH) − VSS(H)	−	−	0.30	mA
IQDDL		VDD(L) = 15 V, LIN(X) = 0 V	VDD(L) − VSS(L)	−	−	3.50	
IQBS	Quiescent VBS Supply Current of Each Phase	VB(X) − VS(X) = 15 V, HIN(X) = 0 V		−	−	0.30	
ISEN	Sensing Current of Each Sense IGBT	VDD(L) = 15 V, VIN = 5 V, RSC = 0 Ω, No Connection of Shunt Resistor at NX Terminals	Ic = 50 A	−	17.0	−	
VFOH	Fault Output Voltage	VDD(L) = 15 V, CIN = 0 V, Pulled up to 5 V by 10 kΩ		4.90	−	−	V
VFOL		VDD(L) = 15 V, CIN = 1 V, IFO = 1 mA		−	−	0.95	
VSC(ref)	Short−Circuit Trip Level	VDD(L) = 15 V	CIN − VSS(L)	0.46	0.48	0.50	
UVDDD	Supply Circuit, Under−Voltage Protection (Note 6)	Detection Level		10.3	−	12.5	
UVDDR		Reset Level		10.8	−	13.0	
UVBSD		Detection Level		10.0	−	12.0	
UVBSR		Reset Level		10.5	−	12.5	
ISC	Short Circuit Trip Level	Rsc = 24 Ω (±1%), No Connection of Shunt Resistor at NU, NV, NW		75	−	−	A
tFOD	Fault−Out Pulse Width	CFOD = 22 nF		1.6	−	−	ms
VTS	LVIC Temperature Sensing Voltage Output	VDD(L) = 15 V, VTS − VSS(L) = 10 nF, TLVIC = 25°C		0.909	1.030	1.151	V
VIN(ON))	ON Threshold Voltage	Applied between HIN(X), LIN(X) − VSS		−	−	2.6	
VIN(OFF)	OFF Threshold Voltage			0.8	−	−	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. ton and toff include the propagation delay time of the internal drive IC. tc(on) and tc(off) are the switching time of IGBT itself under the given gate driving condition internally. For the detail information, please refer to Figure 11.
6. Short−circuit current protection is functioning only at low side.

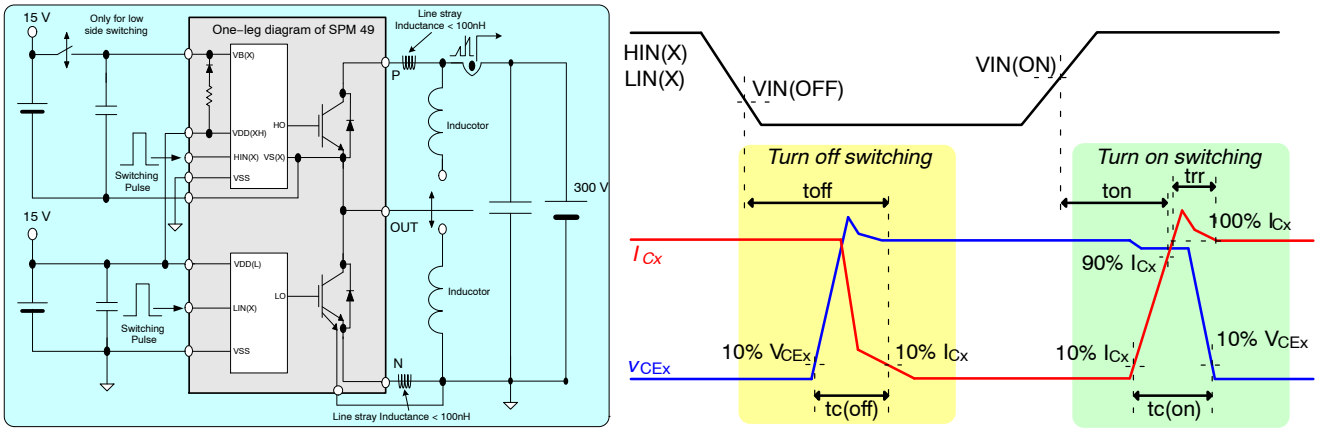


Figure 11. Switching Evaluation Circuit and Switching Time Definition

Recommended Operating Conditions

(Base on NFAL5065L4B (T))

RECOMMENDED OPERATING CONDITIONS (Base on NFAL5065L4B(T))

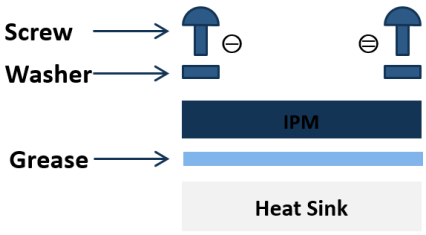
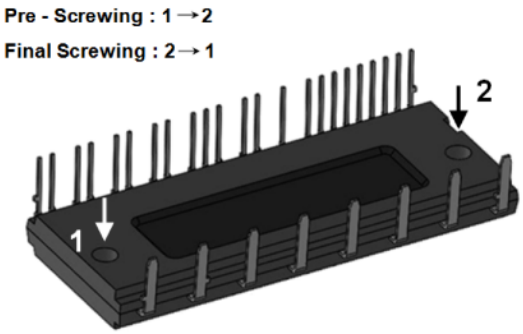
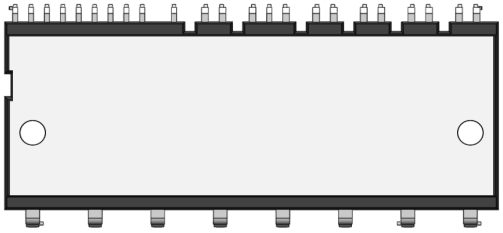
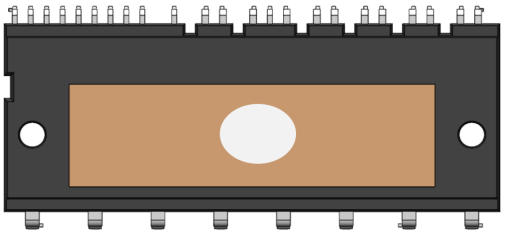
Symbol	Parameter	Condition	Min	Typ	Max	Unit
VPN	Supply Voltage	Applied between P – N_x	–	300	400	V
VDD	Control Supply Voltage	Applied VDD – VSS	13.5	15.0	16.5	
VBS	High−Side Bias Voltage	Applied between VB(X) – VS(X)	13.0	15.0	18.5	V
dVDD/dt, dVBS/dt	Control Supply Variation		−1	–	+1	V/μs
tdead	Blanking Time for Preventing Arm−Short	For Each Input Signal	1.5	–	–	μs
FPWM	PWM Input Signal	40°C ≤ Tc ≤ 125°C, – 40°C ≤ Tj ≤ 150°C	–	–	20	kHz
PWIN(ON)	Minimum Input Pulse Width	VDD = VBS = 15 V, I_C ≤ 50A, Wiring Inductance between NU, NV, NW and DC Link N < 10 nH	1.1	–	–	μs
PWIN(OFF)			2.0	–	–	
Tj	Junction Temperature		−40	–	+150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. This product might not make response if input pulse with is lee than the recommended value.

Mechanical Characteristics

MECHANICAL CHARACTERISTICS

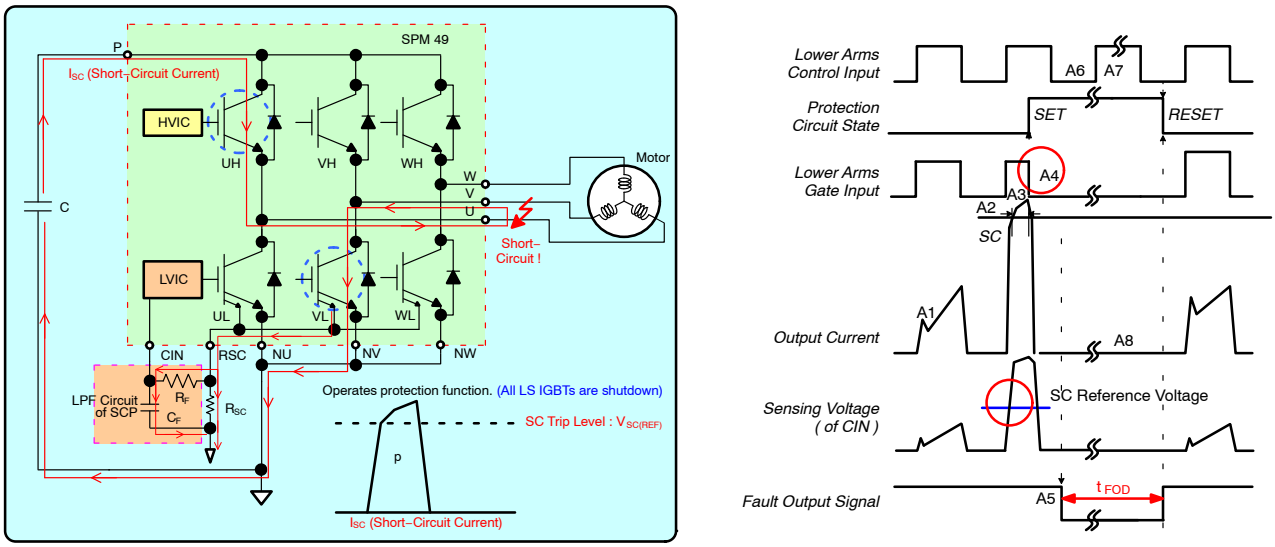
Item	Recommended Condition
Pitch	79.0 ±0.2 mm (Please refer to Package Outline Diagram)
Screw	Diameter: M4 Recommended thread engagement for screws with property class 4.8 to 6.8 for different materials
Washer	Spring washer diameter: D = 7 mm to DIN 127 or DIN 128 Plane washer dimensions: D = 9 mm to DIN 125
Heat sink	Material: Aluminum or Copper Warpage (the surface that contacts IPM): −50 to 100 μm Screw holes must be countersunk. No contamination on the heat sink surface that contacts IPM.
Torque	Pre tightening : 0.2~0.3 Nm on first screw Pre tightening : 0.2~0.3 Nm on second screw Final tightening : 0.98~1.47 Nm on second screw Final tightening : 0.98~1.47 Nm on first screw  
Grease	Silicone grease. Thickness : 50 to 100 μm Uniformly apply silicon grease to whole back. Thermal foils are only recommended after careful evaluation. Thickness, stiffness and compressibility parameters have a strong influence on performance.  Recommend  Not Recommend

OPERATION SEQUENCE FOR PROTECTIONS

Short Circuit Protection

The 650 V SPM 3 uses external shunt resistor for the short circuit current detection, as shown in Figure 12. LVIC has a built−in short−circuit current protection function. This protection function senses the voltage to the CIN pin. If this voltage (VCIN) exceeds the VSC(ref) (the threshold voltage trip level of over current protection) specified in the device datasheets (VSC(ref), typ. is 0.48 V), a fault signal is asserted and the all low side IGBTs are turned off.

Typically, the maximum short−circuit current magnitude is gate−voltage dependent: higher gate voltage (VDD and VBS) results in larger short−circuit current. To avoid potential problems, the maximum short circuit trip level is set below 1.5 times the nominal rated collector current. The LVIC short circuit protection timing chart is shown in Figure 12.

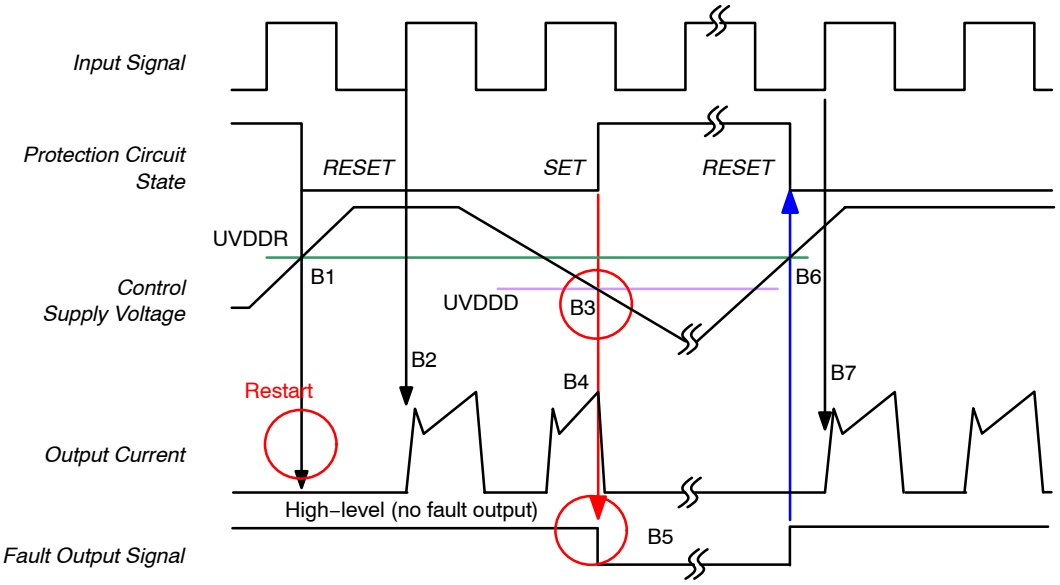


NOTES:
8. A1: normal operation: IGBT turn on and carrying current.
9. A2: short−circuit current detection (SC trigger).
10. A3: hard IGBT gate interrupt.
11. A4: IGBT turns off.
12. A5: fault output timer operation start with internal delay (min. 1.6 ms, CFOD = 22 pF), Fault−out duration time is controlled by CFOD.
13. A6: input “L”: IGBT turn off state.
14. A7: input “H”: IGBT turn on state, but during the active period of fault output the IGBT doesn’t turn on.
15. A8: IGBT keeps turn off state

Figure 12. Operation of Short−Circuit Protection & Timing Chart of Short−Circuit Protection Function

Under−Voltage Lock Out Protection

The LVIC has an Under−Voltage Lock Out protection (UVLO) function to protect the low−side IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 13.

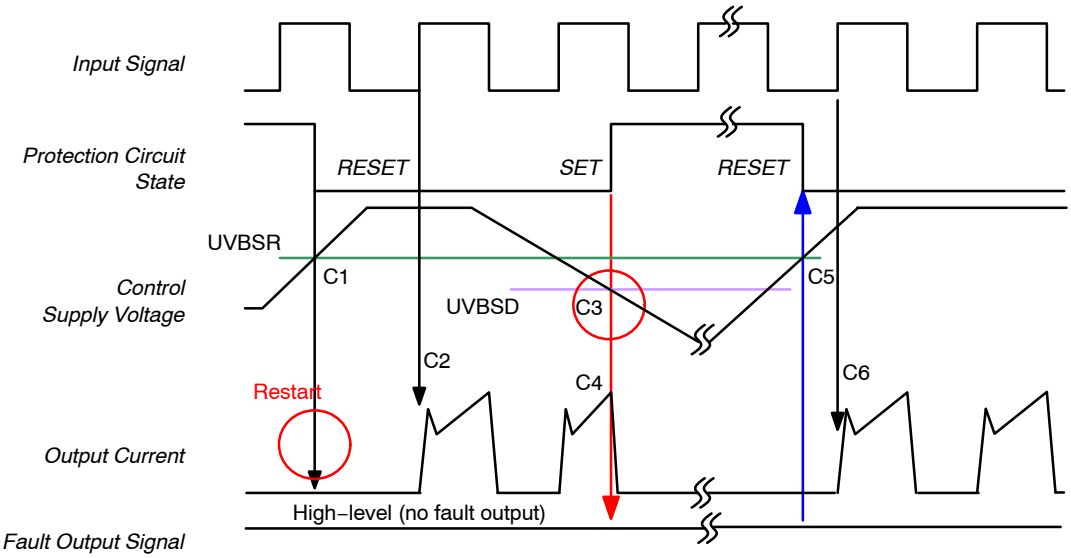


NOTES: *Low−Side Protection Sequence*

16. B1: control supply voltage rise: after the voltage rises UVDDR, the circuits starts to operate when the next input is applied.
17. B2: normal operation: IGBT turn on and carrying current.
18. B3: under−voltage detection UVDDD.
19. B4: IGBT turn off in spite of control input is alive.
20. B5: fault output signal starts.
21. B6: under−voltage reset UVDDR.
22. B7: normal operation: IGBT turn on and carrying current. If fault−out duration (tfod) by external capacitor at CIN pin is longer than UVDDR timing, fault output and IGBT state are cleared after tfod.

Figure 13. Timing Chart of Low−side Under−Voltage Protection Function

The HVIC has an under−voltage lockout function to protect the high−side IGBT from insufficient gate driving voltage. A timing chart for this protection is shown in Figure 14. A fault−out (VFO) alarm is not given for low HVIC bias conditions.



NOTES: *High−Side Protection Sequence*

23. C1: control supply voltage rises: after the voltage reaches UVBSR, the circuit starts when the next input is applied.
24. C2: normal operation: IGBT turn on and carrying current.
25. C3: under−voltage detection (UVBSD).
26. C4: IGBT turn off in spite of control input is alive, but there is no fault output signal.
27. C5: under−voltage reset (UVBSR).
28. C6: normal operation: IGBT turn on and carrying current

Figure 14. Timing Chart of High−Side Under−Voltage Protection Function

KEY PARAMETER DESIGN GUIDANCE

For stable operation, there are recommended parameters for passive components and bias conditions, considering operating characteristics of the 650 V SPM 49 series

Selection of RSC Resistor for Protection

Figure 15 is an example circuit of the short−circuit protection using the R_{SC} resistor. Sense IGBT is employed for the low side. The designer can use the RSC pin for Over−Current Protection (OCP) and Short−Circuit Protection (SCP) without an external shunt resistor at the N−terminal. The line current on RSC is detected and the protective operation signal is passed through the RC filter. If the voltage (VCIN) exceeds the VSC(ref), all the gates of the N−side three IGBTs are turned off and the fault signal is transmitted from SPM 49 to MCU. Since repetitive short circuit is not allowable, IGBT operation should be halted immediately when the fault signal is given. Figure 16 shows "R_{SC} resistance vs. trip current" curve of NFAL7565L4B(T) under the shunt resistor = 0 Ω condition.

For current sensing, apply an external shunt resistor at each N terminal. Sensing voltage from RSC pin is influenced by an external shunt resistor, as shown in Figure 17.

Figure 17 shows RSC value of NFAL7565L4B(T) under one−shunt resistor condition. For adequate RSC value in a three−shunt structure, the RSC value needs to be considered by the N−terminal shunt resistor value and target protection current level.

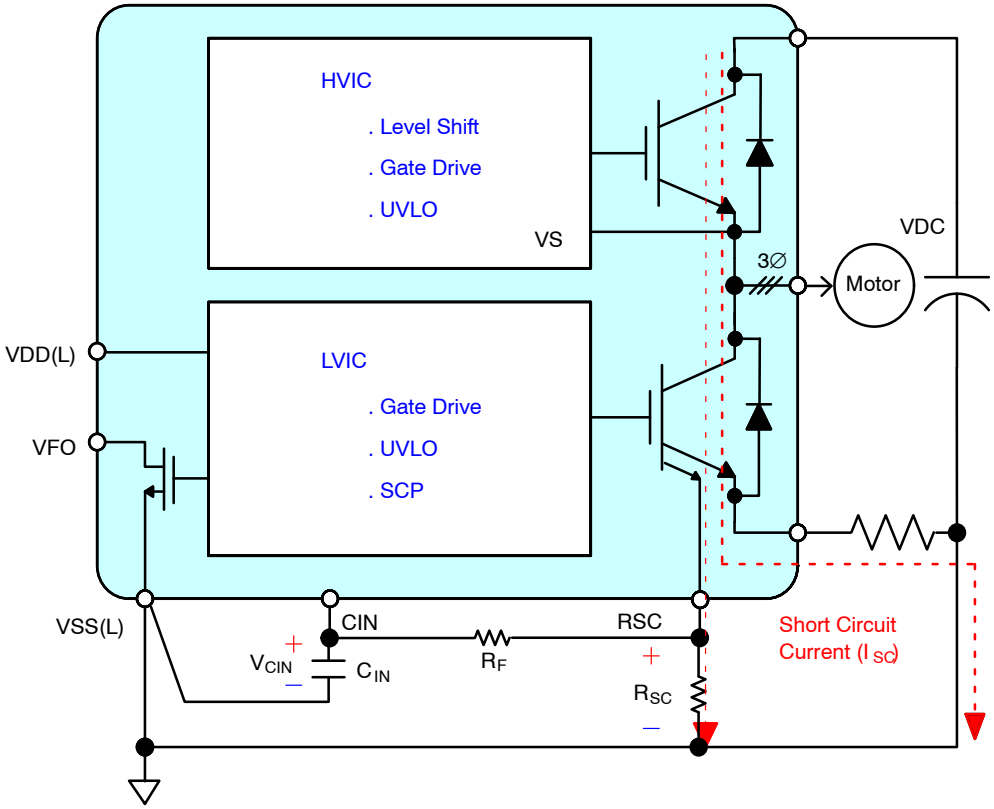


Figure 15. Function Current Path in Short−Circuit Condition by Leg Short Circuit

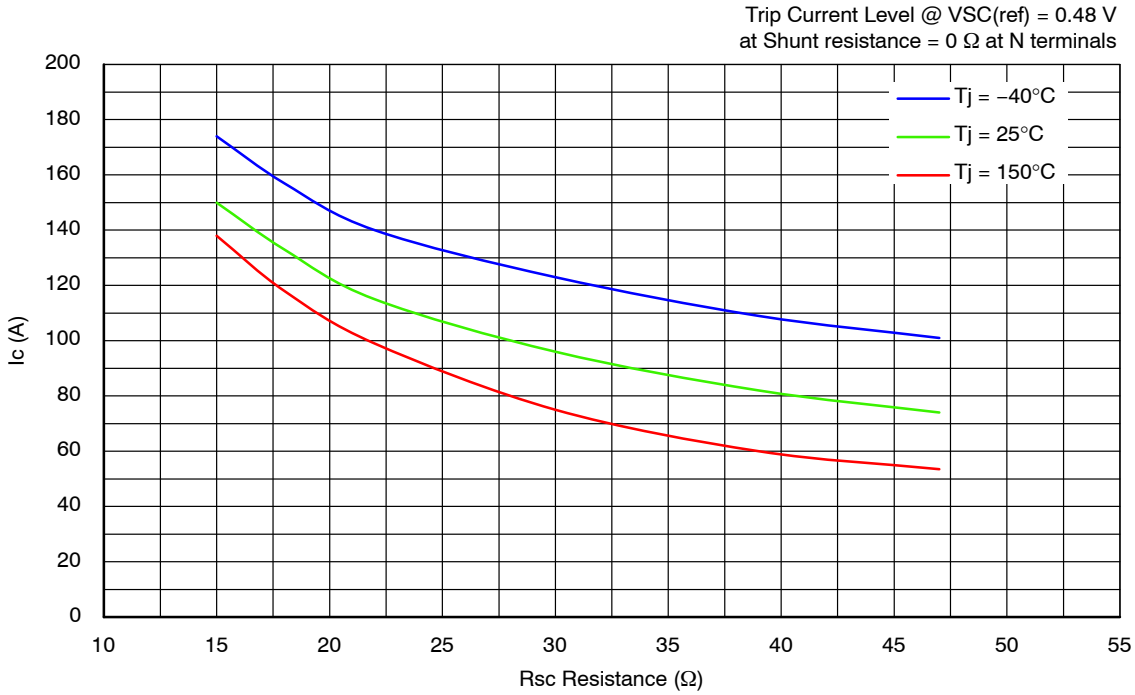
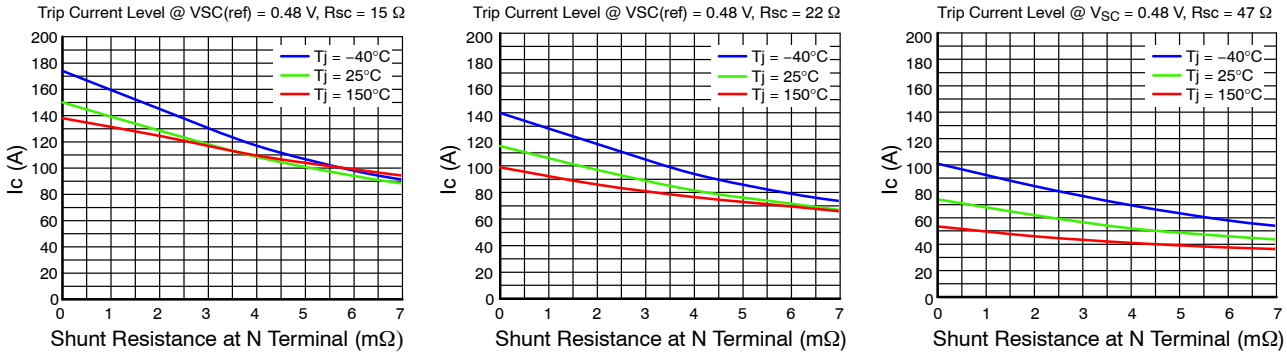


Figure 16. Rsc Resistance vs. Trip Current Level for Protection at Variable Junction Temperature of NFAL7565L4B(T)



(a) (b) (c)

Figure 17. Trip Current Level vs. Shunt Resistor of NFAL7565L4B(T)
(a): R_{SC} = 15 Ω, (b): R_{SC} = 22 Ω, (c): R_{SC} = 47 Ω

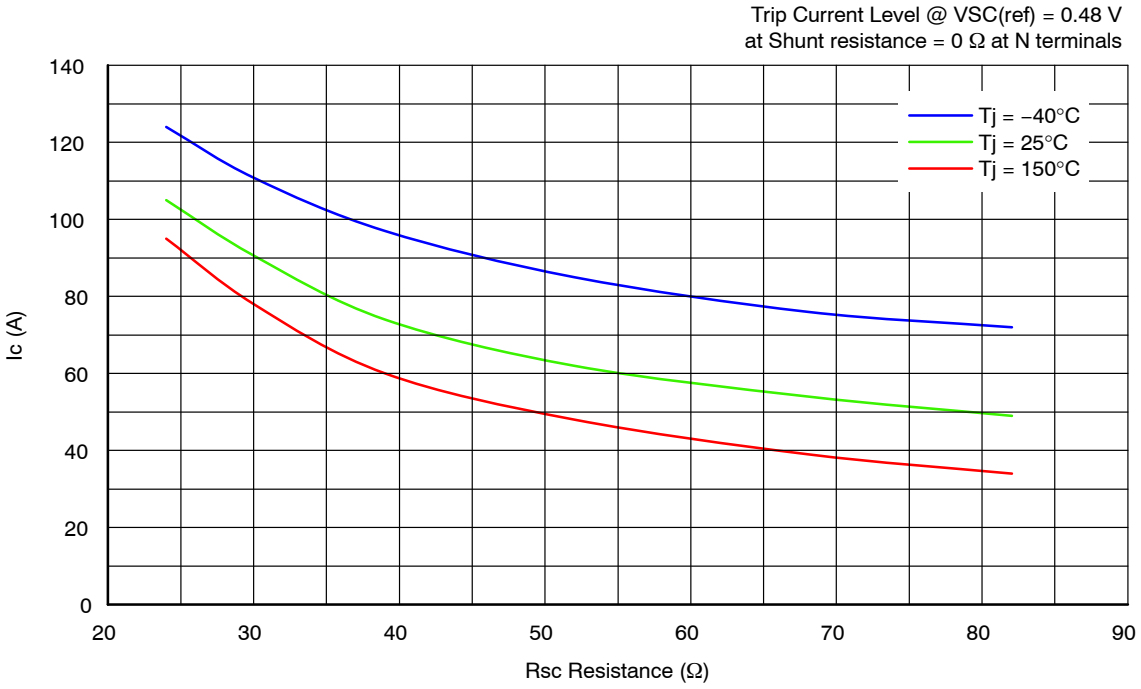


Figure 18. Rsc Resistance vs. Trip Current Level for Protection at Variable Junction Temperature of NFAL5065L4B(T)

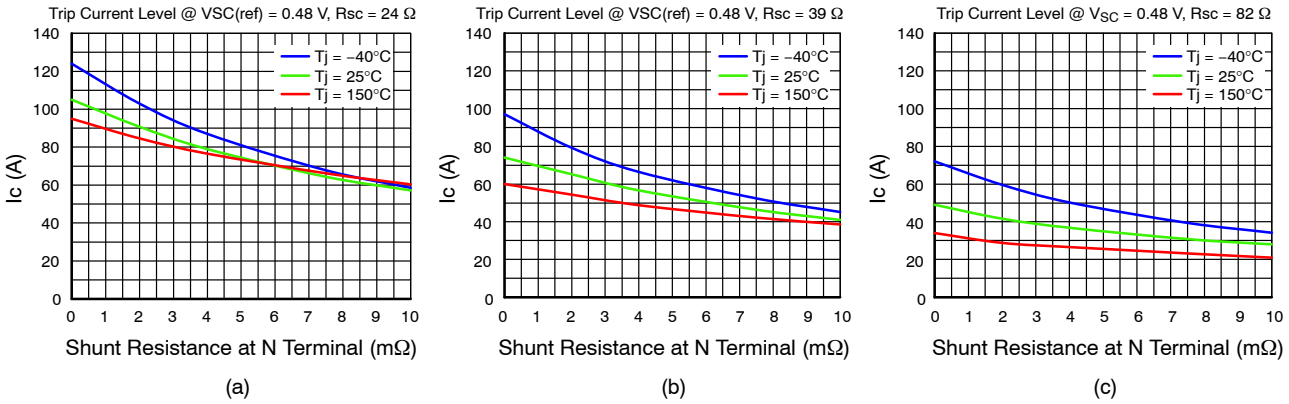


Figure 19. Trip Current Level vs. Shunt Resistor of NFAL5065L4B(T)
(a): R_{SC} = 24 Ω, (b): R_{SC} = 39 Ω, (c): R_{SC} = 82 Ω

Thermal Sensor Output (TOT) and NTC Thermistor

The junction temperature of power devices should not exceed the maximum junction temperature. Even though there is some margin between the Tj_{MAX} specified on the datasheet and the actual Tj_{MAX} at which power devices get destroyed, caution should be given to make sure the junction temperature stays well below the Tj_{MAX}. One of the inconveniences in using previous versions of SPM 49 series products was lack of temperature monitoring. An NTC had to be mounted on the heat sink or very close to the module if over−temperature protection is required in the application

Circuit of VTS

The Thermal Sensing Unit analog voltage output reflects the temperature of the LVIC in 650 V SPM 49 version 6 series products. The relationship between VTS voltage output and LVIC temperature is shown in Figure 22. It does not have any self−protection function, and, therefore, it should be used appropriately based on application requirement. It should be noted that there is a time lag from IGBT temperature to LVIC temperature. It is very difficult to respond quickly when temperature rises sharply in a transient condition such as shoot−through event. Even though VTS has some limitation, it will be definitely useful in enhance the system reliability. Figure 20 shows the LVIC location of SPM 49 series.

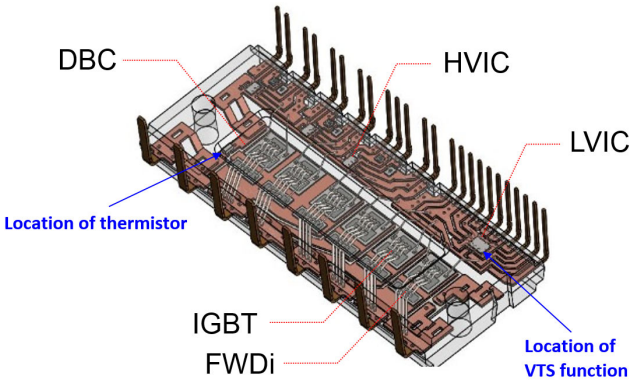


Figure 20. Location of VTS Function (LVIC) and NTC

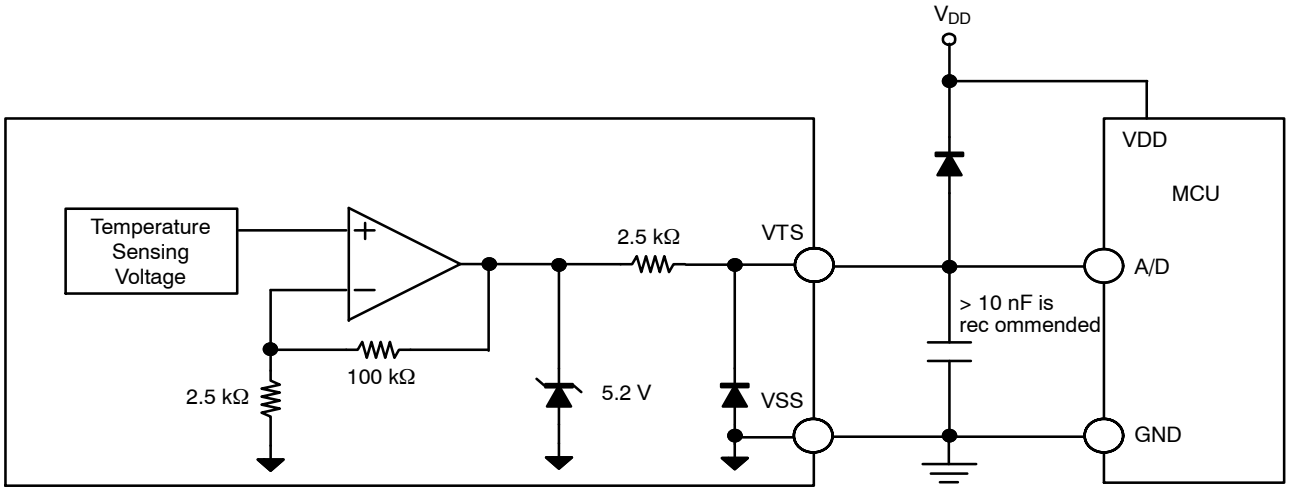


Figure 21. Internal Block Diagram and Interface Circuit of VTS

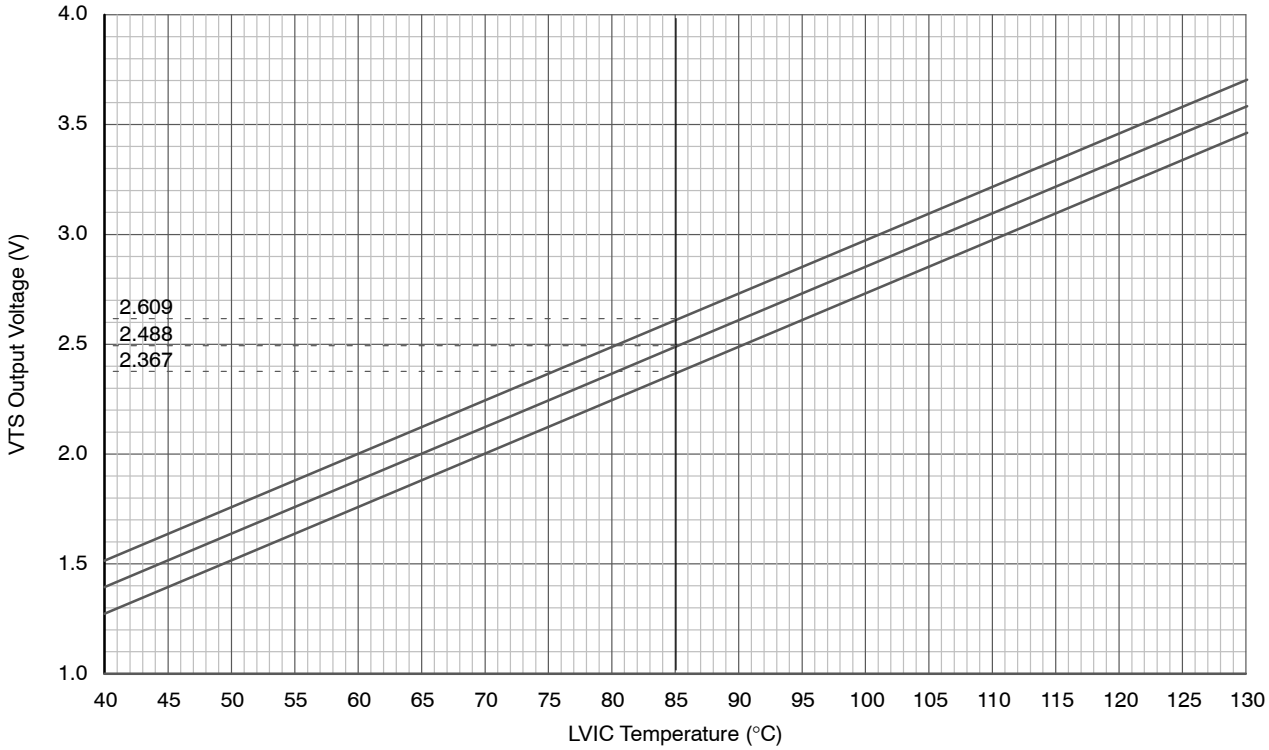


Figure 22. Temperature vs. VTS

Figure 21 shows the equivalent circuit diagram of VTS inside IC and a typical application diagram. This output voltage is clamped to 5.2 V by an internal Zener diode, but in case the maximum input range of Analog to Digital converter of MCU is below 5.2 V, an external Zener diode should be inserted between an A/D input pin and the analog ground pin of MCU. An amplifier can be used to change the range of voltage input to the Analog to Digital converter to have better resolution of the temperature. It is recommended to add a ceramic capacitor of 1000 pF between VTS and VSS (Signal Ground) to make the VTS more stable.

Therefore, the load connected to VTS pin should be minimized to maintain the accurate voltage output level without degradation. Figure 22 shows that the relationship between VTS voltage and LVIC temperature. It can be expressed as the following equation.

$VTS_{,min} = 0.0243 \times T_{LVIC} + 0.3015$ [V]

$VTS_{,typ} = 0.0243 \times T_{LVIC} + 0.4225$ [V]

$VTS_{,max} = 0.0243 \times T_{LVIC} + 0.5435$ [V]

The maximum variation of VTS is 0.121 V, and the minimum variation of VTS is 0.121 V due to process variation which is equivalent ±5°C approximately. This is regardless of the temperature because the slopes of three lines are identical. If the ambient temperature information is available. For example, through NTC in the system, VTS can be measured to adjust the offset before the motor starts to operate. As temperature decreases further below 0°C, VTS decreases linearly until it reaches zero volts. If the temperature of LVIC increases above 150°C, which is above the maximum operating temperature, VTS would increase theoretically up to 5.2 V until it gets clamped by the internal zener diode.

Circuit of NTC Thermistor

The Motion SPM 49 series includes a Negative Temperature Coefficient (NTC) thermistor for module internal temperature sensing. This thermistor is located in DBC substrate with the power chip (IGBT//FWDi).

Therefore, the thermistor can accurately reflect the temperature of the power chip (see Figure 23).

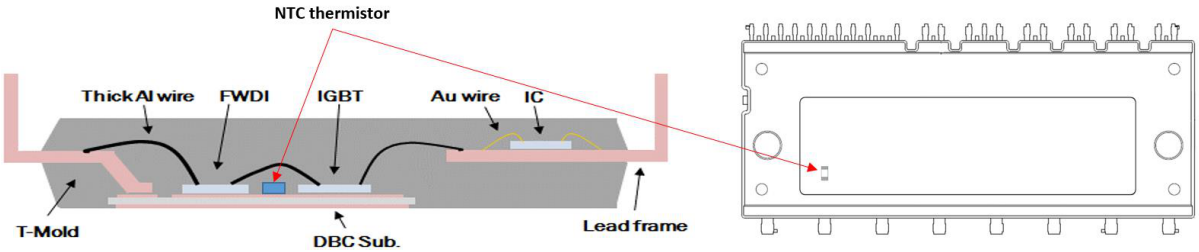


Figure 23. Location of NTC Thermistor in SPM 49 Package

Normally, circuit designers use two kinds of circuit for temperature protection (monitoring) by NTC thermistor. One is circuit by Analog−Digital Converter (ADC). The other is circuit by comparator. Figure 24 shows examples of application circuits with an NTC thermistor.

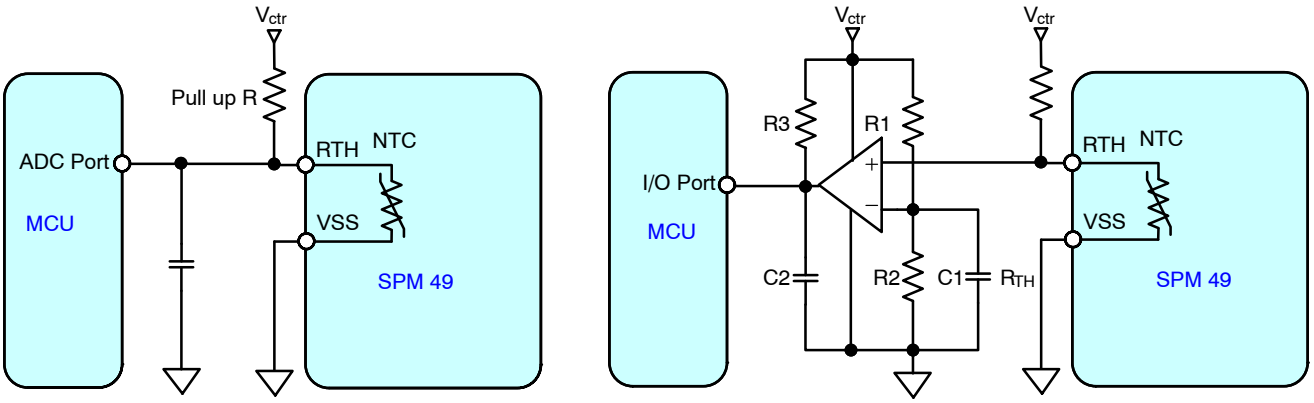


Figure 24. Over Temperature Protection Circuit by MCU and Comparator

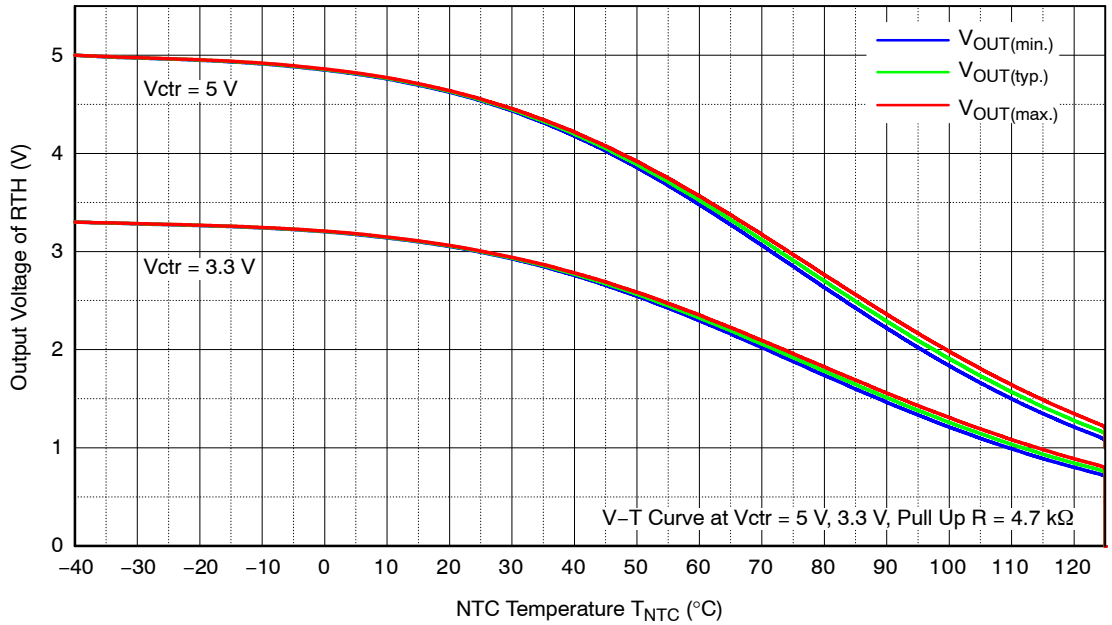


Figure 25. V – T Curve of Figure 24. Pull Up R = 4.7 kΩ

Table 3. THERMISTOR CHARACTERISTICS (BUILT−IN ONLY IN −T TYPE)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{25}	Resistance	Tc = 25°C	46.530	47	47.47	kΩ
R_{125}	Resistance	Tc = 125°C	1.320	1.406	1.497	kΩ
–	B−Constant (25 – 50°C)	B	4009.5	4050	4090.5	K
–	Temperature range	–	−40	–	+125	°C

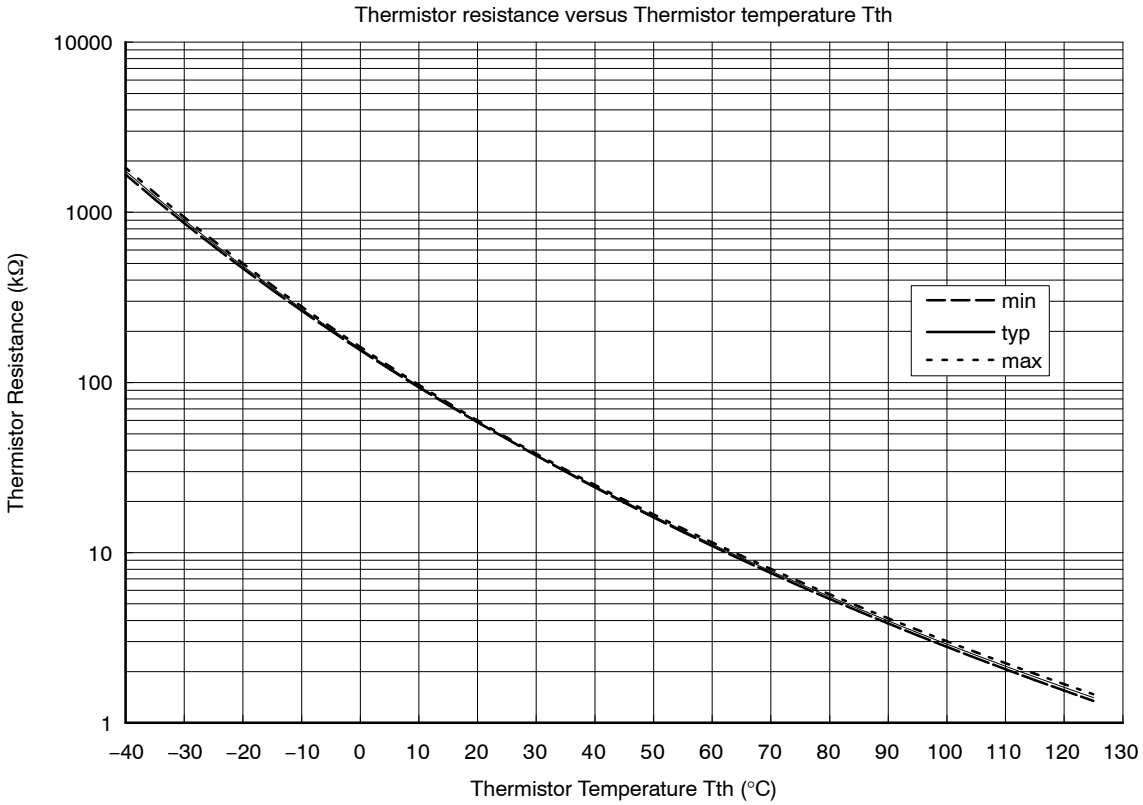


Figure 26. Thermistor Resistance vs. Temperature

Table 4. R−T TABLE OF NTC THERMISTOR

T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)	T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)	T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)
0	153.8063	158.2144	162.7327	42	22.1759	22.6466	23.1249	85	4.4694	4.6736	4.8866
1	146.0956	150.1651	154.3326	43	21.2753	21.7401	22.2129	86	4.3228	4.5226	4.731
2	138.8168	142.5725	146.4152	44	20.4158	20.8746	21.3416	87	4.1817	4.3771	4.5811
3	131.9431	135.4081	138.9502	45	19.5953	20.0478	20.5088	88	4.0459	4.2369	4.4366
4	125.4497	128.6453	131.9091	46	18.812	19.258	19.7126	89	3.915	4.1019	4.2973
5	119.3135	122.2594	125.2655	47	18.0638	18.5032	18.9514	90	3.789	3.9717	4.1629
6	113.5129	116.2273	118.9947	48	17.3492	17.7818	18.2234	91	3.6675	3.8463	4.0334
7	108.0276	110.5275	113.0739	49	16.6663	17.0921	17.5269	92	3.5505	3.7253	3.9084
8	102.8388	105.1398	107.4814	50	16.0137	16.4325	16.8605	93	3.4377	3.6087	3.7879
9	97.9288	100.0454	102.1974	51	15.3899	15.8016	16.2227	94	3.329	3.4963	3.6716
10	93.2812	95.2267	97.2031	52	14.7934	15.1981	15.6122	95	3.2242	3.3878	3.5593
11	88.8803	90.6673	92.481	53	14.223	14.6205	15.0277	96	3.1235	3.2836	3.4515
12	84.7119	86.3519	88.0148	54	13.6773	14.0677	14.4678	97	3.0264	3.183	3.3473
13	80.7624	82.2661	83.7894	55	13.1552	13.5385	13.9316	98	2.9328	3.086	3.2468
14	77.019	78.3963	79.7903	56	12.6556	13.0318	13.4178	99	2.8425	2.9923	3.1497
15	73.47	74.7302	76.0043	57	12.1774	12.5465	12.9255	100	2.7553	2.9019	3.0559
16	70.1042	71.2558	72.4189	58	11.7195	12.0815	12.4536	101	2.6712	2.8146	2.9654
17	66.9112	67.962	69.0224	59	11.281	11.6361	12.0011	102	2.5901	2.7303	2.8779
18	63.8812	64.8386	65.8039	60	10.861	11.2091	11.5673	103	2.5117	2.6489	2.7933
19	61.005	61.8759	62.753	61	10.4594	10.8007	11.152	104	2.436	2.5703	2.7117
20	58.2739	59.0647	59.8601	62	10.0746	10.4091	10.7536	105	2.363	2.4943	2.6327
21	55.6798	56.3961	57.116	63	9.7058	10.0336	10.3714	106	2.2921	2.4206	2.556
22	53.2152	53.8628	54.5127	64	9.3522	9.6734	10.0046	107	2.2236	2.3493	2.4819
23	50.8732	51.4569	52.0422	65	9.0133	9.3279	9.6525	108	2.1575	2.2805	2.4102
24	48.6469	49.1715	49.6969	66	8.6882	8.9963	9.3145	109	2.0936	2.2139	2.3409
25	46.53	47	47.47	67	8.3764	8.6782	8.9899	110	2.0319	2.1496	2.2739
26	44.4567	44.936	45.4159	68	8.0773	8.3727	8.6782	111	1.9725	2.0877	2.2094
27	42.4868	42.9737	43.4618	69	7.7902	8.0795	8.3787	112	1.9151	2.0278	2.147
28	40.6147	41.1075	41.6021	70	7.5147	7.7979	8.091	113	1.8596	1.9699	2.0866
29	38.8351	39.3323	39.8319	71	7.2496	7.5268	7.8138	114	1.806	1.9139	2.0282
30	37.1428	37.6431	38.1463	72	6.995	7.2663	7.5474	115	1.7541	1.8598	1.9716
31	35.5329	36.0351	36.5408	73	6.7505	7.016	7.2913	116	1.7042	1.8076	1.9171
32	34.0011	34.5041	35.0111	74	6.5157	6.7755	7.045	117	1.6559	1.7572	1.8644
33	32.5433	33.0462	33.5534	75	6.2901	6.5443	6.8082	118	1.6092	1.7083	1.8134
34	31.1555	31.6573	32.164	76	6.0739	6.3227	6.581	119	1.564	1.6611	1.7639
35	29.834	30.3339	30.8392	77	5.8662	6.1096	6.3624	120	1.5203	1.6153	1.7161
36	28.576	29.0734	29.5764	78	5.6665	5.9046	6.1521	121	1.4777	1.5707	1.6694
37	27.3776	27.8717	28.372	79	5.4745	5.7075	5.9498	122	1.4365	1.5276	1.6242
38	26.2356	26.726	27.2228	80	5.2899	5.5178	5.7549	123	1.3966	1.4858	1.5804
39	25.1472	25.6332	26.1261	81	5.1129	5.3358	5.568	124	1.358	1.4453	1.538
40	24.1094	24.5907	25.0792	83	4.7788	4.9921	5.2145	125	1.3206	1.406	1.4969
41	23.1198	23.596	24.0796	84	4.6211	4.8299	5.0475				

Selection of Shunt Resistor

Figure 27 shows an example circuit of the SC protection using 1−shunt resistor. The line current on the N side DC−ink is detected and the protective operation signal is passed through the RC filter. If the current exceeds the SC reference level, all the gates of the N−side three−phase IGBTs are switched to the off state and the VFO fault signal is transmitted to MCU. Since SC protection is non−repetitive, IGBT operation should be immediately halted when the VFO fault signal is given.

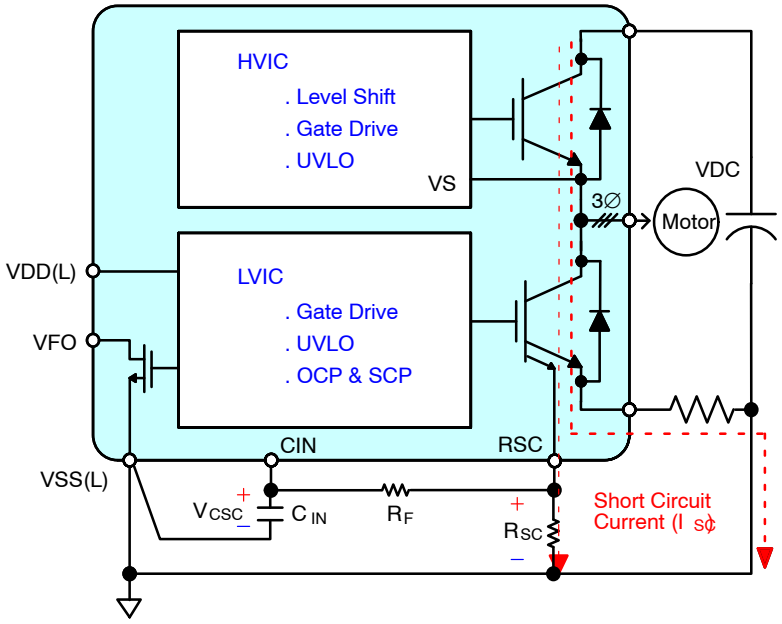


Figure 27. Short Circuit Current Protection Circuit with One Shunt Resistor

The value of shunt resistor is calculated by the following equation.
Maximum over current trip level: $I_{OC(max)}$ = 1.5 x I_C (rated current)
SC trip referenced voltage: V_{SC} = min. 0.45 V, typ. 0.48 V, max. 0.51 V
Shunt resistance: $I_{SC(max)} = V_{SC(max)} / R_{SHUNT(min)} \rightarrow R_{SHUNT(min)} = V_{SC(max)} / I_{SC(max)}$
If the deviation of shunt resistor should is limited below ±5 %,
$R_{SHUNT(typ)} = R_{SHUNT(min)} / 0.95$, $R_{SHUNT(max)} = R_{SHUNT(typ)}$ x 1.05
Actual SC trip current level becomes:
$I_{SC(typ)} = V_{SC(typ)} / R_{SHUNT(min)}$, $I_{SC(min)} = V_{SC(min)} / R_{SHUNT(max)}$
Inverter output power:
$P_{OUT} = \sqrt{3}$ x VO,LL x $I_{O(RMS)}$ x PF
Where:
VO,LL = ($\sqrt{3}$ / $\sqrt{2}$) x MI x (V_{DC} / 2)
I(O)RMS = Maximum load current of inverter; and
MI = Modulation Index;
VDC = DC link voltage;
PF = Power Factor
Average DC Current
$I_{DC\_AVG} = V_{DC\_Link} / (P_{out}$ x Eff)
Where:
Eff = Inverter Efficiency
The power rating of shunt resistor is calculated by the following equation.
$P_{SHUNT} = (I^2_{RMS}$ x R_{SHUNT} x Margin) / De−rating Ratio
Where:
Shunt resistor typical value at T_C=25°C (R_{SHUNT})
De−rating ratio of shunt resistor at T_{SHUNT} = 100°C (From datasheet of shunt resistor)
Safety margin (Determine by customer)

The value of shunt resistor calculation examples:
DUT: NFAL5065L4B(T)
Tolerance of shunt resistor: ±5%
Over Current Trip Reference Voltage:
$Vsc(ref)\_{min}$ = 0.45 V, $Vsc(ref)\_{typ}$ = 0.50 V, $Vsc(ref)\_{max}$ = 0.55 V
Maximum Load Current of Inverter (I_{RMS}): 35 A_{rms}
Maximum Peak Load Current of Inverter ($I_{C(max)}$): 75 A
Modulation Index (MI): 0.9
DC Link Voltage (V_{DC_Link}): 300 V
Power Factor (PF): 0.8
Inverter Efficiency (Eff): 0.95
Shunt Resistor Value at T_C = 25°C (R_{SHUNT}): 7 mΩ
De−rating Ration of Shunt Resistor at T_{SHUNT} = 100°C: 70 % (refer to Figure 28)
Safety Margin: 20%

Calculation results:
$I_{SC(max)}$: 1.5 x $I_{C(max)}$ = 1.5 x 50 A = 75 A
$R_{SHUNT(typ)}$: $Vsc(ref)\_{typ}$ / $I_{SC(max)}$ = 0.48 V / 75 A = 6.4 mΩ
$R_{SHUNT(max)}$: $R_{SHUNT(max)}$ x 1.05 = 6.4 mΩ x 1.05A = 6.72 mΩ
$R_{SHUNT(min)}$: $R_{SHUNT(min)}$ x 0.95 = 6.4 mΩ x 0.95 A = 6.08 mΩ
$I_{SC(min)}$: $Vsc(ref)\_{min}$ / $R_{SHUNT(max)}$ = 0.45 V / 6.72 mΩ = 67 A
$I_{SC(max)}$: $Vsc(ref)\_{max}$ / $R_{SHUNT(min)}$ = 0.51 V / 6.08 mΩ = 84 A
P_{OUT} = √3 x ((√3 / √2) x MI x (V_{DC} / 2)) x $I_{(O)RMS}$ x PF = (3 / √2) x 0.9 x (300 / 2) x 35 x 0.8 = 8019 W
I_{DC_AVG} = (P_{OUT} / Eff) / V_{DC_Link} = 28.14 A
P_{SHUNT} = ($I^2_{DC\_AVG}$ x R_{SHUNT} x Margin) / De−rating Ratio = (28.14^2 x 0.0065 x 1.2) / 0.7 = 8.8 W (therefore, the proper power rating of shunt resistor is over 9 W).

When over−current events are detected, the 650 V Motion SPM 49 series shuts down all low−side IGBTs and sends out the fault−out (VFO) signal. FAULT output timer operation start with internal delay (typ. 2.4 ms, CFOD = 22 nF), Fault−out duration time is controlled by CFOD. To prevent malfunction, it is recommended that an RC filter be inserted at the CIN pin. To shut down IGBTs within 3 μs when over−current situation occurs, a time constant of 0.75~1.25 μs is recommended. Table 5 shows the shunt resistance and typical short−circuit protection current.

Table 5. OVER−CURRENT (OC) PROTECTION TRIP LEVEL

Device	R_{SHUNT}	OC Trip Level	Remark
NFAL3065L4B(T)	16.0 mΩ	30 A	It is typical value
NFAL5065L4B(T)	10.7 mΩ	45 A	
NFAL7565L4B(T)	4.4 mΩ	110 A	

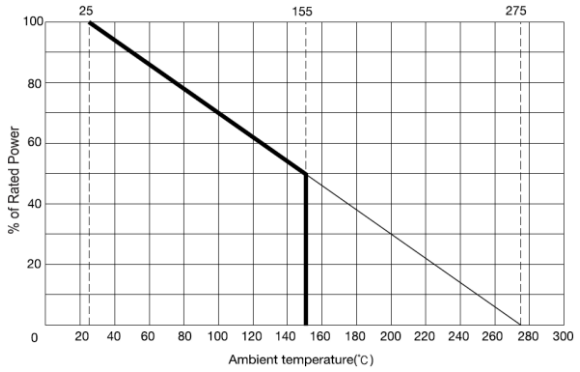


Figure 28. De−rating Curve Example of Shunt Resistor (from RARA Elec.)

Time Constant of Internal Delay

An RC filter is prevents noise−related over and short circuit current protection (OCP, SCP) circuit malfunction. The RC time constant is determined by the applied noise filter time and the Short−Circuit Withstanding Time (SCWT) of SPM 49 version series.

When the R_{shunt} voltage exceeds the VSC(ref) level, this is applied to the CIN pin via the RC filter. The RC filter delay is the time required for the CIN pin voltage to rise to the referenced OCP & SCP level. The LVIC has an internal filter time (logic filter time for noise elimination: around 0.85 μs). Consider this filter time when designing the RC filter of CIN pin. Figure 29 shows actual real time at over and short circuit current protection. Each time sections have a distribution, so we have to consider of distribution.

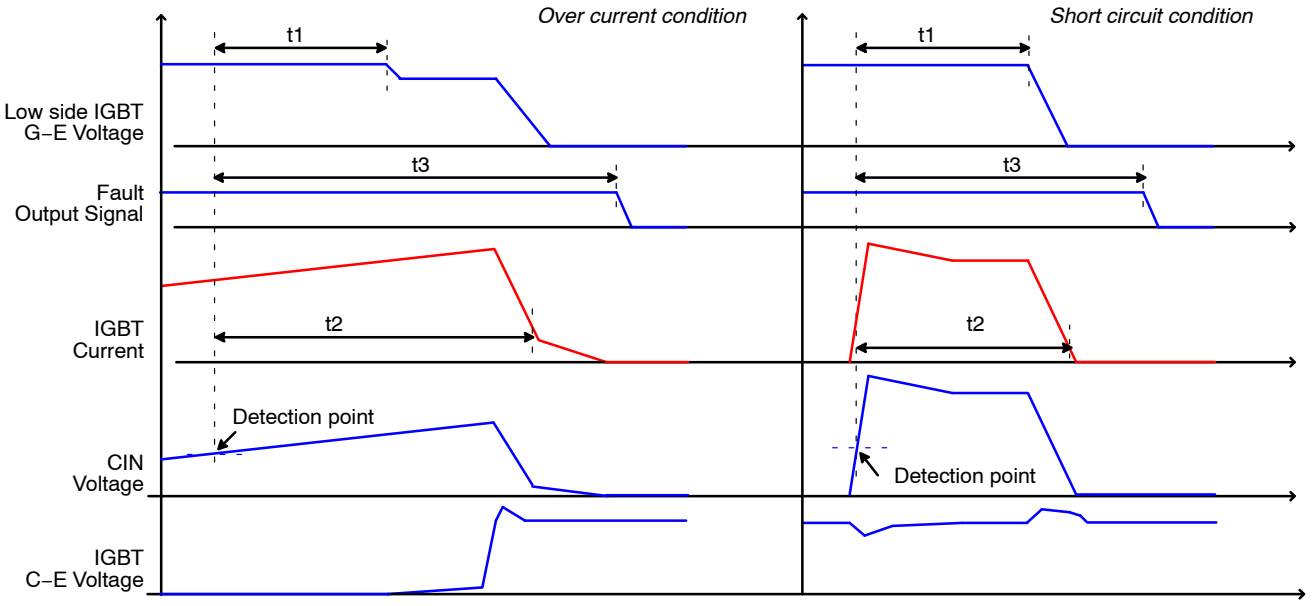


Figure 29. Timing Diagram of Over and Short Circuit Protection

Table 6. TIME TABLE OF OVER AND SHORT CIRCUIT CONDITIONS; VSC(ref) TO LOW SIDE GATE, COLLECTOR CURRENT AND VFO

Ref. Condition VDCbus = 300 V, VDD = 15 V		Over Current Condition. 2 * I Rating						Short Circuit Condition					
		t1 [μs]		t2 [μs]		t3 [μs]		t1 [μs]		t2 [μs]		t3 [μs]	
Device	**T_J [°C]**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**
NFAL3065L4B(T)	*25*	1.05	1.30	TBD	TBD	4.0	5.0	1.05	1.30	TBD	TBD	4.0	5.0
	150	1.0	1.25	TBD	TBD	3.2	4.2	1.0	1.25	TBD	TBD	3.2	4.2
NFAL5065L4B(T)	*25*	1.05	1.30	1.45	1.75	4.0	5.0	1.05	1.30	1.3	1.6	4.0	5.0
	150	1.0	1.25	1.35	1.65	3.2	4.2	1.0	1.25	1.25	1.55	3.2	4.2
NFAL7565L4B(T)	*25*	1.05	1.30	1.6	1.9	4.0	5.0	1.05	1.30	1.45	1.75	4.0	5.0
	150	1.0	1.25	1.5	1.8	3.2	4.2	1.0	1.25	1.35	1.55	3.2	4.2

29. To guarantee safe short−circuit protection under all operating conditions, CIN should be triggered within 1.0 μs after short−circuit occurs. (Recommendation: SCWT < 3.0 μs, Conditions: VDC = 400 V, VDD = 16.5 V, Tj = 150°C).

It is recommended that delay from short−circuit to CIN triggering should be minimized.

1. t1: from CIN detection to gate driver LO shut down
2. t2: from CIN detection to collector current 10%
3. t3: from CIN detection to fault out signal activation

Fault Output Circuit

Because VFO terminal is an open−drain type; it should be pulled up via a pull−up resistor.

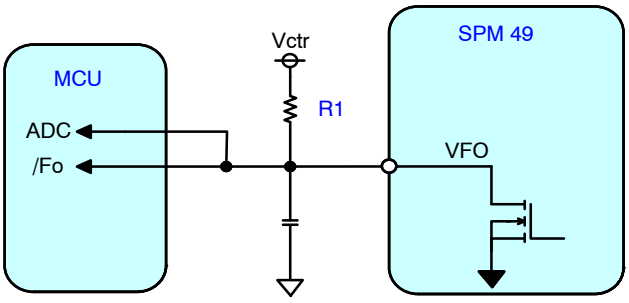


Figure 30. Voltage−Current Characteristics of VFO Terminal

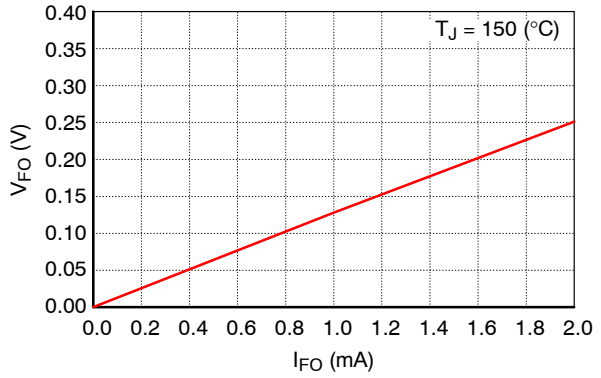


Figure 31. Voltage−Current Characteristics of VFO Terminal

Circuit of Input Signal (HINx, LINx)

Figure 32 shows recommended I/O interface circuit between the MCU and SPM 49. Because SPM 49 input logic is active HIGH and there are built−in pull−down resistors, external pull−down resistors are not needed.

The input and fault output maximum rated voltages are shown in Table 18. Since the fault output is open drain and its rating is VDD + 0.5 V, 15 V supply interface is possible.

However, it is recommended that the fault output be configured with the 5 V logic supplies, which is the same as the input signals. It is also recommended that the decoupling capacitors be placed at both the MCU and Motion SPM 49 ends of the VFO signal line, as close as possible to each device. The RC coupling at each input (parts shown dotted in Figure 32) can be changed depending on the PWM control scheme used in the application and the wiring impedance of the PCB layout.

The input signal section of the Motion SPM 49 series integrates a 5 kΩ (typical) pull−down resistor. Therefore, when using an external filtering resistor between the MCU output and the Motion SPM 49 input, attention should be given to the signal voltage drop at the Motion SPM 49 input terminals to satisfy the turn on threshold voltage requirement. For instance, R = 100 Ω and C = 1 nF for the parts shown dotted in Figure 32.

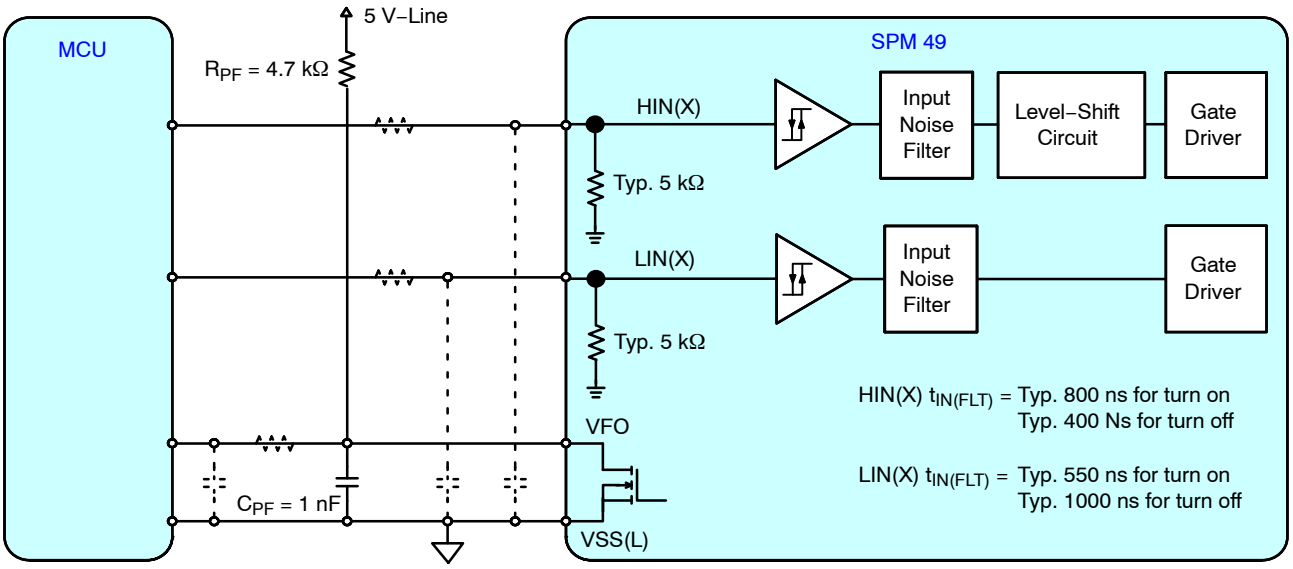


Figure 32. Recommended MCU I/O Interface Circuit

Bootstrap Circuit Design

Operation of Bootstrap Circuit

The V_{BS} voltage, which is the voltage difference between VB(X) and VS(X), provides the supply to the HVIC within the 650 V SPM 49 series. This supply must be in the range of 13.0 V~18.5 V to ensure that the HVIC can fully drive the high−side IGBT. The SPM 49 series includes an under−voltage lock out protection function for the V_{BS} to ensure that the HVIC does not drive the high−side IGBT, if the V_{BS} voltage drops below a specified voltage. This function prevents the IGBT from operating in a high dissipation mode. There are a number of ways in which the VBS floating supply can be generated. One of them is the bootstrap method described here (refer to Figure 33). This method has the advantage of being simples and inexpensive. However, the duty cycle and on−time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap to ground (either through the low−side or the load), the bootstrap capacitor (C_{BOOT}) is charged through the bootstrap diode (D_{BOOT}) and the resistor (R_{BOOT}) from the VDD supply.

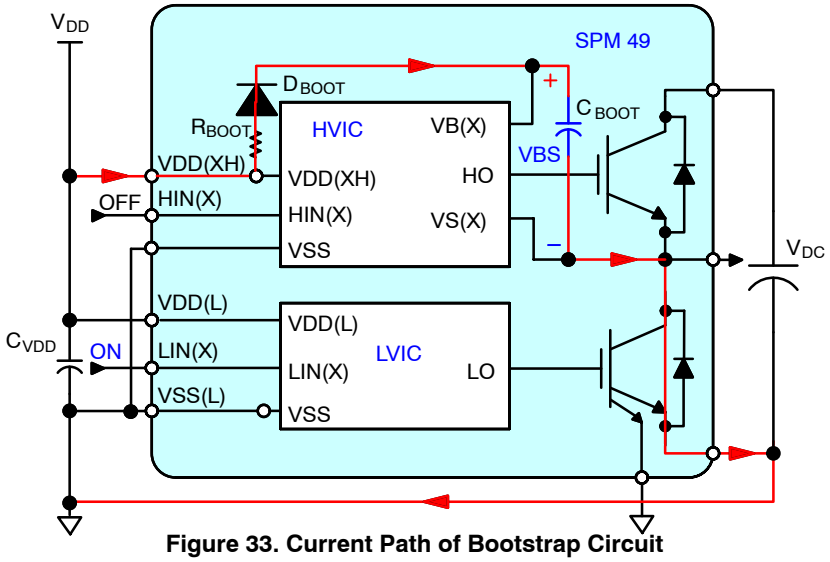


Figure 33. Current Path of Bootstrap Circuit

Selection of Bootstrap Capacitor Considering Initial Charging

Adequate on−time of the low−side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated by:

$$t_{charge} = C_{BOOT} \times R_{BOOT} \times \frac{1}{\delta} \times \ln \frac{V_{DD}}{VDD - VBS(min.) - VF - VLS} \quad \text{(eq. 1)}$$

Where:

VF = Forward voltage drop across the bootstrap diode;

VBS(min.) = The minimum value of the bootstrap capacitor;

VLS = Voltage drop across the low−side IGBT or load; and

Δ = Duty ratio of PWM.

When the bootstrap capacitor is charged initially; VDD drop voltage is generated based on initial charging method, VDD line SMPS output current, VDD source capacitance, and bootstrap capacitance. If VDD drop voltage reaches UVDDD level, the low side is shut down and a fault signal is activated.

To avoid this malfunction, related parameter and initial charging method should be considered. To reduce VDD voltage drop at initial charging, a large VDD source capacitor and selection of optimized low−side turn−on method are recommended. Adequate on−time duration of the low−side IGBT to fully charge the bootstrap capacitor is initially required before normal operation of PWM starts.

Figure 34 shows an example of initial bootstrap charging sequence. Once VDD establishes, VBS needs to be charged by turning on the low−side IGBTs. PWM signals are typically generated by an interrupt triggered by a timer with a fixed interval, based on the switching carrier frequency.

Therefore, it is desired to maintain this structure without creating complementary high−side PWM signals. The capacitance of VDD should be sufficient to supply necessary charge to VBS capacitance in all three phases. If a normal PWM operation starts before VBS reaches UVLO reset level, the high−side IGBTs cannot switch without creating a fault signal. It may lead to a failure of motor start in some applications. If three phases are charged synchronously, initial charging current through a single shunt resistor may exceed the over−current protection level.

Therefore, initial charging time for bootstrap capacitors should be separated, as shown in Figure 35. The effect of the bootstrap capacitance factor and charging method (low−side IGBT driving method) is shown in Figure 36.

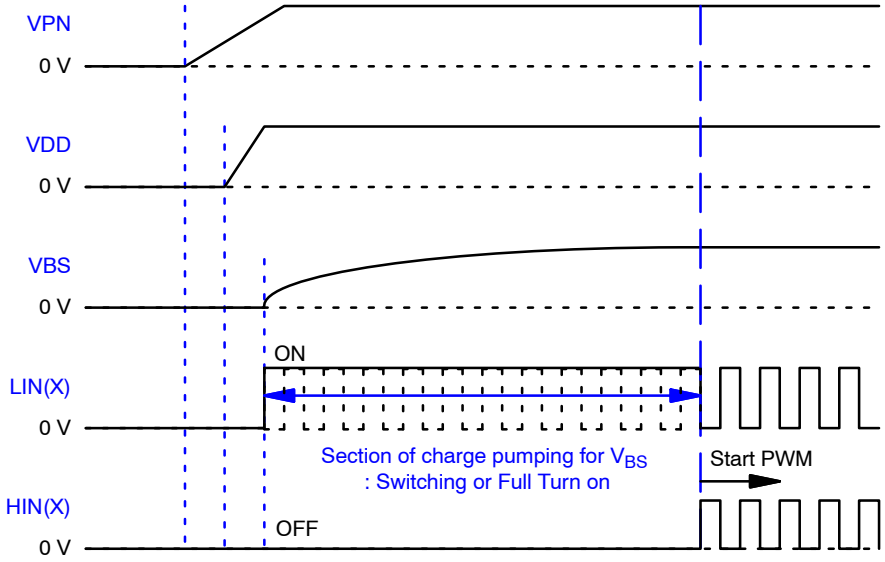


Figure 34. Timing Chart of Initial Bootstrap Charging

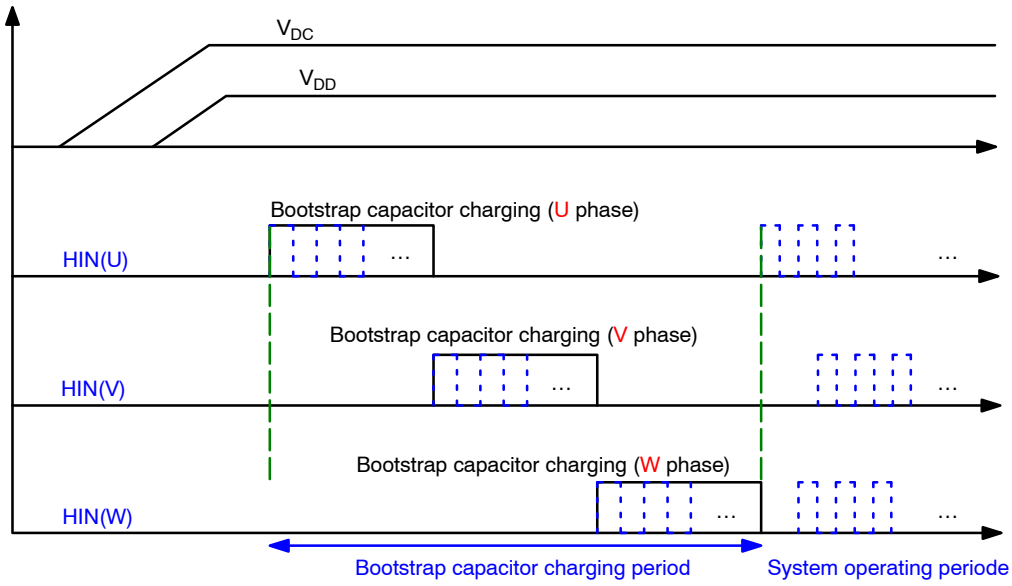


Figure 35. Recommended Initial Bootstrap Capacitors Charging Sequence

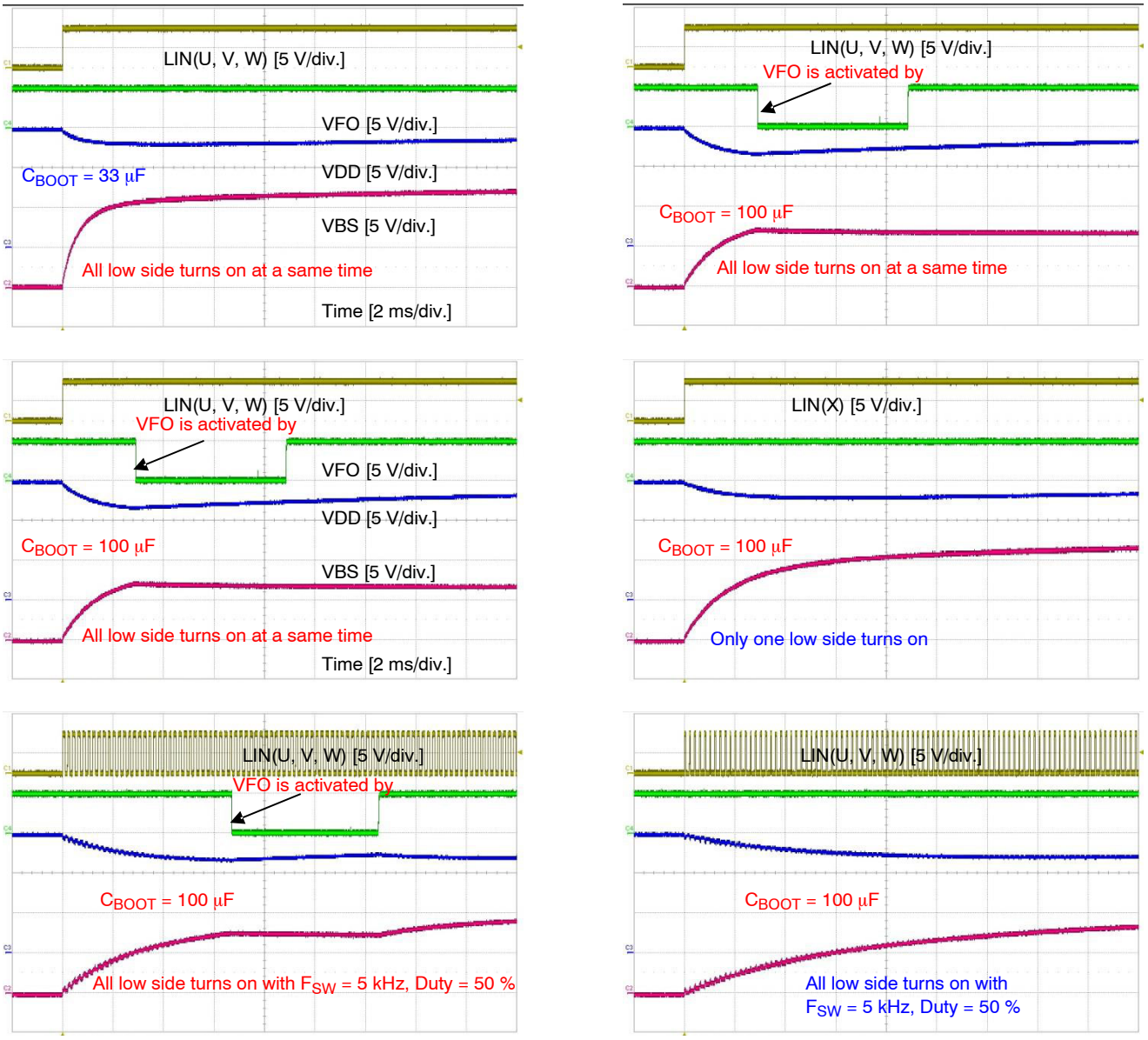


Figure 36. Initial Charging According to Bootstrap Capacitance and Charging Method (Ref. Condition: VDD = 15 V / 300 mA, VDD Capacitor = 220 μF, C_{BOOT} = 100 μF, R_{BOOT} = 20 Ω)

Selection of Bootstrap Capacitor Considering Operating

The bootstrap capacitance can be calculated by:

$$C_{BOOT} = \frac{I_{leak} \times \Delta t}{\Delta VBS} \quad \text{(eq. 2)}$$

Where:

Δt: maximum on pulse width of high−side IGBT;

ΔVBS: the allowable discharge voltage of the C_{BOOT} (voltage ripple); and

ILeak: maximum discharge current of the C_{BOOT}.

Mainly via the following mechanisms:

Gate charge for turning the high−side IGBT on.

Quiescent current to the high−side circuit in HVIC.

Level−shift charge required by level−shifters in HVIC.

Leakage current in the bootstrap circuit.

C_{BOOT} capacitor leakage current (ignored for non−electrolytic capacitors).

Bootstrap diode reverse recovery charge.

Practically, 6.5 mA of I Leak is recommended for the 650 V SPM 49 series. By considering dispersion and reliability, the capacitance is generally selected to be 2~3 times the calculated one. The C_{BOOT} is only charged when the high−side IGBT is off and the VS(x) voltage is pulled down to ground.

The on−time of the low−side IGBT must be sufficient to for the charge drawn from the C_{BOOT} capacitor to be fully replenished. This creates an inherent minimum on−time of the low−side IGBT (or off−time of the high−side IGBT).

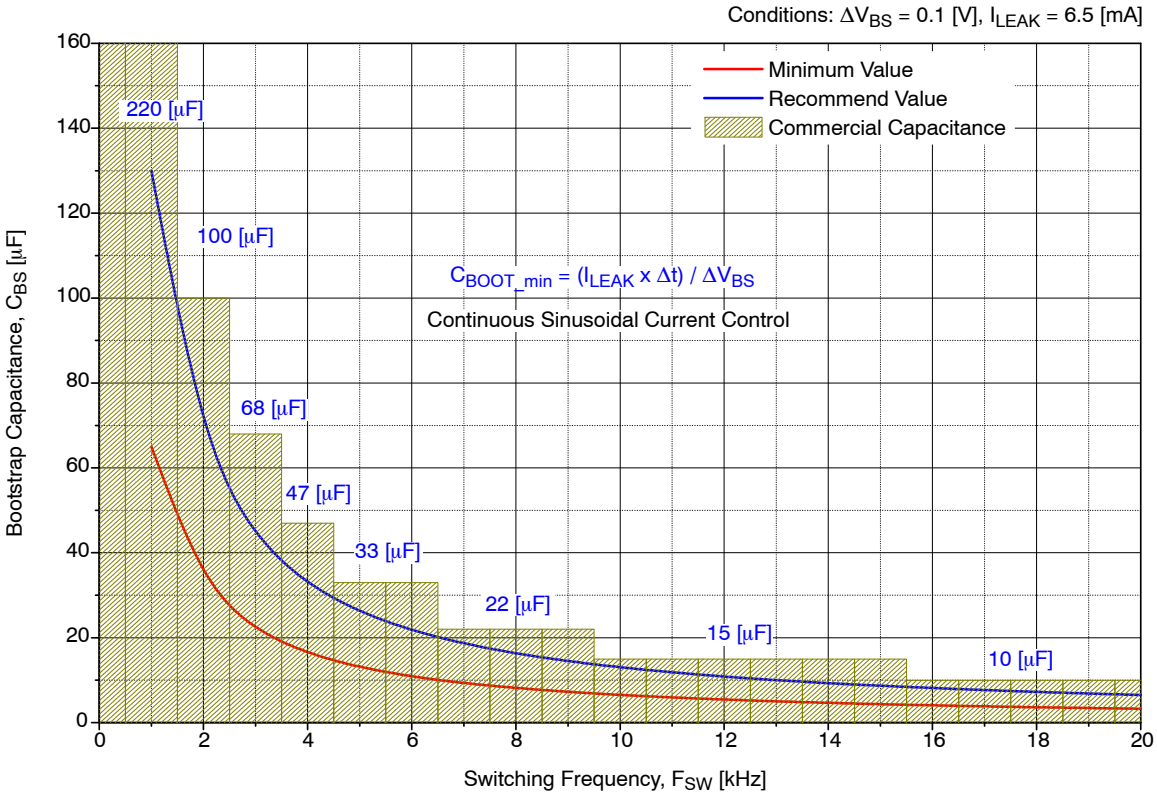


Figure 37. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

Based on switching frequency and recommended ΔVBS.

I_{Leak}: circuit current = 6.5 mA (recommended value)

ΔVBS: discharged voltage = 1.0 V (recommended value)

Δt: maximum on pulse width of high−side IGBT = 0.2 ms (depends on application)

$C_{BOOT\_min} = ((I_{leak} \times \Delta t) / \Delta V_{BS}) = ((6.5\ mA \times 0.2\ ms) / 1.0\ V) = 9 \times 10^{-6}$

→ More than 2 times → 26 μF. (33 μF STD value)

NOTE: The capacitance value can be changed according to the switching frequency, the capacitor selected, and the recommended VBS voltage of 13.0~18.5 V (from datasheet). The above result is just a calculation example. This value can be changed according to the actual control method and lifetime of the component.

Built−in Bootstrap Circuit

When the low−side IGBT or diode conducts, the bootstrap diode (D_{BOOT}) supports the entire bus voltage. Hence, a diode with withstand voltage of more than 650 V is recommended. It is important that this diode has a fast recovery (recovery time < 100 ns) characteristic to minimize the amount of charge fed back from the bootstrap capacitor into the VDD supply. The bootstrap resistor (R_{BOOT}) is to slow down the dVBS/dt and limit initial charging current (I_{charge}) of bootstrap capacitor.

Normally, a bootstrap circuit consists of bootstrap diode (D_{BOOT}), bootstrap resistor (R_{BOOT}), and bootstrap capacitor (C_{BOOT}). As shown in Figure 39, the built−in bootstrap circuit of SPM 49 product has series resistor to be used without additional bootstrap resistor. Therefore, only external bootstrap capacitors are needed to make bootstrap circuit.

The characteristics of the built−in bootstrap diode in the SPM 49 products are:

Fast recovery diode: 650 V / 2 A

Resistive characteristic: equivalent resistor of approximately 15.5 Ω

Table 7 shows the specification of bootstrap circuit. Figure 39 shows forward voltage drop and reverse recovery characteristic of the bootstrap diode.

Table 7. SPECIFICATION FOR INTEGRATED BOOTSTRAP CIRCUIT

Symbol	Parameter	Conditions	Typ	Unit
VF	Forward−Drop Voltage	I_F = 0.1 A, T_C = 25°C	2.2	V
RBOOT	Bootstrap Resistor		15.5	Ω

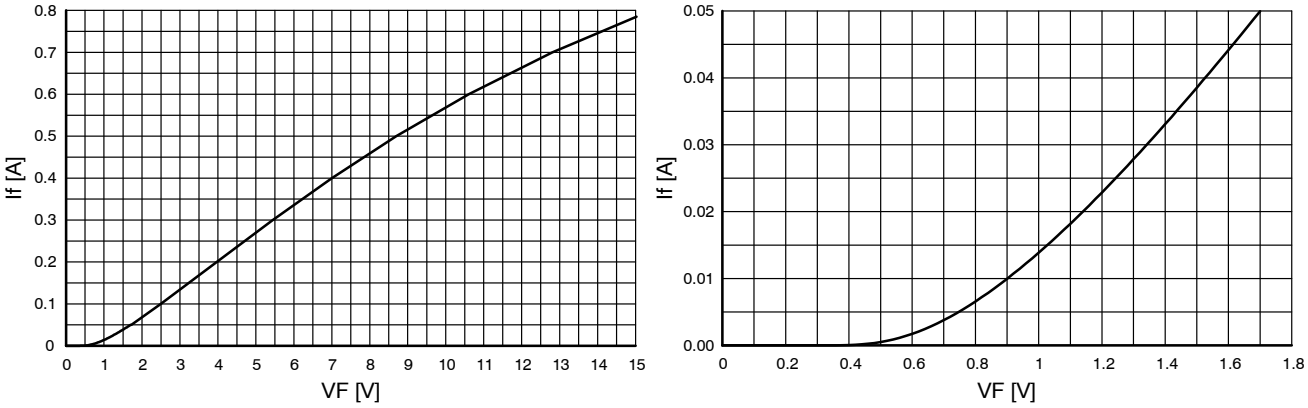


Figure 38. V−I characteristics of Bootstrap Circuit in SPM 49 Series Products (Right: Zoom in Figure)

PRINT CIRCUIT BOARD (PCB) DESIGN

General Application Circuit Example

Figure 39 shows a general application circuitry of interface schematic with control signals connected directly to a MCU. Figure 40 shows guidance of PCB layout for the 650 V SPM 49 series.

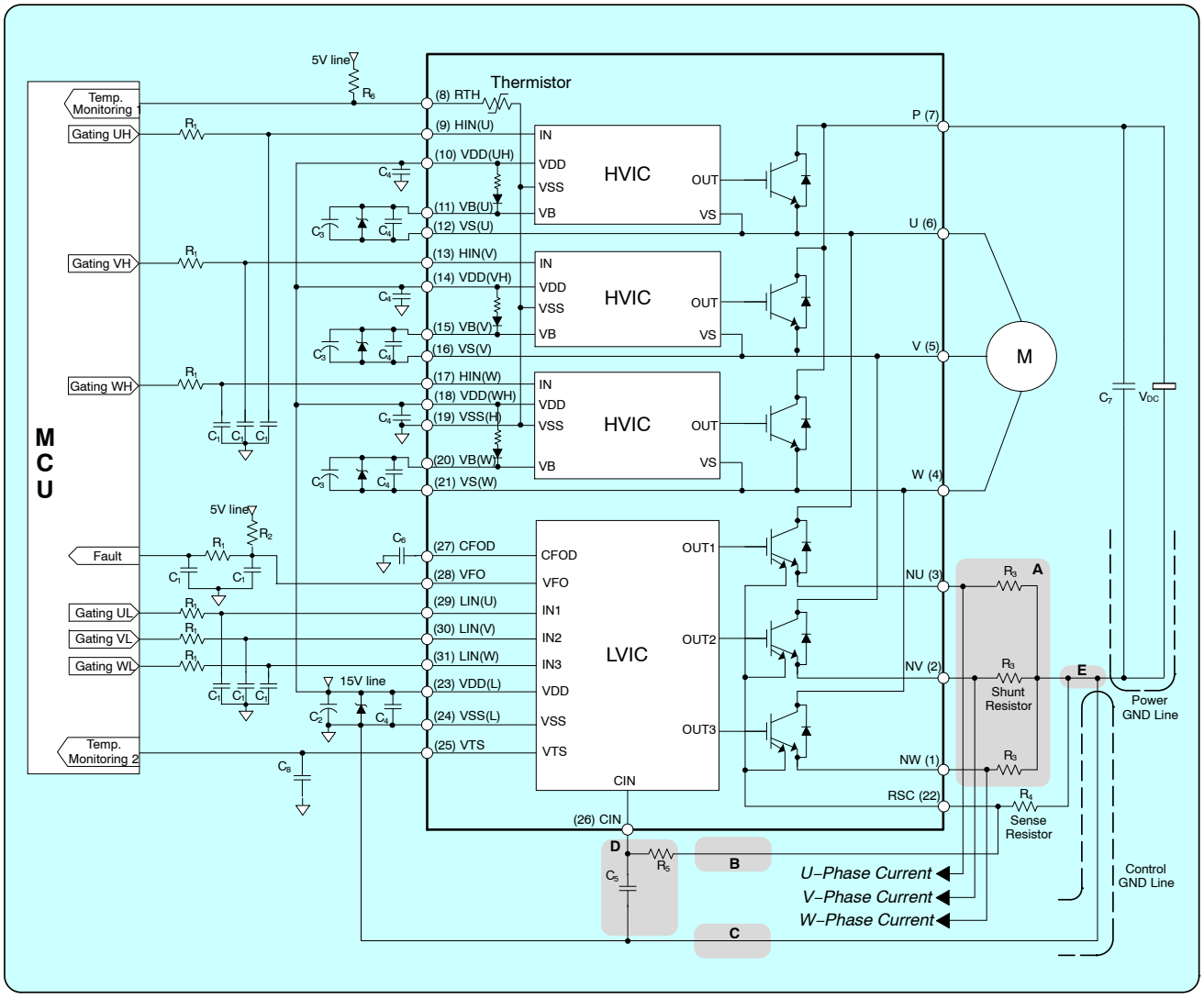


Figure 39. General Application Circuitry for 650 V Motion SPM 49

PCB Layout Guidance

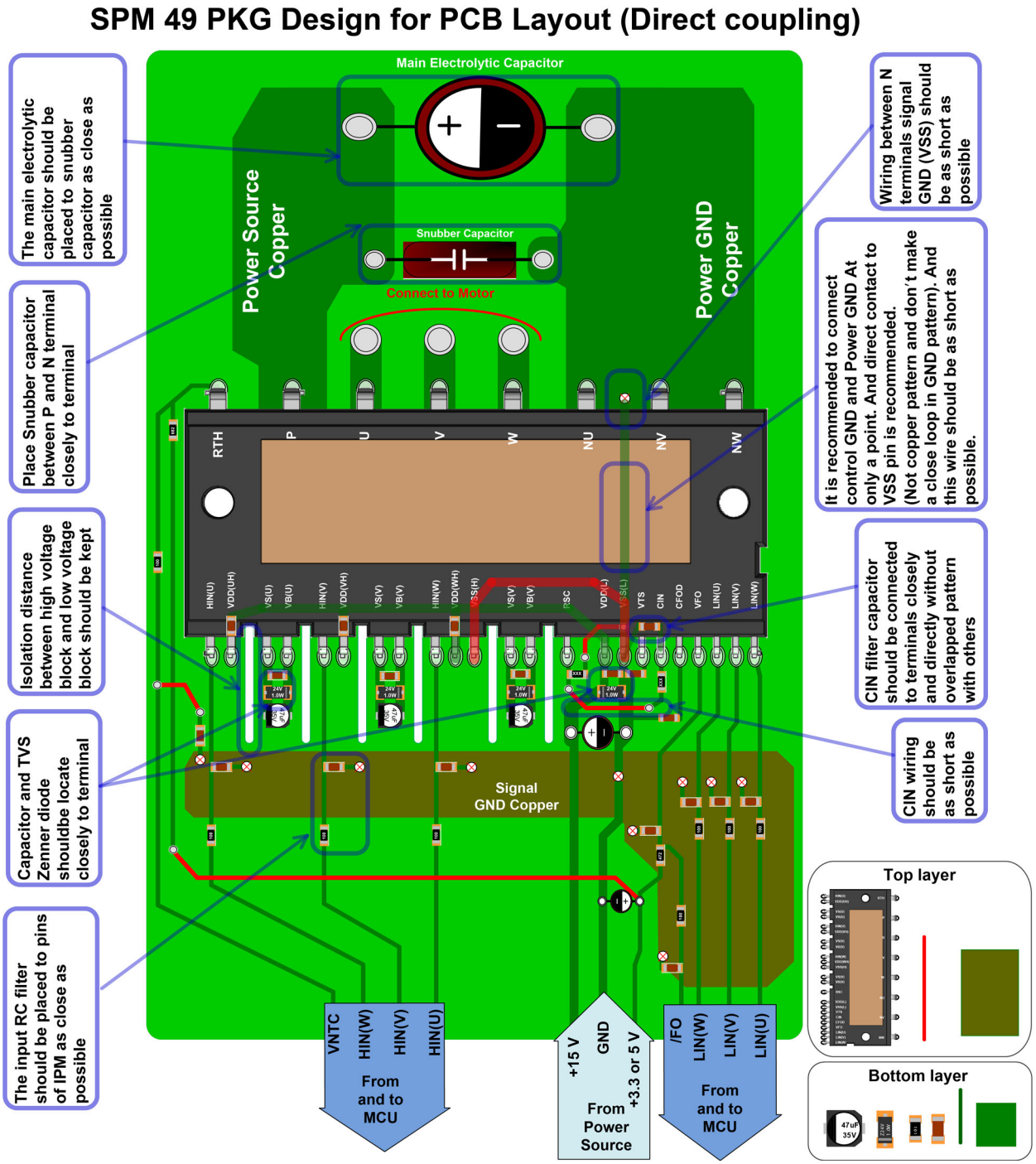


Figure 40. Print Circuit Board (PCB) Layout Guidance for SPM 49 Series

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