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CMOS 8-BIT MICROCONTROLLER

LC872R00 SERIES USER'S MANUAL

REV : 1.00

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ON Semiconductor
Digital Solution Division
Microcontroller & Flash Business Unit

Contents

Contents

Contents

1. Overview

1.1 Overview

The LC872R00 series is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3 ns, integrates on a single chip a number of hardware features such as 4K-byte flash ROM (onboard programmable) or mask ROM, 128-byte RAM, a sophisticated 16-bit timer/counter (may be divided into 8-bit timers), two 8-bit timers with a prescaler, an asynchronous/synchronous SIO interface, a 12-bit 8-channel AD converter with 12-/8-bit resolution selector, a system clock frequency divider, an internal reset circuit, and 12-source 8-vector interrupt feature.

1.2 Features

● ROM

- Flash ROM version

  LC87F2R04A: 4096 × 8 bits

  - Capable of onboard programming with a wide range of supply voltages: 2.2 to 5.5V.
  - Block erasable in 128-byte units
  - Data can be written in 2-byte units

- Mask ROM version

  LC872R04A: 4096 × 8 bits

● RAM

- 128 × 9 bits

● Minimum bus cycle time

- 83.3 ns (12 MHz, VDD = 2.7 to 5.5V)
- 100 ns (10 MHz, VDD = 2.2 to 5.5V)

  Note: The bus cycle time here refers to the ROM read speed.

● Minimum instruction cycle time (Tcyc)

- 250 ns (12 MHz, VDD = 2.7 to 5.5V)
- 300 ns (10 MHz, VDD = 2.2 to 5.5V)

● Ports

- Normal withstand voltage I/O ports

  Ports whose I/O direction can be designated in 1-bit units: 11 (P1n, P20, P21, P70)

  Ports whose I/O direction can be designated in 4-bit units: 8 (P0n)
- Dedicated oscillator/input ports: 2 (CF1/XT1, CF2/XT2)
- Reset pin: 1 ($\overline{\text{RES}}$)
- Power pins: 2 (VSS1, VDD1)

● Timers

● Timer 0: 16-bit timer/counter with a capture register

Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels

Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)

Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)

Mode 3: 16-bit counter (with a 16-bit capture register)

● Timer 6: 8-bit timer with a 6-bit prescaler (with toggle output)

● Timer 7: 8-bit timer with a 6-bit prescaler (with toggle output)

● SIO

● SIO1: 8-bit asynchronous/synchronous serial interface

Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 Tcyc transfer clock)

Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 Tcyc baudrate)

Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 Tcyc transfer clock)

Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)

● AD converter: 12 bits × 8 channels

- 12-/8- bit AD converter resolution selectable.

● Remote control receiver circuit (multiplexed with P15/SCK1/INT3/T0IN pin)

- Noise filtering function (noise filter time constant selectable from among 1Tcyc, 32Tcyc, and 128Tcyc.)

● Watchdog timer

1) External RC watchdog timer
2) Interrupt or a reset signal selectable

● Interrupts

● 12 sources, 8 vector addresses

1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt request of the level equal to or lower than the current interrupt is not accepted.
2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address is given priority.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3
5	00023H	H or L	T0H
6	0002BH	H or L	None
7	00033H	H or L	None
8	0003BH	H or L	SIO1
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0

- Priority levels: X > H > L
- When interrupts of the same level occur at the same time, an interrupt with the smallest vector address is given priority.

- **Subroutine stack levels: Up to 64 levels (stack is allocated in RAM)**

- **High-speed multiplication/division instructions**
  - 16 bits × 8 bits (5 Tcyc execution time)
  - 24 bits × 16 bits (12 Tcyc execution time)
  - 16 bits ÷ 8 bits (8 Tcyc execution time)
  - 24 bits ÷16 bits (12 Tcyc execution time)

- **Oscillator circuits**

  - **Internal oscillator circuits**
    1) Medium-speed RC oscillator circuit: For system clock (1 MHz)
    2) Variable modulation frequency RC oscillator circuit: For system clock (8 MHz)

  - **External oscillator circuit**
    1) High-speed CF oscillator circuit: For system clock, with internal Rf
       <1> The CF oscillator circuit stops operation on a system reset. When the reset is released, the CF oscillator circuit resumes operation.

- **System clock dividing function**
  - Can run on low current.
  - The minimum instruction cycle can be selected from among 300 ns, 600 ns, 1.2 μs, 2.4 μs, 4.8 μs, 9.6 μs, 19.2 μs, 38.4 μs, and 76.8 μs (at a main clock rate of 10 MHz).

- **Internal reset circuits**

  - **Power-on reset (POR) function**
    1) POR reset is generated only at power-on time.
    2) The POR release level can be selected from among 8 levels (1.67V, 1.97V, 2.07V, 2.37V, 2.57V, 2.87V, 3.86V, and 4.35V) by configuring options.

  - **Low-voltage detection reset (LVD) function**
    1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
    2) The use/disuse of the LVD function and the low voltage threshold level (7 levels: 1.91V, 2.01V, 2.31V, 2.51V, 2.81V, 3.79V, and 4.28V) can be changed by configuring options.

- **Standby function**

  - **HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation**
    1) Oscillation is not stopped automatically.
    2) There are four ways of releasing HALT mode.
       <1> Setting the reset pin to a low level
       <2> Reset caused by low voltage detection
       <3> Reset caused by watchdog timer
       <4> Generating an interrupt

  - **HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.**
    1) The CF and the medium-speed RC oscillators automatically stop operation.
    2) There are five ways of releasing HOLD mode.
       <1> Setting the reset pin to the low level.
       <2> Reset caused by low voltage detection
       <3> Reset caused by watchdog timer

<4> Establishing an interrupt source at one of the INT0, INT1, INT2, and INT4 pins.
* INT0 and INT1 HOLD mode release is available only when level detection is set.
<5> Establishing an interrupt source at port 0

● On-chip debugger function (flash ROM version)

- Supports software debugging with the microcontroller mounted on the target board.
- There are two channels of on-chip debugger pins to support small pin count devices.
  DBGP0(P0), DBGP1(P1)

● Data security function (flash ROM version)

- Protects the program data stored in flash memory from unauthorized read or copy.

Note: This data security function does not necessarily provide absolute data security.

● Package form

- MFP24S (300 mil) (lead-free and halogen-free product)
- SSOP24 (225 mil) (lead-free and halogen-free product)

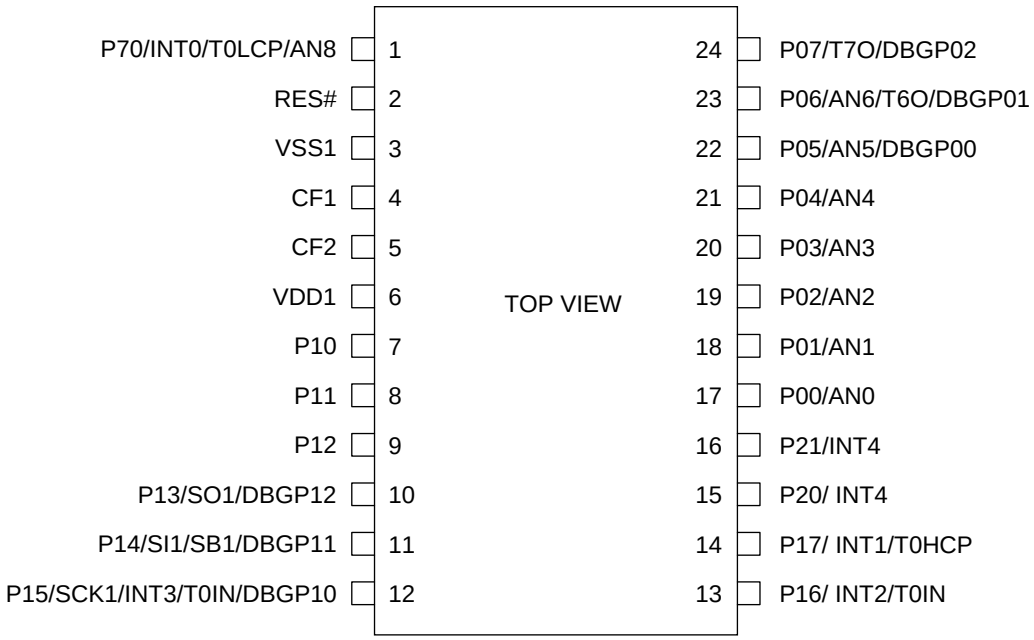
● Development tools

- On-chip debugger: TCB87 Type B + LC87F2R04A
  : TCB87 Type C (3-wire configuration) + LC87F2R04A

● Programming board

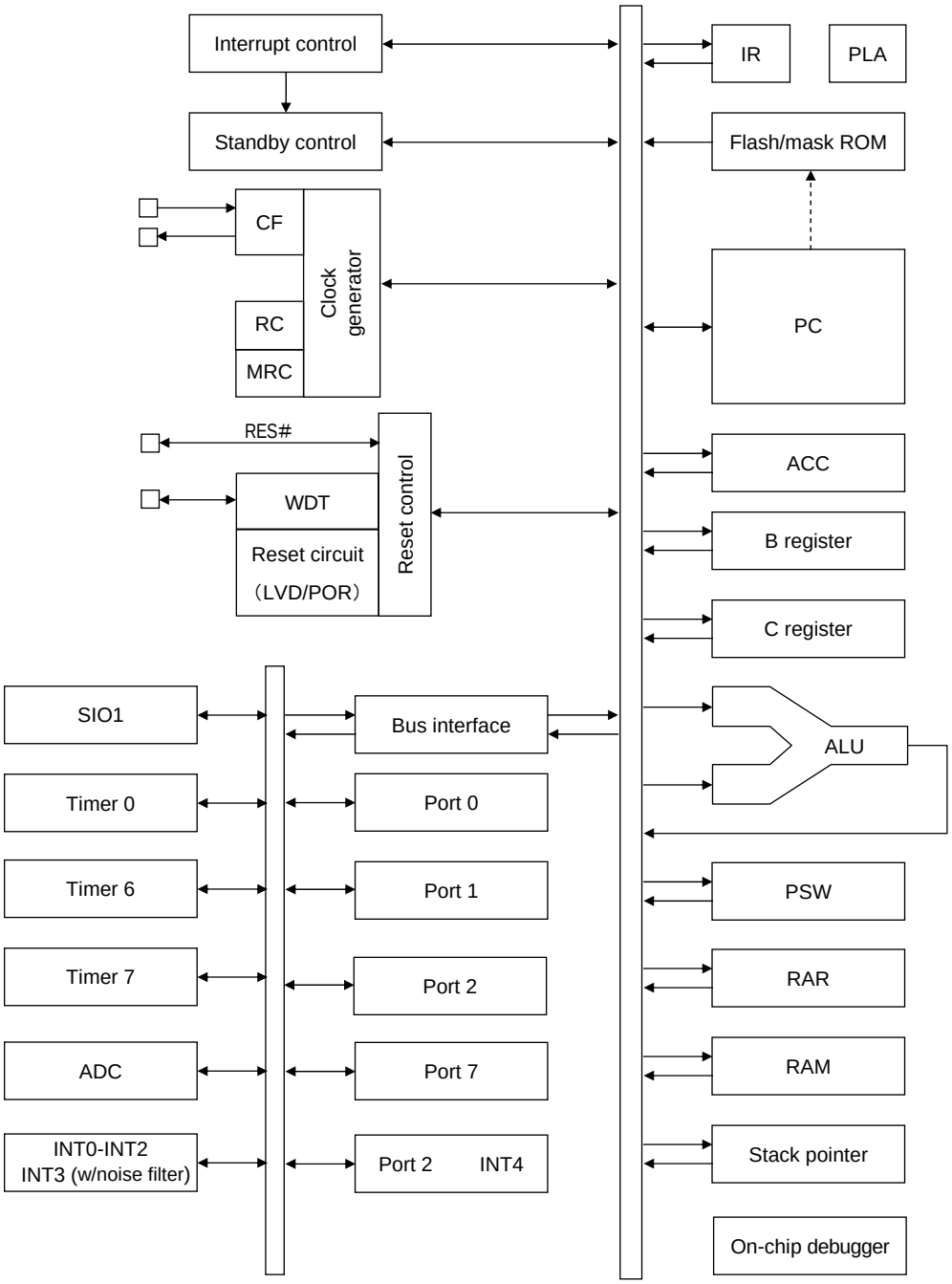
Package	Programming Board
MFP24S	W87F2GM
SSOP24	W87F2GS

1.3 Pinout



SANYO MFP24S/SSOP24 (lead-free and halogen-free product)

1.4 System Block Diagram



1.5 Pin Functions

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>VSS1</td><td>−</td><td>− power supply pin</td><td>No</td></tr>
<tr><td>VDD1</td><td>−</td><td>+ power supply pin</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 4-bit units
• Pull-up resistors can be turned on and off in 4-bit units
• HOLD release input
• Port 0 interrupt input
• Pin functions
P06: Timer 6 toggle output
P07: Timer 7 toggle output
P00 (AN0) to P06(AN6): AD converter input
P05 (DBGP00) to P07(DBGP02): On-chip debugger-0 pin</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units
• Pin functions
P13: SIO1 data output
P14: SIO1 data input/bus I/O
P15: SIO1 clock I/O / INT3 input (with noise filter input)/ timer 0 event input/timer 0H capture input
P16: INT2 input/HOLD release input/timer 0 event input/timer 0L capture input
P17: INT1 input/HOLD release input/timer 0H capture input
P15 (DBGP10) to P13 (DBGP12): On-chip debugger-1 pin
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT1</td><td>○</td><td>○</td><td>×</td><td>○</td><td>○</td></tr>
<tr><td>INT2</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td></tr>
<tr><td>INT3</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 2
P20, P21</td><td>I/O</td><td>• 2-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units
• Pin functions
P20, P21: INT4 input/HOLD release input/timer 0L capture input/ timer 0H capture input
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 7
P70</td><td>I/O</td><td>• 1-bit I/O port
• I/O direction specifiable
• Pull-up resistors can be turned on and off.
• Pin functions
P70: INT0 input/HOLD release input/timer 0L capture input/watchdog timer output
P70 (AN8): AD converter input port
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>○</td><td>○</td><td>×</td><td>○</td><td>○</td></tr>
</table></td><td>No</td></tr>
</table>

(Continued on next page)

Name	I/O	Description	Option
$\overline{\text{RES}}$	I/O	External reset input/internal reset output	No
CF1		• Ceramic resonator input • Pin functions General-purpose input	No
CF2	I/O	• Ceramic resonator output • Pin functions General-purpose input	No

1.6 On-chip Debugger Pin Connection Requirements

For the treatment of the on-chip debugger pins, refer to the separately available documents entitled "RD87 On-chip Debugger Installation Manual" and "LC872000 Series On-chip Debugger Pin Connection Requirements "

1.7 Recommended Unused Pin Connections

Port Name	Recommended Unused Pin Connections	
	Board	Software
P00 to P07	Open	Output low
P10 to P17	Open	Output low
P20 to P21	Open	Output low
P70	Open	Output low
CF1	Pulled low with a 100 kΩ resistor or less	General-purpose input port
CF2	Pulled low with a 100 kΩ resistor or less	General-purpose input port

1.8 Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.

Data can be read into any input port even if it is in the output mode.

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	N-channel open drain	No
P10 to P17 P20, P21	1 bit	1	CMOS	Programmable
		2	N-channel open drain	Programmable
P70	—	No	N-channel open drain	Programmable

Note 1: The control of the presence or absence of the programmable pull-up resistors for port 0 and the switching between low- and high-impedance pull-up connection is exercised in nibble (4-bit) units (P00 to 03 or P04 to 07).

1.9 User Option Table

Option Name	Option Type	Mask ROM Version *1	Flash ROM Version	Option Selected in Units of	Option Selection
Port output type	P00 to P07	○	○	1 bit	CMOS
					N-channel open drain
	P10 to P17	○	○	1 bit	CMOS
					N-channel open drain
	P20 to P21	○	○	1 bit	CMOS
					N-channel open drain
Program start address	—	X *2	○	—	00000h
					01E00h
Low-voltage detection reset function	Detection function	○	○	—	Enable: Used
					Disable: Not used
	Detection level	○	○	—	7 levels
Power-on reset function	Power-on reset level	○	○	—	8 levels

**1: Due to a selection as mask ROM option, the contents cannot be changed after the completion of mask ROM.*

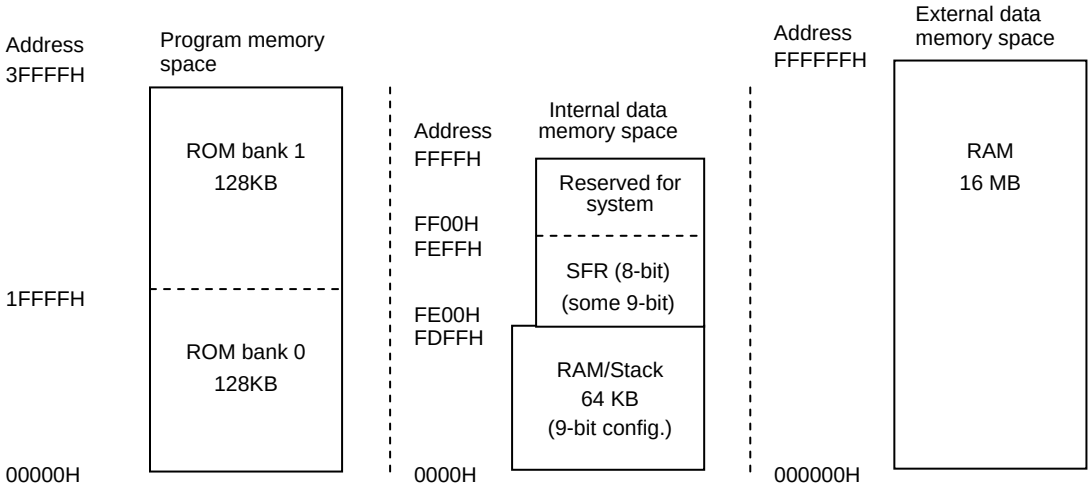
**2: The program start address for mask ROM version will be 00000h.*

2. Internal Configuration

2.1 Memory Space

LC870000 series microcontrollers have the following three types of memory space:

1) Program memory space: 256K bytes (128K bytes × 2 banks)
2) Internal data memory space: 64K bytes (0000H to FDFFH out of 0000H to FFFFH is shared with the stack area.)
3) External data memory space: 16M bytes



Note: SFR is the area in which special function registers such as the accumulator are allocated (see Appendixes A-I).

Figure 2.1.1 Types of Memory Space

2.2 Program Counter (PC)

The program counter (PC) is made up of 17 bits and a bank flag BNK. The value of BNK determines the bank. The lower-order 17 bits of the PC allows linear access to the 128K ROM space in the current bank.

Normally, the PC advances automatically in the current bank on each execution of an instruction. Bank switching is accomplished by executing a Return instruction after pushing necessary addresses onto the stack. When executing a branch or subroutine instruction, when accepting an interrupt, or when a reset is generated, the value corresponding to each operation is loaded into the PC.

Table 2.2.1 lists the values that are loaded into the PC when the respective operations are performed.

Table 2.2.1 Values Loaded in the PC

Operation			PC Value	BNK Value
Inter-rupt	Reset (Note)		00000H	0
			01E00H	0
	INT0		00003H	0
	INT1		0000BH	0
	INT2/T0L/INT4		00013H	0
	INT3		0001BH	0
	T0H		00023H	0
	None		0002BH	0
	None		00033H	0
	SIO1		0003BH	0
	ADC/T6/T7		00043H	0
	Port 0		0004BH	0
Unconditional branch instructions		JUMP a17	PC=a17	Unchanged
		BR r12	PC=PC+2+r12[-2048 to +2047]	Unchanged
Conditional branch instructions		BE, BNE, DBNZ, DBZ, BZ, BNZ, BZW, BNZW, BP, BN, BPC	PC=PC+nb+r8[-128 to +127] nb: Number of instruction bytes	Unchanged
Call instructions		CALL a17	PC=a17	Unchanged
		RCALL r12	PC=PC+2+r12[-2048 to +2047]	Unchanged
		RCALLA	PC=PC+1+Areg[0 to +255]	Unchanged
Return instructions		RET, RETI	PC16 to 08=(SP) PC07 to 00=(SP-1) (SP) denotes the contents of RAM address designated by the value of the stack pointer SP.	BNK is set to bit 8 of (SP-1).
Standard instructions		NOP, MOV, ADD, …	PC=PC+nb nb: Number of instruction bytes	Unchanged

Note: The reset-time program start address can be selected through a user option in the flash version of the microcontroller. In the mask version, the program start address is fixed at address 00000H.

2.3 Program Memory (ROM)

This series of microcontrollers has a program memory space of 256K bytes, but the size of the ROM that is actually incorporated in the microcontroller varies with the type of microcontroller. The ROM table look-up instruction (LDC) can be used to reference all ROM data within the bank. Of the ROM space, the 256 bytes in ROM bank 0 (LC872R00 series: 1F00H to 1FFFH) is reserved as the option area. Consequently, this area is not available as a program area.

2.4 Internal Data Memory (RAM)

This series of microcontrollers has an internal data memory space of 64K bytes, but the size of the RAM that is actually incorporated in the microcontroller varies with the type of the microcontroller. Nine bits are used to access addresses 0000H to FDFFH of the 128K ROM space and 8 or 9 bits are used to access addresses FE00H to FFFFH. The 9th bit of RAM is implemented by bit 1 of the PSW and can be read and written.

The 128 bytes of RAM from 0000H to 007FH are paired to form 64 2-byte indirect address registers. The bit length of these indirect registers is normally 16 bits (8 bits × 2). When they are used by the ROM table look-up instruction (LDC), however, their bit length is set to 17 bits (9 higher-order bits + 8 lower-order bits).

As shown in Figure 2.4.1, the available instructions vary depending on the RAM address.

The efficiency of the ROM used and a higher execution speed can be attempted using these instructions properly.

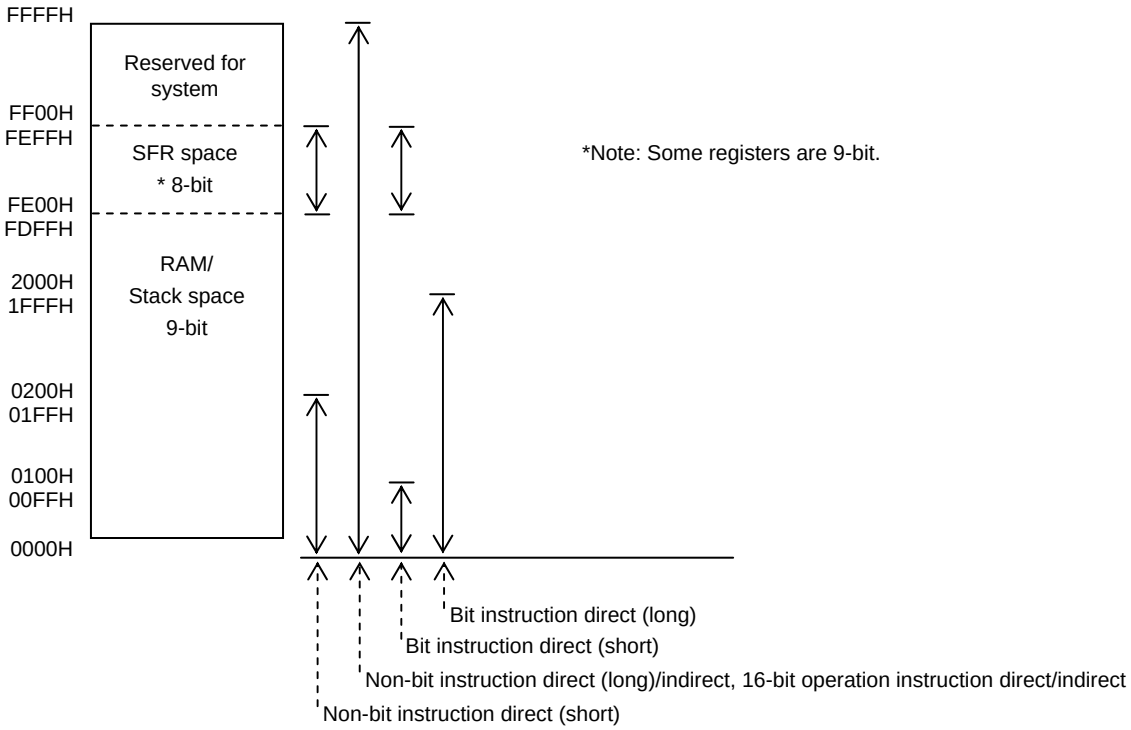


Figure 2.4.1 RAM Addressing Map

When the value of the PC is stored in RAM during the execution of a subroutine call instruction or interrupt, assuming that SP represents the current value of the stack pointer, the value of BNK and the lower-order 8 bits of the (17-bit) PC are stored in RAM address SP+1 and the higher-order 9 bits in SP+2, after which SP is set to SP+2.

2.5 Accumulator/A Register (ACC/A)

The accumulator (ACC), also called the A register, is an 8-bit register that is used for data computation, transfer, and I/O processing. It is allocated to address FE00H in the internal data memory space and initialized to 00H when a reset is performed.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE00	0000 0000	R/W	AREG	AREG7	AREG6	AREG5	AREG4	AREG3	AREG2	AREG1	AREG0

2.6 B Register (B)

The B register is combined with the ACC to form a 16-bit arithmetic register during the execution of a 16-bit arithmetic instruction. During a multiplication or division instruction, the B register is used with the ACC and C register to store the results of computation. In addition, during an external memory access instruction (LDX or STX), the B register designates the higher-order 8 bits of the 24-bit address.

The B register is allocated to address FE01H of the internal data memory space and initialized to 00H when a reset is performed.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE01	0000 0000	R/W	BREG	BREG7	BREG6	BREG5	BREG4	BREG3	BREG2	BREG1	BREG0

2.7 C Register (C)

The C register is used with the ACC and B register to store the results of computation during the execution of a multiplication or division instruction. In addition, during a C register offset indirect instruction, the C register stores the offset data (-128 to +127) to the contents of an indirect register.

The C register is allocated to address FE02H of the internal data memory space and initialized to 00H when a reset is performed.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE02	0000 0000	R/W	CREG	CREG7	CREG6	CREG5	CREG4	CREG3	CREG2	CREG1	CREG0

2.8 Program Status Word (PSW)

The program status word (PSW) is made up of flags that indicate the status of computation results, a flag to access the 9th bit of RAM, and a flag to designate the bank during the LDCW instruction. The PSW is allocated to address FE06H of the internal data memory space and initialized to 00H when a reset is performed.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE06	0000 0000	R/W	PSW	CY	AC	PSWB5	PSWB4	LDCBNK	OV	P1	PARITY

CY (bit 7): Carry flag

CY is set (to 1) when a carry occurs as the result of a computation and cleared (to 0) when no carry occurs. There are following four types of carries:

1) Carry resulting from an addition
2) Borrow resulting from a subtraction
3) Borrow resulting from a comparison
4) Carry resulting from a rotation

There are some instructions that do not affect this flag at all.

AC (bit 6): Auxiliary carry flag

AC is set (to 1) when a carry or borrow occurs in bit 3 (bit 3 of the higher-order byte during a 16-bit computation) as the result of an addition or subtraction and cleared (to 0) otherwise.

There are some instructions that do not affect this flag at all.

PSWB5, PSWB4 (bits 5 and 4): User bits

These bits can be read and written through instructions. They can be used by the user freely.

LDCBNK (bit 3): Bank flag for the table look-up instruction (LDCW)

This bit designates the ROM bank to be specified when reading the program ROM with a table look-up instruction.

(0: ROM-ADR = 0 to 1FFFF, 1: ROM-ADR = 20000 to 3FFFF)

OV (bit 2): Overflow flag

OV is set (to 1) when an overflow occurs as the result of an arithmetic operation and cleared (to 0) otherwise. An overflow occurs in the following cases:

1) When MSB is used as the sign bit and when the result of negative number + negative number or negative number – positive number is a positive.
2) When MSB is used as the sign bit and when the result of positive number + positive number or positive number – negative number is a negative number.

3) When the higher-order 8 bits of a 16 bits × 8 bits multiplication is nonzero
4) When the higher-order 16 bits of a 24 bits × 16 bits multiplication is nonzero
5) When the divisor of a division is 0.

There are some instructions that do not affect this flag at all.

P1 (bit 1): RAM bit 8 data flag

P1 is used to manipulate bit 8 of 9-bit internal data RAM (0000H to FDFFH). Its behavior varies depending on the instruction executed. See Table 2.4.1 for details.

PARITY (bit 0): Parity flag

This bit shows the parity of the accumulator (A register). The parity flag is set (to 1) when there is an odd number of 1s in the A register. It is cleared (to 0) when there is an even number of 1s (in the A register).

2.9 Stack Pointer (SP)

LC870000 series microcontrollers can use RAM addresses 0000H to FDFFH as a stack area. The size of RAM, however, varies depending on the microcontroller type. The SP is 16 bits long and made up of two registers: SPL (at address FE0A) and SPH (at address FE0B). It is initialized to 0000H when a reset is performed.

The SP is incremented by 1 before data is saved in stack memory and decremented by 1 after the data is restored from stack memory.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE0A	0000 0000	R/W	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
FE0B	0000 0000	R/W	SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8

The value of the SP changes as follows:

1) When the PUSH instruction is executed: SP = SP + 1, RAM (SP) = DATA
2) When the CALL instruction is executed: SP = SP + 1, RAM (SP) = ROMBANK + ADL
   SP = SP + 1, RAM (SP) = ADH
3) When the POP instruction is executed: DATA = RAM (SP), SP = SP - 1
4) When the RET instruction is executed: ADH = RAM (SP), SP = SP - 1
   ROMBANK + ADL = RAM(SP), SP = SP - 1

2.10 Indirect Addressing Registers

LC870000 series microcontrollers are provided with three addressing schemes ([Rn], [Rn+C], [off]), which use the contents of indirect registers (indirect addressing modes). (See Section 2.11 for the addressing modes.) These addressing modes use 64 2-byte indirect registers (R0 to R63) allocated to RAM addresses 0 to 7EH. The indirect registers can also be used as general-purpose registers (e.g., for saving 2-byte data). Naturally, these addresses can be used as ordinary RAM (in 1-byte (9 bits) units) if they are not used as indirect registers. R0 to R63 are “system reserved words” to the assembler and need not be defined by the user.

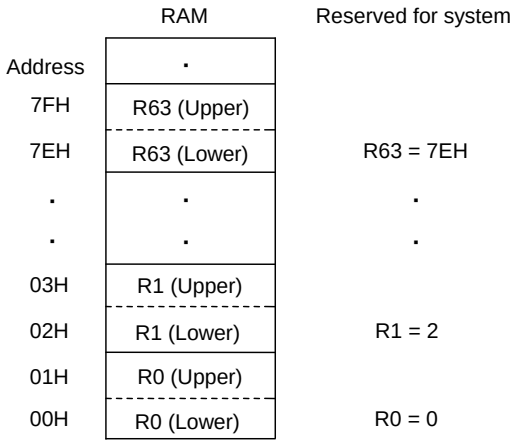


Figure 2.10.1 Allocation of Indirect Registers

2.11 Addressing Modes

LC870000 series microcontrollers support the following seven addressing modes:

1) Immediate (immediate data refers to data whose value has been established at program preparation (assembly) time.)
2) Indirect register (Rn) indirect ($0 \leq n \leq 63$)
3) Indirect register (Rn) + C register indirect ($0 \leq n \leq 63$)
4) Indirect register (R0) + Offset value indirect
5) Direct
6) ROM table look-up
7) External data memory access

The rest of this section describes these addressing modes.

2.11.1 Immediate Addressing (#)

The immediate addressing mode allows 8-bit (1-byte) or 16-bit (1-word) immediate data to be handled. Examples are given below.

Examples:

```
      LD      #12H;       Loads the accumulator with byte data (12H).
L1:   LDW     #1234H;     Loads the BA register pair with word data (1234H).
      PUSH    #34H;       Loads the stack with byte data (34H).
      ADD     #56H;       Adds byte data (56H) to the accumulator.
      BE      #78H, L1;   Compares byte data (78H) with the accumulator for a branch.
```

2.11.2 Indirect Register Indirect Addressing ([Rn])

In indirect register indirect addressing mode, it is possible to select one of the indirect registers (R0 to R63) and use its contents to designate an address in RAM or SFR. When the selected register contains, for example, "FE02H," it designates the C register.

Example: When R3 contains "123H" (RAM address 6: 23H, RAM address 7: 01H)

```
      LD    [R3];      Transfers the contents of RAM address 123H to the accumulator.
L1:   STW   [R3];      Transfers the contents of BA register pair to RAM address 123H.
      PUSH  [R3];      Saves the contents of RAM address123H in the stack.
      SUB   [R3];      Subtracts the contents of RAM address 123H from the accumulator.
      DBZ   [R3], L1;  Decrements the contents of RAM address 123H by 1 and causes a branch if
                       zero.
```

2.11.3 Indirect Register + C Register Indirect Addressing ([Rn, C])

In indirect register + C register indirect addressing mode, the result of adding the contents of one of the indirect registers (R0 to R63) to the contents of the C register (-128 to +127 with MSB being the sign bit) designates an address in RAM or SFR. For example, if the selected indirect register contains "FE02H" and the C register contains "FFH (-1)," the address "B register (FE02H + (-1) = FE01H" is designated.

Examples: When R3 contains "123H" and the C register contains "02H"

```
      LD    [R3, C];     Transfers the contents of RAM address 125H to the accumulator.
L1:   STW   [R3, C];     Transfers the contents of the BA register pair to RAM address 125H.
      PUSH  [R3, C];     Saves the contents of RAM address 125H in the stack.
      SUB   [R3, C];     Subtracts the contents of RAM address 125H from the accumulator.
      DBZ   [R3, C], L1; Decrements the contents of RAM address 125H by 1 and causes a branch if
                         zero.
```

<Notes on this addressing mode >

The internal data memory space is divided into three closed functional areas as explained in Section 2.1, namely, 1) system reserved area (FF00H to FFFFH), 2) SFR area (FE00H to FEFFH), and 3) RAM/stack area (0000H to FDFFH). Consequently, it is not possible to point to a different area using the value of the C register from the basic area designated by the contents of Rn. For example, if the instruction "LD [R5,C]" is executed when R5 contains "0FDFFH" and the C register contains "1," since the basic area is 3) RAM/stack area (0000H to FDFFH), the intended address "0FDFFH+1 = 0FE00H" lies outside the basic area and "0FFH" is placed in the ACC as the result of LD. If the instruction "LD [R5,C]" is executed when R5 contains "0FEFFH" and the C register contains "2," since the basic area is 2) SFR area (FE00H to FEFFH), the intended address "0FEFFH+2 = 0FF01H" lies outside the basic area. In this case, since SFR is confined in an 8-bit address space, the part of the address data addressing outside the 8-bit address space is ignored and the contents of 0FE01H (B register) are placed in the ACC as the result of the computation "0FF01H&0FFH+0FE00H = 0FE01H."

2.11.4 Indirect Register (R0) + Offset Value Indirect Addressing ([off])

In this addressing mode, the result of adding the 7-bit signed offset data off (-64 to + 63) to the contents of the indirect register R0 designate an address in RAM or SFR. If R0 contains "FE02H" and off has a value of "7EH(-2)," for example, the A register (FE02H+(-2) = FE00H) is designated.

Examples: When R0 contains "123H" (RAM address 0: 23H, RAM address 1: 01H)

```
      LD    [10H];      Transfers the contents of RAM address 133H to the accumulator.
L1:   STW   [10H];      Transfers the contents of the BA register pair to RAM address 133H.
      PUSH  [10H];      Saves the contents of RAM address 133H in the stack.
      SUB   [10H];      Subtracts the contents of RAM address 133H from the accumulator.
      DBZ   [10H], L1;  Decrements the contents of RAM address 133H by 1 and causes a branch if
                        zero.
```

<Notes on this addressing mode>

The internal data memory space is divided into three closed closed functional areas as explained in Section 2.1, namely, 1) system reserved area (FF00H to FFFFH), 2) SFR area (FE00H to FEFFH), and 3) RAM/stack area (0000H to FDFFH). Consequently, it is not possible to point to a different area using an offset value from the basic area designated by the contents of R0. For example, if the instruction "LD [1]" is executed when R0 contains "0FDFFH," since the basic area is 3) RAM/stack area (0000H to FDFFH), the intended address "0FDFFH+1 = 0FE00H" lies outside the basic area and "0FFH" is placed in the ACC as the results of LD. If the instruction "LD [2]" is executed when R0 contains "0FEFFH," since the basic area is 2) SFR area (FE00H to FEFFH), the intended address "0FEFFH+2 = 0FF01H" lies outside the basic area. In this case, since SFR is confined in an 8-bit address space, the part of the address data addressing outside the 8-bit address space is ignored and the contents of "0FE01H (B register) are placed in the ACC as the result of computation "0FF01H&0FFH+0FE00H = 0FE01H."

2.11.5 Direct Addressing (dst)

Direct addressing mode allows a RAM or SFR address to be specified directly in an operand. In this addressing mode, the assembler automatically generates the optimum instruction code from the address specified in the operand (the number of instruction bytes varies according to the address specified in the operand). Long (middle) range instructions (identified by an "L (M)" at the end of the mnemonic) are available to make the byte count of instructions constant (align instructions with the longest one).

Examples:

```
      LD    123H;       Transfers the contents of RAM address 123H to the accumulator
                        (2-byte instruction).
      LDL   123H;       Transfers the contents of RAM address 123H to the accumulator
                        (3-byte instruction).
L1:   STW   123H;       Transfers the contents of the BA register pair to RAM address 123H.
      PUSH  123H;       Saves the contents of RAM address 123H in the stack.
      SUB   123H;       Subtracts the contents of RAM address 123H from the accumulator.
      DBZ   123H, L1;   Decrements the contents of RAM address 123H by 1 and causes a branch if
                        zero.
```

2.11.6 ROM Table Look-up Addressing

LC870000 series microcontrollers can read 2-byte data into the BA register pair at once using the LDCW instruction. Three addressing modes ([Rn], [Rn, C], and [off]) are available for this purpose. (In this case only, Rn is configured as 17-bit registers (128K-byte space)).

For models with banked ROM, it is possible to reference the ROM data in the ROM bank (128K bytes) identified by the LDCBNK flag (bit 3) in the PSW. Consequently, when looking into the ROM table on a series model with banked ROM, execute the LDCW instruction after switching the bank using the SET1 or CLR1 instruction so that the LDCBNK flag designates the ROM bank where the ROM table resides.

Examples:

```
TBL: DB      34H
     DB      12H
     DW      5678H
     •       •
     •       •
     LDW     #TBL;              Loads the BA register pair with the TBL address.
     CHGP3   (TBL >> 17) & 1;   Loads LDCBNK in PSW with bit 17 of the TBL address. (Note 1)
     CHGP1   (TBL >> 16) & 1;   Loads P1 in PSW with bit 16 of the TBL address.
     STW     R0;                Loads indirect register R0 with the TBL address (bits 16 to 0).
     LDCW    [1];               Reads the ROM table (B=78H, ACC=12H).
     MOV     #1, C;             Loads the C register with "01H."
     LDCW    [R0, C];           Reads the ROM table (B=78H, ACC=12H).
     INC     C;                 Increments the C register by 1.
     LDCW    [R0, C]:           Reads the ROM table (B=56H, ACC=78H).
```

Note 1: LDCBNK (bit 3) of PSW needs to be set up only for models with banked ROM.

2.11.7 External Data Memory Addressing

LC870000 series microcontrollers can access external data memory spaces of up to 16M bytes (24 bits) using the LDX and STX instructions. To designate a 24-bit space, specify the contents of the B register (8 bits) as the highest-order byte of the address and the contents (16 bits) of either (Rn), (Rn) + (C), or (R0) + off as the lower-order bytes of the address.

Examples:

```
LDW     #3456H;    Sets up the lower-order 16 bits.
STW     R0;        Loads the indirect register R0 with the lower-order 16 bits of the address.
MOV     #12H, B;   Sets up the higher-order 8 bits of the address.
LDX     [1];       Transfers the contents of external data memory (address 123457H) to the
                   accumulator.
```

Table 2.4.1 Chart of State Transitions of Bit 8 (RAM / SFR) and P1

Instruction	Bit 8 (RAM/SFR)	P1 (PSW Bit 1)	Remarks
LD#/LDW#	—	—	
LD	—	P1←REG8	
LDW	—	P1←REGH8	
ST	REG8←P1	—	
STW	REGL8, REGH8←P1	—	
MOV	REG8←P1	—	
PUSH#	RAM8←P1	—	
PUSH	RAM8←REG8	P1←REG8	
PUSHW	RAMH8←REGH8, RAML8←REGL8	P1←REGH8	
PUSH_P	RAM8←Pl	—	
PUSH_BA	RAMH8←P1, RAML8←P1	—	
POP	REG8←RAM8	P1←RAM8	P1←bit1 when PSW is popped
POPW	REGH8←RAMH8, REGL8←RAML8	Pl←RAMH8	P1←bit1 when higher-order address of PSW is popped
POP_P	—	P1←RAMl (bit l)	BIT8 ignored
POP_BA	—	P1←RAMH8	
XCH	REG8↔P1	Same as left.	
XCHW	REGH8←P1, REGL8←Pl, P1←REGH8	Same as left.	
INC	INC 9 bits	P1←REG8 after computation	INC 9 bits
INCW	INC 17 bits, REGL8←lower-byte of CY	P1←REGH8 after computation	INC 17 bits
DEC	DEC 9 bits	P1←REG8 after computation	DEC 9 bits
DECW	DEC 17 bits, REGL8← lower byte of CY inverted	P1←REGH8 after computation	DEC 17 bits
DBNZ	DEC 9 bits	P1←REG8	DEC 9 bits, check lower-order 8 bits
DBZ	DEC 9 bits	P1←REG8	DEC 9 bits, check lower-order 8 bits
SET1	—	—	
NOT1	—	—	
CLR1	—	—	
BPC	—	—	
BP	—	—	
BN	—	—	
MUL24 /DIV24	RAM8←“1”	—	Bit 8 of RAM address for storing results is set to 1.
FUNC	—	—	

Note: A “1” is read and processed if the processing target is an 8-bit register (no bit 8).

Legends:

REG8: Bit 8 of a RAM or SFR location
REGH8/REGL8: Bit 8 of the higher-order byte of a RAM location or SFR/bit 8 of the lower-order byte
RAM8: Bit 8 of a RAM location
RAMH8/RAML8: Bit 8 of the higher-order byte of a RAM location/bit 8 of the lower-order byte

3. Peripheral System Configuration

This chapter describes the internal functional blocks (peripheral system) of this series of microcontrollers except the CPU core, RAM, and ROM. Port block diagrams are provided in Appendix (A-II) for reference.

3.1 Port 0

3.1.1 Overview

Port 0 is an 8-bit I/O port equipped with programmable pull-up resistors. It is made up of a data latch, a data direction register, and a control circuit. Control of the input/output signal direction and the pull-up resistors is accomplished through the data direction register in 4-bit units.

This port can also serve as a pin for external interrupts and can release HOLD mode. As a user option, either CMOS output with a programmable pull-up resistor or N-channel open drain output can be selected as the output type in 1-bit units.

<Notes on the flash ROM version>

Port P05 is temporarily set low when the microcontroller is reset. During the reset sequence, do not apply a clock or any medium voltage level signal (including Hi-Z) to port P07.

For treatment of the on-chip debugger pins, refer to the separately available documents entitled "RD87 On-chip Debugger Installation Manual" and "LC872000 Series On-chip Debugger Pin Connection Requirements."

3.1.2 Functions

1) Input/output port (8 bits: P00-P07)
   - The port output data is controlled by the port 0 data latch (P0: FE40) in 1-bit units.
   - I/O control of P00 to P03 is accomplished by P0LDDR (P0DDR: FE41, bit 0).
   - I/O control of P04 to P07 is accomplished by P0HDDR (P0DDR: FE41, bit 1).
   - Ports selected as CMOS outputs by user option are provided with programmable pull-up resistors.
   - The programmable pull-up resistors may be of either low impedance or high impedance type.
   - The programmable pull-up resistors for P00 to P03 are controlled by the P0LPU (P0DDR: FE41, bit 2). Their type (either low impedance or high impedance) is selected by P0LPUS (P0DDR: FE41, bit 6).
   - The programmable pull-up resistors for P04 to P07 are controlled by P0HPU (P0DDR: FE41, bit 3). Their type (either low impedance or high impedance) is selected by P0HPUS (P0DDR: FE41, bit 7).

2) Interrupt pin function

   P0FLG (P0DDR: FE41, bit 5) is set when an input port is specified and 0 level data is input to one of port bits whose corresponding bit in the port 0 data latch (P0: FE40) is set to 1.

   In this case, if P0IE (P0DDR: FE41, bit 4) is 1, HOLD mode is released and an interrupt request to vector address 004BH is generated.

3) Multiplexed pin function

Pin P06 also serves as the timer 6 toggle output, pin P07 as the timer 7 toggle output, and P00 to P06 as the analog input channel pins AN0 to AN6.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE40	0000 0000	R/W	P0	P07	P06	P05	P04	P03	P02	P01	P00
FE41	0000 0000	R/W	P0DDR	P0HPUS	P0LPUS	P0FLG	P0IE	P0HPU	P0LPU	P0HDDR	P0LDDR
FE42	00HH HHHH	R/W	P0FCR	T7OE	T6OE	-	-	-	-	-	-

3.1.3 Related Registers

3.1.3.1 Port 0 data latch (P0)

1) The port 0 data latch is an 8-bit register for controlling port 0 output data and port 0 interrupts.
2) When this register is read with an instruction, data at pins P00 to P07 is read in. If P0 (FE40) is manipulated using the NOT1, CLR1, SET1, DBZ, DBNZ, INC, or DEC instruction, the contents of the register are referenced instead of the data at the port pins.
3) Port 0 data can always be read regardless of the I/O state of the port.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE40	0000 0000	R/W	P0	P07	P06	P05	P04	P03	P02	P01	P00

3.1.3.2 Port 0 data direction register (P0DDR)

1) This register is an 8-bit register that controls the I/O direction of port 0 data in 4-bit units, the pull-up resistors in 4-bit units, and port 0 interrupts.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE41	0000 0000	R/W	P0DDR	P0HPUS	P0LPUS	P0FLG	P0IE	P0HPU	P0LPU	P0HDDR	P0LDDR

P0HPUS (bit 7): P07-P04 high/low impedance pull-up resistor select

A 1 in this bit selects high impedance pull-up resistors for pins P07 to P04 and a 0 selects low impedance pull-up resistors.

P0LPUS (bit 6): P03-P00 high/low impedance pull-up resistor select

A 1 in this bit selects high impedance pull-up resistors for pins P03 to P00 and a 0 selects low impedance pull-up resistors.

P0FLG (bit 5): P0 interrupt source flag

This flag is set when a low level is applied to a port 0 pin that is set up for input and the corresponding P0 (FE40) bit is set.

A HOLD mode release signal and an interrupt request to vector address 004BH are generated when this bit and the interrupt request enable bit (P0IE) are set to 1.

This bit must be cleared with an instruction as it is not cleared automatically.

P0IE (bit 4): P0 interrupt request enable

Setting this bit and P0FLG to 1 generates a HOLD mode release signal and an interrupt request to vector address 004BH

P0HPU (bit 3): P07-P04 pull-up resistor control

When this bit is set to 1 and P0HDDR to 0, pull-up resistors are connected to port P07 to P04 that are selected as CMOS output by user option.

P0LPU (bit 2): P03-P00 pull-up resistor control

When this bit is set to 1 and P0LDDR to 0, pull-up resistors are connected to port bits P03 to P00 that are selected as CMOS output by user option.

P0HDDR (bit 1): P07-P04 I/O control

When this bit is set to 1, P07 to P04 are placed into output mode and the contents of the corresponding port 0 data latch (P0) are output from the port.

When this bit is set to 0, P07 to P04 are placed into input mode and P0FLG is set when a low level is detected at a port whose corresponding port 0 data latch (P0) bit is set to 1.

P0LDDR (bit 0): P03-P00 I/O control

When this bit is set to 1, P03 to P00 are placed into output mode and the contents of the corresponding port 0 data latch (P0) are output from the port.

When this bit is set to 0, P03 to P00 are placed into input mode and P0FLG is set when a low level is detected at a port whose corresponding port 0 data latch (P0) bit is set to 1.

P07-P04 pull-up resistor selection settings

P0HPUS	P0HPU	Port for Which P0HDDR=0 and CMOS Option is Specified
X	0	Pull-up resistor OFF
X	0	Pull-up resistor OFF
0	1	Low impedance pull-up resistor ON
1	1	High impedance pull-up resistor ON

P03-P00 pull-up resistor selection settings

P0LPUS	P0LPU	Port for Which P0LDDR=0 and CMOS Option is Specified
X	0	Pull-up resistor OFF
X	0	Pull-up resistor OFF
0	1	Low impedance pull-up resistor ON
1	1	High impedance pull-up resistor ON

3.1.3.3 Port 0 function control register (P0FCR)

1) This register is a 2-bit register that controls the port 0 multiplexed output pin

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE42	00HH HHHH	R/W	P0FCR	T7OE	T6OE	-	-	-	-	-	-

T7OE (bit 7):

This bit controls the output data at pin P07. It is disabled when P07 is in input mode.

When P07 is in output mode:

0: Carries the value of the port data latch.

1: Carries the OR of the waveform that toggles at the interval determined by timer 7 and the value of the port data latch.

T6OE (bit 6):

This bit controls the output data at pin P06. It is disabled when P06 is in input mode.

When P06 is in output mode:

0: Carries the value of the port data latch.

1: Carries the OR of the waveform that toggles at the interval determined by timer 6 and the value of the port data latch.

3.1.4 Options

Two user options are available.

1) CMOS output (with a programmable pull-up resistor)
2) N-channel open drain output

3.1.5 HALT and HOLD Mode Operation

When in HALT or HOLD mode, port 0 retains the state that is established when HALT or HOLD mode is entered.

3.2 Port 1

3.2.1 Overview

Port 1 is an 8-bit I/O port equipped with programmable pull-up resistors. It is made up of a data latch, a data direction register, a function control register, and a control circuit. Control of the input/output signal direction is accomplished by the data direction register in 1-bit units. Port 1 can also be used as a serial interface I/O port by manipulating its function control register.

As a user option, either CMOS output with a programmable pull-up resistor or N-channel open drain output with a programmable pull-up resistor can be selected as the output type in 1-bit units.

<Notes on the flash ROM version>

Port P15 is temporarily set low when the microcontroller is reset. During the reset sequence, do not apply a clock or any medium voltage level signal (including Hi-Z) to port P13.

For treatment of the on-chip debugger pins, refer to the separately available manuals entitled "RD87 On-chip Debugger Installation Guide" and "LC872000 Series On-chip Debugger Pin Connection Requirements "

3.2.2 Functions

1) Input/output port (8 bits: P10 to P17)
   - The port output data is controlled by the port 1 data latch (P1:FE44) and the I/O direction is controlled by the port 1 data direction register (P1DDR:FE45).
   - Each port is provided with a programmable pull-up resistor.

2) Interrupt input pin function
   - P17 is assigned to INT1 and used to detect a low or high level, or a low or high edge and set the interrupt flag.
   - P16 and P15 are assigned to INT2 and INT3, respectively, and used to detect a low edge, high edge, or both edges and set the interrupt flag.

3) Timer 0 count input function

   A count signal is sent to timer 0 each time a signal change that sets the interrupt flag is supplied to the port selected from P16 and P15

4) Timer 0L capture input function

   A timer 0L capture signal is generated each time a signal change that sets the interrupt flag is supplied to the port selected from P70 and P16.

   When a selected level of signal is input to P70 that is specified for level-triggered interrupts, a timer 0L capture signal is generated at 1 cycle interval for the duration of the input signal.

5) Timer 0H capture input function

   A timer 0H capture signal is generated each time a signal change that sets the interrupt flag is supplied to the port selected from P17 and P15.

   When a selected level of signal is input to P17 that is specified for level-triggered interrupts, a timer 0H capture signal is generated at 1 cycle interval for the duration of the input signal.

6) HOLD mode release function

- When the interrupt flag and interrupt enable flag are set by INT1 or INT2, a HOLD mode release signal is generated, releasing HOLD mode. The CPU then enters HALT mode (system clock set to medium-speed RC). When the interrupt is accepted, the CPU switches from HALT mode to normal operating mode.
- When a level of signal that sets an interrupt flag is input to P17 that is specified for level-triggered interrupts in HOLD mode, the interrupt flag is set. In this case, if the corresponding interrupt enable flag is set, HOLD mode is released.
- When a signal change that sets an interrupt flag is input to P16 in HOLD mode, the interrupt flag is set. In this case, HOLD mode is released if the corresponding interrupt enable flag is set. The interrupt flag, however, can be set neither by a rising edge occurring when P16 data which is established when HOLD mode is entered is in the high state nor by a falling edge occurring when P16 data which is established when HOLD mode is entered is in the low state. Consequently, to release HOLD mode with P16, it is recommended that P16 be used in the double edge interrupt mode.

7) Multiplexed pin functions

P17 is also used as the timer 0H capture input, P16 as the timer 0 event input/timer 0L capture input, P15 as the timer 0 event input/timer 0H capture input/SIO1 clock I/O, and P14 to P13 for SIO1 I/O.

	Input	Output	Interrupt Input Signal Detection	Timer 0 Count Input	Capture Input	HOLD Mode Release
P17	With a programmable pull-up resistor	CMOS/N-channel open drain	L level, H level, L edge, H edge	–	Timer 0H	Enabled (Note)
P16			L edge, H edge, Both edges	Yes	Timer 0L	Enabled
P15				Yes	Timer 0H	–

Note: P17 HOLD mode release is available only when level detection is set.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE44	0000 0000	R/W	P1	P17	P16	P15	P14	P13	P12	P11	P10
FE45	0000 0000	R/W	P1DDR	P17DDR	P16DDR	P15DDR	P14DDR	P13DDR	P12DDR	P11DDR	P10DDR
FE46	HH00 0HHH	R/W	P1FCR	-	-	P15FCR	P14FCR	P13FCR	-	-	-
FE47	0000 HHH0	R/W	P1TST	FIX0	FIX0	FIX0	FIX0	-	-	-	FIX0
FE5D	0000 0000	R/W	I01CR	INT1LH	INT1LV	INT1IF	INT1IE	INT0LH	INT0LV	INT0IF	INT0IE
FE5E	0000 0000	R/W	I23CR	INT3HEG	INT3LEG	INT3IF	INT3IE	INT2HEG	INT2LEG	INT2IF	INT2IE
FE5F	00HH H000	R/W	ISL	ST0HCP	ST0LCP	-	-	-	NFSEL	NFON	ST0IN

Bits 7, 6, 5, 4, and 0 of P1TST (FE47) are reserved for testing. They must always be set to 0.

3.2.3 Related Registers

3.2.3.1 Port 1 data latch (P1)

1) The port 1 data latch is an 8-bit register for controlling port 1 output data and pull-up resistors
2) When this register is read with an instruction, data at pins P10 to P17 is read in. If P1 (FE44) is manipulated using the NOT1, CLR1, SET1, DBZ, DBNZ, INC, or DEC instruction, the contents of the register are referenced instead of the data at the port pins.
3) Port 1 data can always be read regardless of the I/O state of the port.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE44	0000 0000	R/W	P1	P17	P16	P15	P14	P13	P12	P11	P10

3.2.3.2 Port 1 data direction register (P1DDR)

1) This register is an 8-bit register that controls the I/O direction of port 1 data in 1-bit units. Port P1n is placed in output mode when bit P1nDDR is set to 1 and in input mode when set to 0.

2) When bit P1nDDR is set to 0 and bit P1n of the port 1 data latch to 1, port P1n is an input with a pull-up resistor.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE45	0000 0000	R/W	P1DDR	P17DDR	P16DDR	P15DDR	P14DDR	P13DDR	P12DDR	P11DDR	P10DDR

Register Data		Port P1n State		Internal Pull-up Resistor
P1n	P1nDDR	Input	Output	
0	0	Enabled	Open	OFF
1	0	Enabled	Internal pull-up resistor	ON
0	1	Enabled	Low	OFF
1	1	Enabled	High/open (CMOS/N-channel open drain)	OFF

3.2.3.3 Port 1 function control register (P1FCR)

1) This register is a 3-bit register that controls the multiplexed output of port 1.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE46	HH00 0HHH	R/W	P1FCR	-	-	P15FCR	P14FCR	P13FCR	-	-	-

n	P1nFCR	P1n	P1n Pin Data in Output Mode (P1nDDR=1)
5	0	–	Value of port data latch (P15)
	1	0	SIO1 clock output data
	1	1	High output
4	0	–	Value of port data latch (P14)
	1	0	SIO1 output data
	1	1	High output
3	0	–	Value of port data latch (P13)
	1	0	SIO1 output data
	1	1	High output

The high data output at a pin that is selected as an N-channel open drain output (by a user option) is represented by an open circuit.

P15FCR (bit 5): P15 function control (SIO1 clock output control)

This bit controls the output data at pin P15.

When P15 is placed in output mpde (P15DDR = 1) and P15FCR is set to 1, OR of the SIO1 clock output data and the port data latch is placed at pin P15.

P14FCR (bit 4): P14 function control (SIO1 data output control)

This bit controls the output data at pin P14.

When bit P14 is placed in output mpde (P14DDR = 1) and P14FCR is set to 1, OR of the SIO1 output data and the port data latch is placed at pin P14.

If SIO1 is active, SIO1 input data is taken in from pin P14 regardless of the I/O state of P14.

P13FCR (bit 3): P13 function control (SIO1 data output control)

This bit controls the output data at pin P13.

When bit P13 is placed in output mpde (P13DDR = 1) and P13FCR is set to 1, the OR of the SIO1 output data and the port data latch is placed at pin P13.

3.2.3.4 External interrupt 0/1 control register (I01CR)

1) This register is an 8-bit register for controlling external interrupts 0 and 1.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE5D	0000 0000	R/W	I01CR	INT1LH	INT1LV	INT1IF	INT1IE	INT0LH	INT0LV	INT0IF	INT0IE

INT1LH (bit 7): INT1 detection polarity select

INT1LV (bit 6): INT1 detection level/edge select

INT1LH	INT1LV	INT1 Interrupt Conditions (P17 Pin Data)
0	0	Falling edge detected
0	1	Low level detected
1	0	Rising edge detected
1	1	High level detected

INT1IF (bit 5): INT1 interrupt source flag

This bit is set when the conditions specified by INT1LH and INT1LV are satisfied. When this bit and the INT1 interrupt request enable bit (INT1IE) are set to 1, a HOLD mode release signal and an interrupt request to vector address 000BH are generated.

This bit must be cleared with an instruction as it is not cleared automatically.

INT1IE (bit 4): INT1 interrupt request enable

When this bit and INT1IF are set to 1, a HOLD mode release signal and an interrupt request to vector address 000BH are generated.

INT0LH (bit 3): INT0 detection polarity select

INT0LV (bit 2): INT0 detection level/edge select

INT0LH	INT0LV	INT0 Interrupt Conditions (P70 Pin Data)
0	0	Falling edge detected
0	1	Low level detected
1	0	Rising edge detected
1	1	High level detected

INT0IF (bit 1): INT0 interrupt source flag

This bit is set when the conditions specified by INT0LH and INT0LV are satisfied. When this bit and the INT0 interrupt request enable bit (INT0IE) are set to 1, a HOLD mode release signal and an interrupt request to vector address 0003H are generated.

This bit must be cleared with an instruction as it is not cleared automatically.

INT0IE (bit 0): INT0 interrupt request enable

When this bit and INT0IF are set to 1, a HOLD mode release signal and an interrupt request to vector address 0003H are generated.

3.2.3.5 External interrupt 2/3 control register (I23CR)

1) This register is an 8 bit register for controlling external interrupts 2 and 3.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE5E	0000 0000	R/W	I23CR	INT3HEG	INT3LEG	INT3IF	INT3IE	INT2HEG	INT2LEG	INT2IF	INT2IE

INT3HEG (bit 7): INT3 rising edge detection control

INT3LEG (bit 6): INT3 falling edge detection control

INT3HEG	INT3LEG	INT3 Interrupt Conditions (P15 Pin Data)
0	0	No edge detected
0	1	Falling edge detected
1	0	Rising edge detected
1	1	Both edges detected

INT3IF (bit 5): INT3 interrupt source flag

This bit is set when the conditions specified by INT3HEG and INT3LEG are satisfied. When this bit and the INT3 interrupt request enable bit (INT3IE) are set to 1, an interrupt request to vector address 001BH is generated.

This bit must be cleared with an instruction as it is not cleared automatically.

INT3IE (bit 4): INT3 interrupt request enable

When this bit and INT3IF are set to 1, an interrupt request to vector address 001BH is generated.

INT2HEG (bit 3): INT2 rising edge detection control

INT2LEG (bit 2): INT2 falling edge detection control

INT2HEG	INT2LEG	INT2 Interrupt Conditions (P16 Pin Data)
0	0	No edge detected
0	1	Falling edge detected
1	0	Rising edge detected
1	1	Both edges detected

INT2IF (bit 1): INT2 interrupt source flag

This bit is set when the conditions specified by INT2HEG and INT2LEG are satisfied. When this bit and the INT2 interrupt request enable bit (INT2IE) are set to 1, a HOLD mode release signal and an interrupt request to vector address 0013H are generated.

The interrupt flag, however, can be set neither by a rising edge occurring when P16 data which is established when HOLD mode is entered is in the high state nor by a falling edge occurring when P16 data which is established when HOLD mode is entered is in the low state. Consequently, to release HOLD mode with P16, it is recommended that P16 be used in the double edge interrupt mode.

This bit must be cleared with an instruction as it is not cleared automatically.

INT2IE (bit 0): INT2 interrupt request enable

When this bit and INT2IF are set to 1, a HOLD mode release signal and an interrupt request to vector address 0013H are generated.

3.2.3.6 Input signal select register (ISL)

1) This register is a 5-bit register for controlling the timer 0 input and noise filter time constant.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE5F	00HH H000	R/W	ISL	ST0HCP	ST0LCP	-	-	-	NFSEL	NFON	ST0IN

ST0HCP (bit 7): Timer 0H capture signal input port select

This bit selects the timer 0H capture signal input port.

When set to 1, a timer 0H capture signal is generated when an input that satisfies the INT1 interrupt detection conditions is supplied to P17. If the INT1 interrupt detection mode is set to level detection, capture signals are generated at an interval of 1 Tcyc as long as the detection level is present at P17.

When this bit is set to 0, a timer 0H capture signal is generated when an input that satisfies the INT3 interrupt detection conditions is supplied to P17.

ST0LCP (bit 6): Timer 0L capture signal input port select

This bit selects the timer 0L capture signal input port.

When set to 1, a timer 0L capture signal is generated when an input that satisfies the INT0 interrupt detection conditions is supplied to P70. If the INT0 interrupt detection mode is set to level detection, capture signals are generated at an interval of 1 Tcyc as long as the detection level is present at P70.

When this bit is set to 0, a timer 0L capture signal is generated when an input that satisfies the INT2 interrupt detection conditions is supplied to P16.

NFSEL (bit 2): Noise filter time constant select

NFON (bit 1): Noise filter time constant select

NFSEL	NFON	Noise Filter Time Constant
0	0	1 Tcyc
0	1	128 Tcyc
1	0	1 Tcyc
1	1	32 Tcyc

ST0IN (bit 0): Timer 0 count clock input port select

This bit selects the timer 0 count clock signal input port.

When set to 1, a timer 0 count clock is generated when an input that satisfies the INT3 interrupt detection conditions is supplied to P15.

When this bit is set to 0, a timer 0 count clock is generated when an input that satisfies the INT2 interrupt detection conditions is supplied to P16.

Note: If timer 0L capture signal input or timer 0H capture signal input for INT4 is assigned to P70 and P17 to P15 at the same time, the signal from port 7 and port 1 are ignored.

3.2.4 Options

Two user options are available.

1) CMOS output (with a programmable pull-up resistor)
2) N-channel open drain output (with a programmable pull-up resistor)

3.2.5 HALT and HOLD Mode Operation

When in HALT or HOLD mode, port 1 retains the state that is established when HALT or HOLD mode is entered.

3.3 Port 2

3.3.1 Overview

Port 2 is a 2-bit I/O port equipped with programmable pull-up resistors. It is made up of a data latch, a data direction register, and a control circuit. Control of the input/output signal direction is accomplished by the data direction register in 1-bit units.

Port 2 can also serve as an input port for external interrupts. It can also be used as an input port for the timer 0 capture signal input or HOLD mode release signal input.

As a user option, either CMOS output with a programmable pull-up resistor or N-channel open drain output with a programmable pull-up resistor can be selected as the output type in 1-bit units.

3.3.2 Functions

1) Input/output port (2 bits: P20 and P21)
   - The port 2 data latch (P2: FE48) is used to control port output data and the port 2 data direction register (P2DDR: FE49) to control the I/O direction of port data.
   - Each port is provided with a programmable pull-up resistor.

2) Interrupt input pin function

   The port (INT4) selected out of P20 and P21 is provided with a pin interrupt function. This function detects a low edge, a high edge, or both edges and sets the interrupt flag. These two selected ports can also be used as timer 0 capture signal input.

3) Hold mode release function
   - When the interrupt flag and interrupt enable flag are set by INT4, a HOLD mode release signal is generated, releasing HOLD mode. The CPU then enters HALT mode (medium-speed RC oscillator selected as system clock). When the interrupt is accepted, the CPU switches from HALT mode to normal operation mode.
   - When a signal change that sets the INT4 interrupt flag is input in HOLD mode, the interrupt flag is set. In this case, HOLD mode is released if the corresponding interrupt enable flag is set.

     The interrupt flag, however, cannot be set by a rising edge occurring when INT4 data that is established when HOLD mode is entered is in the high state or by a falling edge occurring when INT4 data that is established when HOLD mode is entered is in the low state. Consequently, to release HOLD mode with INT4, it is recommended that INT4 be used in the double edge interrupt mode.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE48	HHHH HH00	R/W	P2	-	-	-	-	-	-	P21	P20
FE49	HHHH HH00	R/W	P2DDR	-	-	-	-	-	-	P21DDR	P20DDR
FE4A	0000 0000	R/W	I45CR	FIX0	FIX0	FIX0	FIX0	INT4HEG	INT4LEG	INT4IF	INT4IE
FE4B	0000 0000	R/W	I45SL	FIX0	FIX0	FIX0	FIX0	I4SL3	I4SL2	I4SL1	I4SL0

3.3.3 Related Registers

3.3.3.1 Port 2 data latch (P2)

1) The port 2 data latch is a 2-bit register for controlling port 2 output data and pull-up resistors.
2) When this register is read with an instruction, data at pins P20 and P21 is read in. If P2 (FE48) is manipulated using the NOT1, CLR1, SET1, DBZ, DBNZ, INC, or DEC instruction, the contents of the register are referenced instead of the data at the port pins.
3) Port 2 data can always be read regardless of the I/O state of the port.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE48	HHHH HH00	R/W	P2	-	-	-	-	-	-	P21	P20

3.3.3.2 Port 2 data direction register (P2DDR)

1) This register is a 2-bit register that controls the I/O direction of port 2 data in 1-bit units. Port P2n is placed in output mode when bit P2nDDR is set to 1 and in input mode when bit P2nDDR is set to 0.
2) When bit P2nDDR is set to 0 and bit P2n of the port 2 data latch is set to 1, port P2n is an input with a pull-up resistor

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE49	HHHH HH00	R/W	P2DDR	-	-	-	-	-	-	P21DDR	P20DDR

Register Data		Port P2n State		Internal Pull-up Resistor
P2n	P2nDDR	Input	Output	
0	0	Enabled	Open	OFF
1	0	Enabled	Internal pull-up resistor	ON
0	1	Enabled	Low	OFF
1	1	Enabled	High/open (CMOS/N-channel open drain)	OFF

3.3.3.3 External interrupt 4/5 control register (I45CR)

1) This register is an 8-bit register for controlling external interrupts 4 and 5.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE4A	0000 0000	R/W	I45CR	FIX0	FIX0	FIX0	FIX0	INT4HEG	INT4LEG	INT4IF	INT4IE

FIX0 (bit 7) to FIX0 (bit 4): These bits must always be set to 0.

INT4HEG (bit 3): INT4 rising edge detection control

INT4LEG (bit 2): INT4 falling edge detection control

INT4HEG	INT4LEG	INT4 Interrupt Conditions (Pin Data)
0	0	No edge detected
0	1	Falling edge detected
1	0	Rising edge detected
1	1	Both edges detected

INT4IF (bit 1): INT4 interrupt source flag

This bit is set when the conditions specified by INT4HEG and INT4LEG are satisfied.

When this bit and the INT4 interrupt request enable bit (INT4IE) are set to 1, a HOLD mode release signal and an interrupt request to vector address 0013H are generated.

The interrupt flag, however, cannot be set by a rising edge occurring when INT4 data which is established when HOLD mode is entered is in the high state or by a falling edge occurring when INT4 data which is established when HOLD mode is entered is in the low state. Consequently, to release HOLD mode with INT4, it is recommended that INT4 be used in the double edge interrupt mode.

This bit must be cleared with an instruction as it is not cleared automatically.

INT4IE (bit 0): INT4 interrupt request enable

When this bit and INT4IF are set to 1, a HOLD mode release signal and an interrupt request to vector address 0013H are generated.

3.3.3.4 External interrupt 4/5 pin select register (I45SL)

1) This register is an 8-bit register used to select the pin for the external interrupts 4 and 5.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE4B	0000 0000	R/W	I45SL	FIX0	FIX0	FIX0	FIX0	I4SL3	I4SL2	I4SL1	I4SL0

FIX0 (bits 7 to 4): These bits must always be set to 0.

I4SL3 (bit 3): INT4 pin select

I4SL2 (bit 2): INT4 pin select

I4SL3	I4SL2	Pin Assigned to INT4
0	0	Port P20
0	1	Port P21
1	0	Inhibited
1	1	Inhibited

I4SL1 (bit 1): INT4 pin function select

I4SL0 (bit 0): INT4 pin function select

When the data change specified in the external interrupt 4/5 control register (I45CR) is given to the pin that is assigned to INT4, timer 0 capture signal is generated.

I4SL1	I4SL0	Function Other Than INT4 Interrupt
0	0	None
0	1	None
1	0	Timer 0L capture signal input
1	1	Timer 0H capture signal input

Notes:

1) If timer 0L capture signal input and timer 0H capture signal input for INT4 are assigned to P70 or P17 to P15 at the same time, the signal from port 7 or port 1 is ignored.

3.3.4 Options

Two user options are available.

1) CMOS output (with a programmable pull-up resistor)
2) N-channel open drain output (with a programmable pull-up resistor)

3.3.5 HALT and Hold Mode Operation

When in HALT or HOLD mode, port 2 retains the state that is established when HALT or HOLD mode is entered.

3.4 Port 7

3.4.1 Overview

Port 7 is a 1-bit I/O port equipped with programmable pull-up resistors. It is made up of a data control latch and a control circuit.

Port 7 can be used as an input port for external interrupts. It can also be used as an input port for a capture signal input or HOLD mode release signal input.

There is no user option for this port.

3.4.2 Functions

1) Input/output port (1 bit: P70)
   - Bit 0 of the port 7 control register (P7: FE5C) is used to control the port output data and bit 4 to control the I/O direction of the port data.
   - P70 is of the N-channel open drain output type.
   - The port is provided with a programmable pull-up resistor.

2) Interrupt input pin function
   - P70 is assigned to INT0 and used to detect a low or high level, or a low or high edge and to set the interrupt flag.

3) Timer 0L capture input function

   A timer 0L capture signal is generated each time a signal change that sets the interrupt flag is supplied to the port selected from P70 and P16.

   When a selected level of signal is input to P70 that is specified for level-triggered interrupts, a timer 0L capture signal is generated at 1 cycle interval for the duration of the input signal.

4) HOLD mode release function
   - When the interrupt flag and interrupt enable flag are set by INT0, a HOLD mode release signal is generated, releasing HOLD mode. The CPU then enters HALT mode (medium-speed RC oscillator selected as system clock). When the interrupt is accepted, the CPU switches from HALT mode to normal operating mode.
   - When a signal change such that sets the interrupt flag is input to P70 in HOLD mode, the interrupt flag is set. In this case, HOLD mode is released if the corresponding interrupt enable flag is set.

5) Multiplexed pin function

   P70 is also used as the AN8 analog input pin.

	Input	Output	Interrupt Input Signal Detection	Timer 0 Count Input	Capture Input	HOLD Mode Release
P70	With a programmable pull-up resistor	N-channel open drain	L level, H level, L edge, H edge	–	Timer 0L	Enabled (Note)

Note: P70 HOLD mode release is available only when level detection is set.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE5C	HHH0 HHH0	R/W	P7	-	-	-	P70DDR	-	-	-	P70
FE5D	0000 0000	R/W	I01CR	INT1LH	INT1LV	INT1IF	INT1IE	INT0LH	INT0LV	INT0IF	INT0IE
FE5E	0000 0000	R/W	I23CR	INT3HEG	INT3LEG	INT3IF	INT3IE	INT2HEG	INT2LEG	INT2IF	INT2IE
FE5F	00HH H000	R/W	ISL	ST0HCP	ST0LCP	-	-	-	NFSEL	NFON	ST0IN

3.4.3 Related Registers

3.4.3.1 Port 7 control register (P7)

1) This register is a 2-bit register for controlling the I/O of port 7 data and pull-up resistors.
2) When this register is read with an instruction, data at pin P70 is read into bit 0. Bit 4 is loaded with bit 4 of register P7. If P7 (FE5C) is manipulated using the NOT1, CLR1, SET1, DBZ, DBNZ, INC, or DEC instruction, the contents of the register are referenced as bit 0 instead of the data at port pins.
3) Port 7 data can always be read regardless of the I/O state of the port.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE5C	HHH0 HHH0	R/W	P7	-	-	-	P70DDR	-	-	-	P70DT

Register Data		Port P70 State		Internal Pull-up Resistor
P70DT	P70DDR	Input	Output	
0	0	Enabled	Open	OFF
1	0	Enabled	Internal pull-up resistor	ON
0	1	Enabled	Low	OFF
1	1	Enabled	Open	ON

(Bits 7 to 5): These bits do not exist. They are always read as 1.

P70DDR (bit 4): P70 I/O control

A 1 or 0 in this bit controls the output (N-channel open drain)/input mode of the pin P70.

(Bits 3 to 1): These bits do not exist. They are always read as 1.

P70DT (bit 0): P70 data

The value of this bit is output from pin P70 when P70DDR is set to 1. Since this bit is of N-channel open drain output type, however, it is placed in the high-impedance state when P70DT is set to 1.

A 1 or 0 in this bit turns on or off the internal pull-up resistor for pin P70.

3.4.3.2 External interrupt 0/1 control register (I01CR)

1) This register is an 8-bit register for controlling external interrupts 0 and 1.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE5D	0000 0000	R/W	I01CR	INT1LH	INT1LV	INT1IF	INT1IE	INT0LH	INT0LV	INT0IF	INT0IE

INT1LH (bit 7): INT1 detection polarity select

INT1LV (bit 6): INT1 detection level/edge select

INT1LH	INT1LV	INT1 Interrupt Conditions (P17 Pin Data)
0	0	Falling edge detected
0	1	Low level detected
1	0	Rising edge detected
1	1	High level detected

INT1IF (bit 5): INT1 interrupt source flag

This bit is set when the conditions specified by INT1LH and INT1LV are satisfied. When this bit and the INT1 interrupt request enable bit (INT1IE) are set to 1, a HOLD mode release signal and an interrupt request to vector address 000BH are generated.

This bit must be cleared with an instruction as it is not cleared automatically.

INT1IE (bit 4): INT1 interrupt request enable

When this bit and INT1IF are set to 1, a HOLD mode release signal and an interrupt request to vector address 000BH are generated.

INT0LH (bit 3): INT0 detection polarity select

INT0LV (bit 2): INT0 detection level/edge select

INT0LH	INT0LV	INT0 Interrupt Conditions (P70 Pin Data)
0	0	Falling edge detected
0	1	Low level detected
1	0	Rising edge detected
1	1	High level detected

INT0IF (bit 1): INT0 interrupt source flag

This bit is set when the conditions specified by INT0LH and INT0LV are satisfied. When this bit and the INT0 interrupt request enable bit (INT0IE) are set to 1, a HOLD mode release signal and an interrupt request to vector address 0003H are generated.

This bit must be cleared with an instruction as it is not cleared automatically.

INT0IE (bit 0): INT0 interrupt request enable

When this bit and INT0IF are set to 1, a HOLD mode release signal and an interrupt request to vector address 0003H are generated.

Note: INT0 HOLD mode release is available only when level detection is set.

3.4.3.3 External interrupt 2/3 control register (I23CR)

1) This register is an 8-bit register for controlling external interrupts 2 and 3.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE5E	0000 0000	R/W	I23CR	INT3HEG	INT3LEG	INT3IF	INT3IE	INT2HEG	INT2LEG	INT2IF	INT2IE

INT3HEG (bit 7): INT3 rising edge detection control

INT3LEG (bit 6): INT3 falling edge detection control

INT3HEG	INT3LEG	INT3 Interrupt Conditions (P15 Pin Data)
0	0	No edge detected
0	1	Falling edge detected
1	0	Rising edge detected
1	1	Both edges detected

INT3IF (bit 5): INT3 interrupt source flag

This bit is set when the conditions specified by INT3HEG and INT3LEG are satisfied. When this bit and the INT3 interrupt request enable bit (INT3IE) are set to 1, an interrupt request to vector address 001BH is generated.

This bit must be cleared with an instruction as it is not cleared automatically.

INT3IE (bit 4): INT3 interrupt request enable

When this bit and INT3IF are set to 1, an interrupt request to vector address 001BH is generated.

INT2HEG (bit 3): INT2 rising edge detection control

INT2LEG (bit 2): INT2 falling edge detection control

INT2HEG	INT2LEG	INT2 Interrupt Conditions (P16 Pin Data)
0	0	No edge detected
0	1	Falling edge detected
1	0	Rising edge detected
1	1	Both edges detected

INT2IF (bit 1): INT2 interrupt source flag

This bit is set when the conditions specified by INT2HEG and INT2LEG are satisfied.

When this bit and the INT2 interrupt request enable bit (INT2IE) are set to 1, a HOLD mode release signal and an interrupt request to vector address 0013H are generated.

The interrupt flag, however, cannot be set by a rising edge occurring when P16 data which is established when HOLD mode is entered is in the high state or by a falling edge occurring when P16 data which is established when HOLD mode is entered is in the low state. Consequently, to release HOLD mode with P16, it is recommended that P16 be used in the double edge interrupt mode.

This bit must be cleared with an instruction as it is not cleared automatically.

INT2IE (bit 0): INT2 interrupt request enable

When this bit and INT2IF are set to 1, a HOLD mode release signal and an interrupt request to vector address 0013H are generated.

3.4.3.4 Input signal select register (ISL)

1) This register is a 5-bit register for controlling the timer 0 input and noise filter time constant.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE5F	00HH H000	R/W	ISL	ST0HCP	ST0LCP	-	-	-	NFSEL	NFON	ST0IN

ST0HCP (bit 7): Timer 0H capture signal input port select

This bit selects the timer 0H capture signal input port.

When set to 1, a timer 0H capture signal is generated when an input that satisfies the INT1 interrupt detection conditions is supplied to P17. If the INT1 interrupt detection mode is set to level detection, capture signals are generated at an interval of 1 Tcyc as long as the detection level is present at P17.

When set to 0, a timer 0H capture signal is generated when an input that satisfies the INT3 interrupt detection conditions is supplied to P15.

ST0LCP (bit 6): Timer 0L capture signal input port select

This bit selects the timer 0L capture signal input port.

When set to 1, a timer 0L capture signal is generated when an input that satisfies the INT0 interrupt detection conditions is supplied to P70. If the INT0 interrupt detection mode is set to level detection, capture signals are generated at an interval of 1 Tcyc as long as the detection level is present at P70.

When set to 0, a timer 0L capture signal is generated when an input that satisfies the INT2 interrupt detection conditions is supplied to P16.

NFSEL (bit 2): Noise filter time constant select

NFON (bit 1): Noise filter time constant select

NFSEL	NFON	Noise Filter Time Constant
0	0	1 Tcyc
0	1	128 Tcyc
1	0	1 Tcyc
1	1	32 Tcyc

ST0IN (bit 0): Timer 0 count clock input port select

This bit selects the timer 0 count clock signal input port.

When set to 1, a timer 0 count clock is generated when an input that satisfies the INT3 interrupt detection conditions is supplied to P15.

When set to 0, a timer 0 count clock is generated when an input that satisfies the INT2 interrupt detection conditions is supplied to P16.

Note: If timer 0L capture signal input or timer 0H capture signal input for INT4 is assigned to P70 or P17 to P15 at the same time, the signal from port 7 and port 1 is ignored.

3.4.4 Options

There is no user option for port 7.

3.4.5 HALT and HOLD Mode Operation

The pull-up resistor to P70 is turned off.

3.5 Timer/Counter 0 (T0)

3.5.1 Overview

The timer/counter 0 (T0) incorporated in this series of microcontrollers is a 16-bit timer/counter that provides the following four functions:

1) Mode 0: 8-bit programmable timer with a programmable prescaler (with an 8-bit capture register) × 2 channels
2) Mode 1: 8-bit programmable timer with a programmable prescaler (with an 8-bit capture register) + 8-bit programmable counter (with an 8-bit capture register)
3) Mode 2: 16-bit programmable timer with a programmable prescaler (with a 16-bit capture register)
4) Mode 3: 16-bit programmable counter (with a 16-bit capture register)

3.5.2 Functions

1) Mode 0: 8-bit programmable timer with a programmable prescaler (with an 8-bit capture register) × 2 channels

- Two independent 8-bit programmable timers (T0L and T0H) run on the clock (with a period of 1 to 256 Tcyc) from an 8-bit programmable prescaler.
- The contents of T0L are captured into the capture register T0CAL on external input detection signals from the P70/INT0/T0LCP, P16/INT2/T0IN, and P20, P21 timer 0L capture input pins.
- The contents of T0H are captured into the capture register T0CAH on external input detection signals from the P17/INT1/T0HCP, P15/INT3/T0IN, and P20, P21 timer 0H capture input pins.

T0L period = (T0LR + 1) × (T0PRR + 1) × Tcyc
T0H period = (T0HR + 1) × (T0PRR + 1) × Tcyc
Tcyc = Period of cycle clock

2) Mode 1: 8-bit programmable timer with a programmable prescaler (with an 8-bit capture register) + 8-bit programmable counter (with an 8-bit capture register)

- T0L serves as an 8-bit programmable counter that counts the number of external input detection signals from the P16/INT2/T0IN and P15/INT3/T0IN pins.
- T0H serves as an 8-bit programmable timer that runs on the clock (with a period of 1 to 256 Tcyc) from an 8-bit programmable prescaler.
- The contents of T0L are captured into the capture register T0CAL on external input detection signals from the P70/INT0/T0LCP, P16/INT2/T0IN, and P20, P21 timer 0L capture input pins.
- The contents of T0H are captured into the capture register T0CAH on external input detection signals from the P17/INT1/T0HCP, P15/INT3/T0IN, and P20, P21 timer 0H capture input pins.

T0L period = (T0LR + 1)
T0H period = (T0HR + 1) × (T0PRR +1) × Tcyc

3) Mode 2: 16-bit programmable timer with a programmable prescaler (with a 16-bit capture register)

- Timer/counter 0 serves as a 16-bit programmable timer that runs on the clock (with a period of 1 to 256 Tcyc) from an 8-bit programmable prescaler.
- The contents of T0L and T0H are captured into the capture registers T0CAL and T0CAH at the same time on external input detection signals from the P17/INT1/T0HCP, P15/INT3/T0IN, and P20, P21 timer 0H capture input pins.

$$\text{T0 period} = ([\text{T0HR, T0LR}] + 1) \times (\text{T0PRR} + 1) \times \text{Tcyc}$$

16 bits

4) Mode 3: 16-bit programmable counter (with a 16-bit capture register)

- Timer/counter 0 serves as a 16-bit programmable counter that counts the number of external input detection signals from the P16/INT2/T0IN and P15/INT3/T0IN pins.
- The contents of T0L and T0H are captured into the capture registers T0CAL and T0CAH at the same time on external input detection signals from the P17/INT1/T0HCP, P15/INT3/T0IN, and P20, P21 timer 0H capture input pins.

$$\text{T0 period} = [\text{T0HR, T0LR}] + 1$$

16 bits

5) Interrupt generation

T0L or T0H interrupt request is generated at the counter interval for timer/counter T0L or T0H if the interrupt request enable bit is set.

6) Tt is necessary to manipulate the following special function registers to control timer/counter 0 (T0).

- T0CNT, T0PRR, T0L, T0H, T0LR, T0HR, T0CAL, T0CAH
- P7, ISL, I01CR, I23CR
- P2, P2DDR, I45CR, I45SL

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE10	0000 0000	R/W	T0CNT	T0HRUN	T0LRUN	T0LONG	T0LEXT	T0HCMP	T0HIE	T0LCMP	T0LIE
FE11	0000 0000	R/W	T0PRR	T0PRR7	T0PRR6	T0PRR5	T0PRR4	T0PRR3	T0PRR2	T0PRR1	T0PRR0
FE12	0000 0000	R	T0L	T0L7	T0L6	T0L5	T0L4	T0L3	T0L2	T0L1	T0L0
FE13	0000 0000	R	T0H	T0H7	T0H6	T0H5	T0H4	T0H3	T0H2	T0H1	T0H0
FE14	0000 0000	R/W	T0LR	T0LR7	T0LR6	T0LR5	T0LR4	T0LR3	T0LR2	T0LR1	T0LR0
FE15	0000 0000	R/W	T0HR	T0HR7	T0HR6	T0HR5	T0HR4	T0HR3	T0HR2	T0HR1	T0HR0
FE16	XXXX XXXX	R	T0CAL	T0CAL7	T0CAL6	T0CAL5	T0CAL4	T0CAL3	T0CAL2	T0CAL1	T0CAL0
FE17	XXXX XXXX	R	T0CAH	T0CAH7	T0CAH6	T0CAH5	T0CAH4	T0CAH3	T0CAH2	T0CAH1	T0CAH0

3.5.3 Circuit Configuration

3.5.3.1 Timer/counter 0 control register (T0CNT) (8-bit register)

1) This register controls the operation and interrupts of T0L and T0H.

3.5.3.2 Programmable prescaler match register (T0PRR) (8-bit register)

1) This register stores the match data for the programmable prescaler.

3.5.3.3 Programmable prescaler (8-bit counter)

1) Start/stop: This register runs in modes other than HOLD mode.
2) Count clock: Cycle clock (period = 1 Tcyc).
3) Match signal: A match signal is generated when the count value matches the value of register T0PRR (period: 1 to 256 Tcyc).
4) Reset: The counter starts counting from 0 when a match signal occurs or when data is written into T0PRR.

3.5.3.4 Timer/counter 0 low byte (T0L) (8-bit counter)

1) Start/stop: This counter is stopped and started by the 0/1 value of T0LRUN (timer 0 control register, bit 6).
2) Count clock: Either a prescaler match signal or an external signal can be selected through the 0/1 value of T0LEXT (timer 0 control register, bit 4).
3) Match signal: A match signal is generated when the count value matches the value of the match buffer register (16 bits of data needs to match in the 16-bit mode).
4) Reset: When the counter stops operation or a match signal is generated.

3.5.3.5 Timer/counter 0 high byte (T0H) (8-bit counter)

1) Start/stop: This counter is stopped and started by the 0/1 value of T0HRUN (timer 0 control register, bit 7).
2) Count clock: Either prescaler match signal or T0L match signal can be selected through the 0/1 value of T0LONG (timer 0 control register, bit 5).
3) Match signal: A match signal is generated when the count value matches the value of the match buffer register (16 bits of data needs to match in the 16-bit mode).
4) Reset: When the counter stops operation or a match signal is generated.

3.5.3.6 Timer/counter 0 match data register low byte (T0LR) (8-bit register with a match buffer register)

1) This register is used to store the match data for T0L. It has an 8-bit match buffer register. A match signal is generated when the value of this match buffer register matches the value of the lower-order byte of timer/counter 0 (16 bits of data needs to match in the 16-bit mode).
2) The match buffer register is updated as follows:
   - When it is inactive (T0LRUN=0), the match register matches T0LR.
   - When it is active (T0LRUN=1), the match buffer register is loaded with the contents of T0LR when a match signal is generated.

3.5.3.7 Timer/counter 0 match data register high byte (T0HR) (8-bit register with a match buffer register)

1) This register is used to store the match data for T0H. It has an 8-bit match buffer register. A match signal is generated when the value of this match buffer register matches the value of the higher-order byte of timer/counter 0 (16 bits of data needs to match in the 16-bit mode).
2) The match buffer register is updated as follows:
   - When it is inactive (T0HRUN=0), the match register matches T0HR.
   - When it is active (T0HRUN=1), the match buffer register is loaded with the contents of T0HR when a match signal is generated.

3.5.3.8 Timer/counter 0 capture register low byte (T0CAL) (8-bit register)

1) Capture clock: External input detection signals from the P70/INT0/T0LCP, P16/INT2/T0IN, and P20, P21 timer 0L capture input pins when T0LONG (timer 0 control register, bit 5) is set to 0.

   External input detection signals from the P17/INT1/T0HCP, P15/INT3/T0IN, and P20, P21 timer 0H capture input pins when T0LONG (timer 0 control register, bit 5) is set to 1.

2) Capture data: Contents of timer/counter 0 low byte (T0L).

3.5.3.9 Timer/counter 0 capture register high byte (T0CAH) (8-bit register)

1) Capture clock: External input detection signals from the P17/INT1/T0HCP, P15/INT3/T0IN, and P20, P21 timer 0H capture input pins.

2) Capture data: Contents of timer/counter 0 high byte (T0H)

Table 3.5.1 Timer 0 (T0H, T0L) Count Clocks

Mode	T0LONG	T0LEXT	T0H Count Clock	T0L Count Clock	[T0H, T0L] Count Clock
0	0	0	T0PRR match signal	T0PRR match signal	–
1	0	1	T0PRR match signal	External signal	–
2	1	0	–	–	T0PRR match signal
3	1	1	–	–	External signal

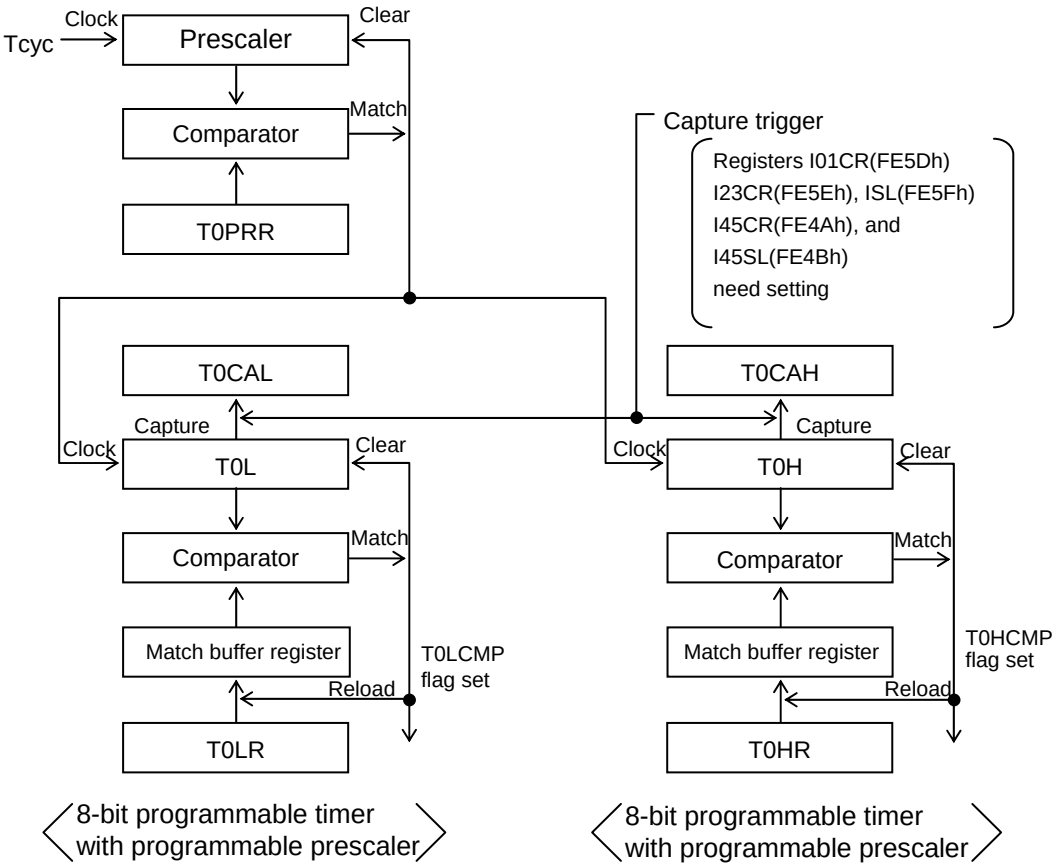


Figure 3.5.1 Mode 0 Block Diagram (T0LONG =0 , T0LEXT = 0)

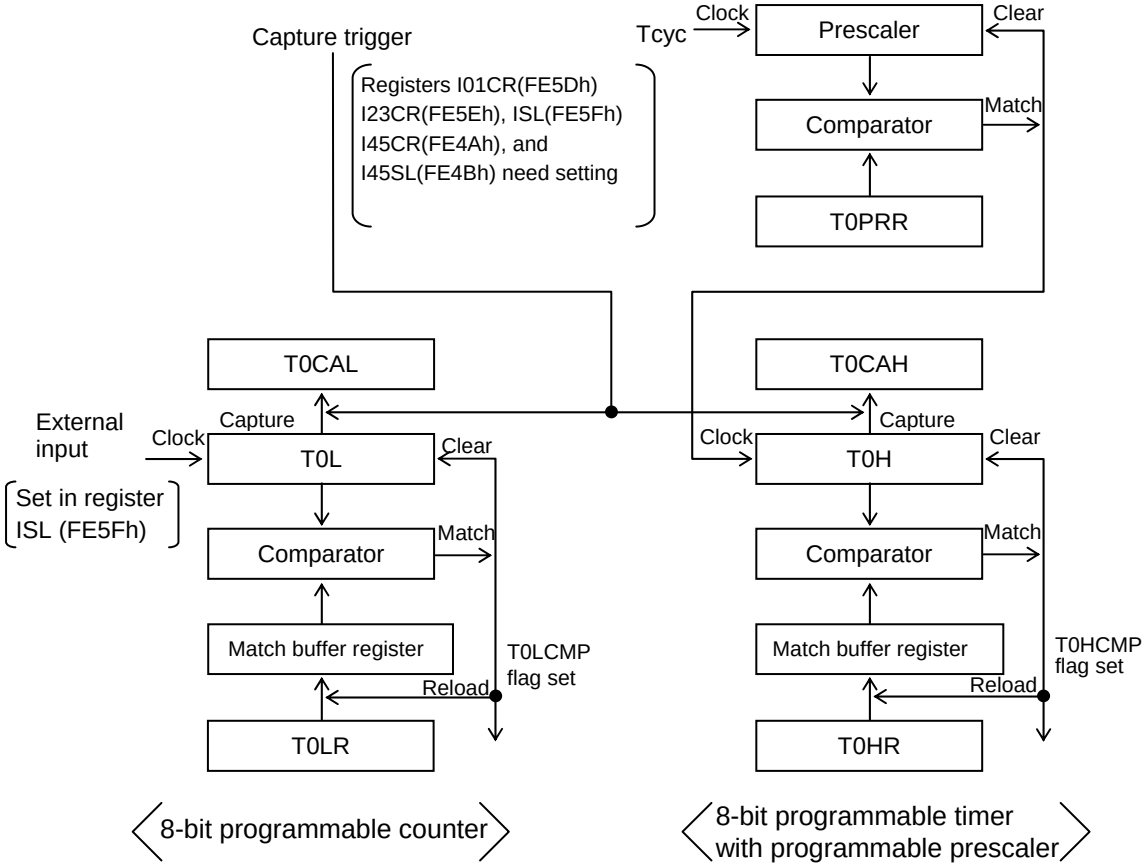


Figure 3.5.2 Mode 1 Block Diagram (T0LONG = 0, T0LEXT = 1)

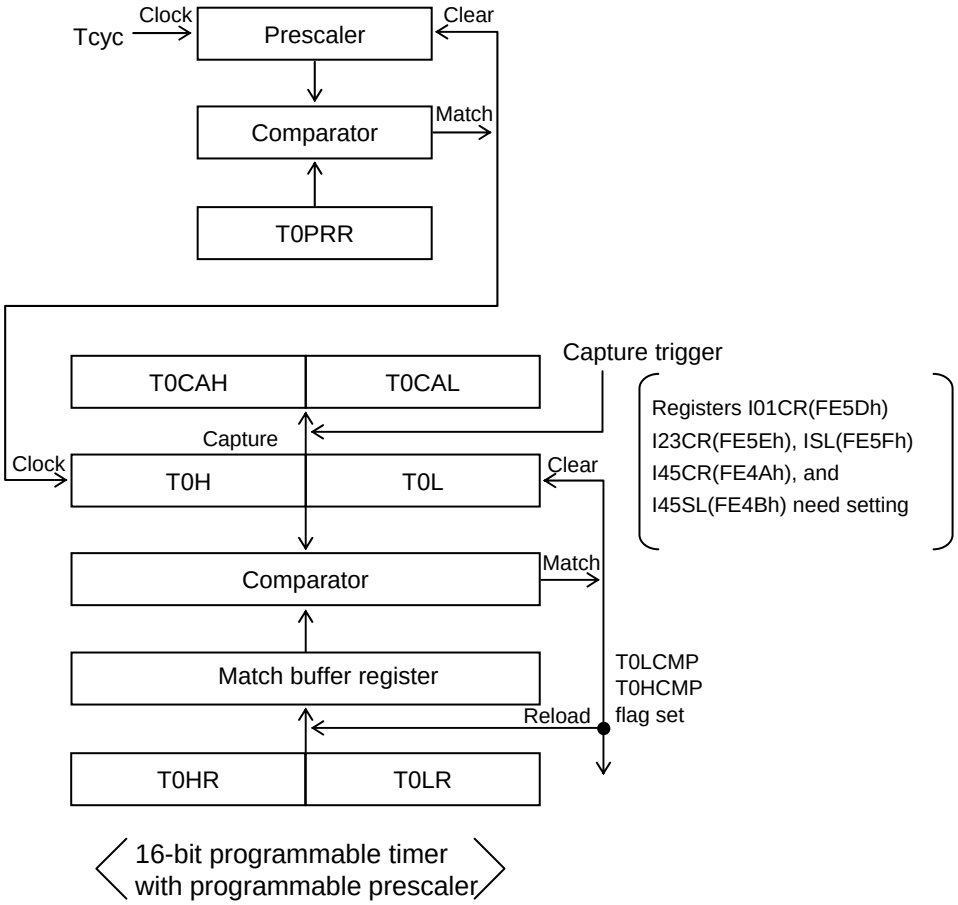


Figure 3.5.3 Mode 2 Block Diagram (T0LONG = 1, T0LEXT = 0)

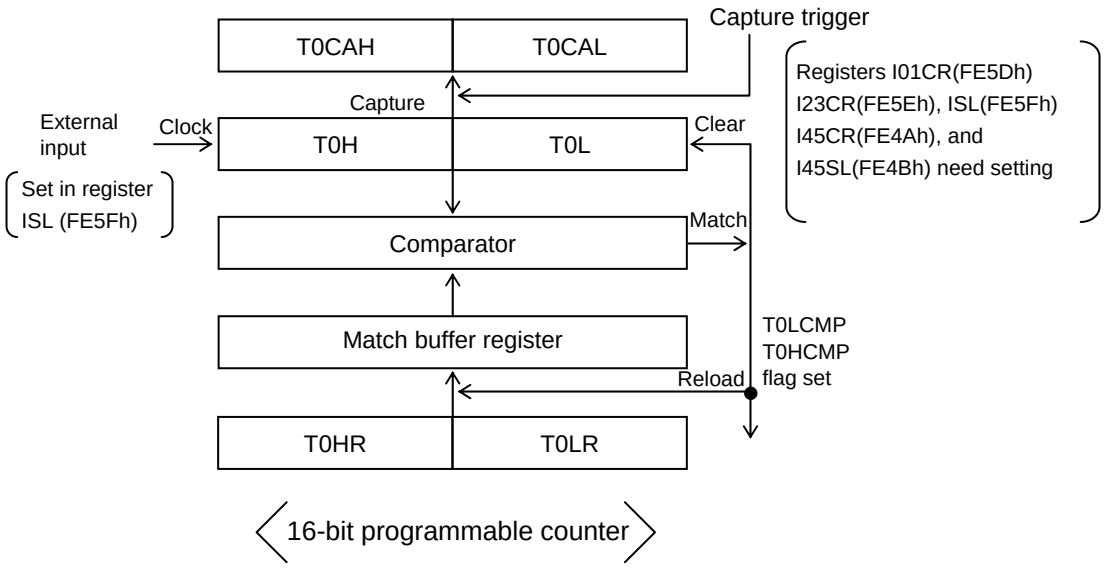


Figure 3.5.4 Mode 3 Block Diagram (T0LONG = 1, T0LEXT = 1)

3.5.4 Related Registers

3.5.4.1 Timer/counter 0 control register (T0CNT)

1) This register is an 8-bit register that controls the operation and interrupts of T0L and T0H.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE10	0000 0000	R/W	T0CNT	T0HRUN	T0LRUN	T0LONG	T0LEXT	T0HCMP	T0HIE	T0LCMP	T0LIE

T0HRUN (bit 7): T0H count control

When this bit is set to 0, timer/counter 0 high byte (T0H) stops on a count value of 0. The match buffer register of T0H has the same value as T0HR.

When this bit is set to 1, timer/counter 0 high byte (T0H) performs the required counting operation. The match buffer register of T0H is loaded with the contents of T0HR when a match signal is generated.

T0LRUN (bit 6): T0L count control

When this bit is set to 0, timer/counter 0 low byte (T0L) stops on a count value of 0. The match buffer register of T0L has the same value as T0LR.

When this bit is set to 1, timer/counter 0 low byte (T0L) performs the required counting operation. The match buffer register of T0L is loaded with the contents of T0LR when a match signal is generated.

T0LONG (bit 5): Timer/counter 0 bit length select

When this bit is set to 0, timer/counter 0 higher- and lower-order bytes serve as independent 8-bit timers/counters.

When this bit is set to 1, timer/counter 0 functions as a 16-bit timer/counter. A match signal is generated when the count value of the 16-bit counter comprising T0H and T0L matches the contents of the match buffer register of T0H and T0L.

T0LEXT (bit 4): T0L input clock select

When this bit is set to 0, the count clock of T0L is the match signal for the prescaler.

When this bit is set to 1, the count clock of T0L is an external input signal.

T0HCMP (bit 3): T0H match flag

This bit is set when the value of T0H matches the value of the match buffer register for T0H and a match signal is generated while T0H is running (T0HRUN=1). Its state does not change if no match signal is generated. Consequently, this flag must be cleared with an instruction.

In the 16-bit mode (T0LONG=1), a match needs to occur in all 16 bits of data for a match signal to occur.

T0HIE (bit 2): T0H interrupt request enable control

When this bit and T0HCMP are set to 1, an interrupt request to vector address 0023H is generated.

T0LCMP (bit 1): T0L match flag

This bit is set when the value of T0L matches the value of the match buffer register for T0L and a match signal is generated while T0L is running (T0LRUN=1). Its state does not change if no match signal is generated. Consequently, this flag must be cleared with an instruction.

In the 16-bit mode (T0LONG=1), a match needs to occur in all 16 bits of data for a match signal to occur.

T0LIE (bit 0): T0L interrupt request enable control

When this bit and T0LCMP are set to 1, an interrupt request to vector address 0013H is generated.

Notes:

- *T0HCMP and T0LCMP must be cleared to 0 with an instruction.*
- *When the 16-bit mode is to be used, T0LRUN and T0HRUN must be set to the same value to control operation.*
- *T0LCMP and T0HCMP are set at the same time in the 16-bit mode.*

3.5.4.2 Timer 0 programmable prescaler match register (T0PRR)

1) This register is an 8-bit register that is used to define the clock period (Tpr) of timer/counter 0.
2) The count value of the prescaler starts at 0 when T0PRR is loaded with data.
3) Tpr = (T0PRR+1) × Tcyc Tcyc = Period of cycle clock

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE11	0000 0000	R/W	T0PRR	T0PRR7	T0PRR6	T0PRR5	T0PRR4	T0PRR3	T0PRR2	T0PRR1	T0PRR0

3.5.4.3 Timer/counter 0 low byte (T0L)

1) This is a read-only 8-bit timer/counter. It counts the number of match signals from the prescaler or external signals.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE12	0000 0000	R	T0L	T0L7	T0L6	T0L5	T0L4	T0L3	T0L2	T0L1	T0L0

3.5.4.4 Timer/counter 0 high byte (T0H)

1) This is a read-only 8-bit timer/counter. It counts the number of match signals from the prescaler or overflow occurring in T0L.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE13	0000 0000	R	T0H	T0H7	T0H6	T0H5	T0H4	T0H3	T0H2	T0H1	T0H0

3.5.4.5 Timer/counter 0 match data register low byte (T0LR)

1) This register is used to store the match data for T0L. It has an 8-bit match buffer register. A match signal is generated when the value of this match buffer register matches the value of the lower-order byte of timer/counter 0 (16 bits of data needs to match in the 16-bit mode).
2) The match buffer register is updated as follows:
   - When it is inactive (T0LRUN=0), the match register matches T0LR.
   - When it is active (T0LRUN=1), the match buffer register is loaded with the contents of T0LR when a match signal is generated.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE14	0000 0000	R/W	T0LR	T0LR7	T0LR6	T0LR5	T0LR4	T0LR3	T0LR2	T0LR1	T0LR0

3.5.4.6 Timer/counter 0 match data register high byte (T0HR)

1) This register is used to store the match data for T0H. It has an 8-bit match buffer register. A match signal is generated when the value of this match buffer register matches the value of the higher-order byte of timer/counter 0 (16 bits of data needs to match in the 16-bit mode).

2) The match buffer register is updated as follows:

- When it is inactive (T0HRUN=0), the match register matches T0HR.
- When it is active (T0HRUN=1), the match buffer register is loaded with the contents of T0HR when a match signal is generated.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE15	0000 0000	R/W	T0HR	T0HR7	T0HR6	T0HR5	T0HR4	T0HR3	T0HR2	T0HR1	T0HR0

3.5.4.7 Timer/counter 0 capture register low byte (T0CAL)

1) This register is a read-only 8-bit register used to capture the contents of timer/counter 0 low byte (T0L) on an external input detection signal.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE16	XXXX XXXX	R	T0CAL	T0CAL7	T0CAL6	T0CAL5	T0CAL4	T0CAL3	T0CAL2	T0CAL1	T0CAL0

3.5.4.8 Timer/counter 0 capture register high byte (T0CAH)

1) This register is a read-only 8-bit register used to capture the contents of timer/counter 0 high byte (T0H) on an external input detection signal.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE17	XXXX XXXX	R	T0CAH	T0CAH7	T0CAH6	T0CAH5	T0CAH4	T0CAH3	T0CAH2	T0CAH1	T0CAH0

3.6 Timer 6 and Timer 7 (T6, T7)

3.6.1 Overview

The timer 6 (T6) and timer 7 (T7) incorporated in this series of microcontrollers are 8-bit timers with two independently controlled 6-bit prescalers.

3.6.2 Functions

1) Timer 6 (T6)

Timer 6 is an 8-bit timer that runs on either 4Tcyc, 16Tcyc, or 64Tcyc clock. It can generate, at pin P06, toggle waveforms whose frequency is equal to the period of timer 6.

$$\text{T6 period} = (\text{T6R} + 1) \times 4^{n}\text{Tcyc} \quad (n = 1, 2, 3)$$

Tcyc = Period of cycle clock

2) Timer 7 (T7)

Timer 7 is an 8-bit timer that runs on either 4Tcyc, 16Tcyc, or 64Tcyc clock. It can generate, at pin P07, toggle waveforms whose frequency is equal to the period of timer 7.

$$\text{T7 period} = (\text{T7R} + 1) \times 4^{n}\text{Tcyc} \quad (n = 1, 2, 3)$$

Tcyc = Period of cycle clock

3) Interrupt generation

An interrupt request to vector address 0043H is generated when the overflow flag is set at the interval of timer 6 or timer 7 period and the corresponding interrupt request enable bit is set.

4) It is necessary to manipulate the following special function registers to control the timer 6 (T6) and timer 7 (T7).

- T67CNT, T6R, T7R
- P0, P0DDR, P0FCR

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE78	0000 0000	R/W	T67CNT	T7C1	T7C0	T6C1	T6C0	T7OV	T7IE	T6OV	T6IE
FE7A	0000 0000	R/W	T6R	T6R7	T6R6	T6R5	T6R4	T6R3	T6R2	T6R1	T6R0
FE7B	0000 0000	R/W	T7R	T7R7	T7R6	T7R5	T7R4	T7R3	T7R2	T7R1	T7R0
FE42	00HH HHHH	R/W	P0FCR	T7OE	T6OE	-	-	-	-	-	-

3.6.3 Circuit Configuration

3.6.3.1 Timer 6/7 control register (T67CNT) (8-bit register)

1) This register controls the operation and interrupts of T6 and T7.

3.6.3.2 Timer 6 counter (T6CTR) (8-bit counter)

1) This counter counts the number of clocks from the timer 6 prescaler (T6PR). The value of timer 6 counter (T6CTR) reaches 0 on the clock following the clock that brought about the value specified in the timer 6 period setting register (T6R), when the interrupt flag (T6OV) is set.
2) When T6C0 and T6C1 (T67CNT: FE78, bits 4 and 5) are set to 0, the timer 6 counter stops at a count value of 0. In the other cases, the timer 6 counter continues operation.
3) When data is written into T6R while timer 6 is running, both the timer 6 prescaler and counter are cleared and start counting again.

3.6.3.3 Timer 6 prescaler (T6PR) (6-bit counter)

1) This prescaler is used to define the clock period for the timer 6 determined by T6C0 and T6C1. (T67CNT: FE78, bits 4 and 5).

Table 3.6.1 Timer 6 Count Clocks

T6C1	T6C0	T6 Count Clock
0	0	Timer 6 prescaler and timer/counter are reset.
0	1	4 Tcyc
1	0	16 Tcyc
1	1	64 Tcyc

3.6.3.4 Timer 6 period setting register (T6R) (8-bit register)

1) This register defines the clock period for timer 6.
2) When data is written into T6R while timer 6 is running, both the timer 6 prescaler and counter are cleared and start counting again.

3.6.3.5 Timer 7 counter (T7CTR) (8-bit counter)

1) This counter counts the number of clocks from the timer 7 prescaler (T7PR). The value of timer 7 counter (T7CTR) reaches 0 on the clock following the clock that brought about the value specified in the timer 7 period setting register (T7R), when the interrupt flag (T7OV) is set.
2) When T7C0 and T7C1 (T67CNT: FE78 bits 6 and 7) are set to 0, the timer 7 counter stops at a count value of 0. In the other cases, the timer 7 counter continues operation.
3) When data is written into T7R while timer 7 is running, both the timer 7 prescaler and counter are cleared and start counting again.

3.6.3.6 Timer 7 prescaler (T7PR) (6-bit counter)

1) This prescaler is used to define the clock period for the timer 7 determined by T7C0 and T7C1 (T67CNT: FE78 bits 6 and 7).

Table 3.6.2 Timer 7 Count Clocks

T7C1	T7C0	T7 Count Clock
0	0	Timer 7 prescaler and timer/counter are reset.
0	1	4 Tcyc
1	0	16 Tcyc
1	1	64 Tcyc

3.6.3.7 Timer 7 period setting register (T7R) (8-bit register)

1) This register defines the period of timer 7.
2) When data is written into T7R while timer 7 is running, both the timer 7 prescaler and counter are cleared and start counting again.

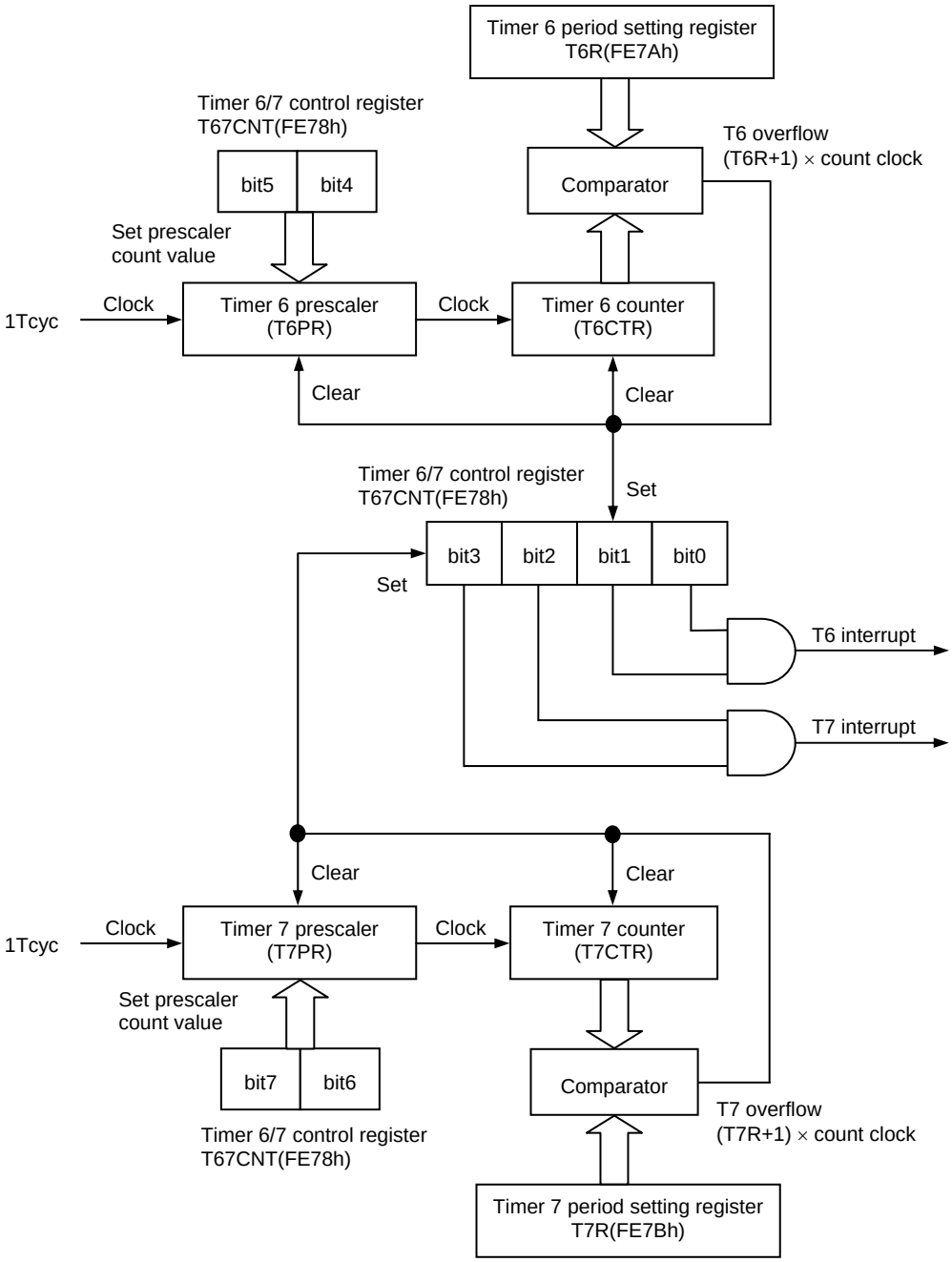


Figure 3.6.1 Timer 6/7 Block Diagram

3.6.4 Related Registers

3.6.4.1 Timer 6/7 control register (T67CNT)

1) This register is an 8-bit register that controls the operation and interrupts of T6 and T7.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE78	0000 0000	R/W	T67CNT	T7C1	T7C0	T6C1	T6C0	T7OV	T7IE	T6OV	T6IE

T7C1 (bit 7): T7 count clock control

T7C0 (bit 6): T7 count clock control

T7C1	T7C0	T7 Count Clock
0	0	Timer 7 prescaler and timer/counter are stopped in the reset state.
0	1	4 Tcyc
1	0	16 Tcyc
1	1	64 Tcyc

T6C1 (bit 5): T6 count clock control

T6C0 (bit 4): T6 count clock control

T6C1	T6C0	T6 Count Clock
0	0	Timer 6 prescaler and timer/counter are stopped in the reset state.
0	1	4 Tcyc
1	0	16 Tcyc
1	1	64 Tcyc

T7OV (bit 3): T7 overflow flag

This flag is set at the interval of timer 7 period when timer 7 is running.

This flag must be cleared with an instruction.

T7IE (bit 2): T7 interrupt request enable control

An interrupt request to vector address 0043H is generated when this bit and T7OV are set to 1.

T6OV (bit 1): T6 overflow flag

This flag is set at the interval of timer 6 period when timer 6 is running.

This flag must be cleared with an instruction.

T6IE (bit 0): T6 interrupt request enable control

An interrupt request to vector address 0043H is generated when this bit and T6OV are set to 1.

3.6.4.2 Timer 6 period setting register (T6R)

1) This register is an 8-bit register for defining the period of timer 6.

   Timer 6 period = (T6R value + 1) × Timer 6 prescaler value (4, 16 or 64 Tcyc)

2) When data is written into T6R while timer 6 is running, both the timer 6 prescaler and counter are cleared and start counting again.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE7A	0000 0000	R/W	T6R	T6R7	T6R6	T6R5	T6R4	T6R3	T6R2	T6R1	T6R0

3.6.4.3 Timer 7 period setting register (T7R)

1) This register is an 8-bit register for defining the period of timer 7.

   Timer 7 period = (T7R value + 1) × Timer 7 prescaler value (4, 16 or 64 Tcyc)

2) When data is written into T7R while timer 7 is running, both the timer 7 prescaler and counter are cleared and start counting again.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE7B	0000 0000	R/W	T7R	T7R7	T7R6	T7R5	T7R4	T7R3	T7R2	T7R1	T7R0

3.6.4.4 Port 0 function control register (P0FCR)

1) This register is a 2-bit register that controls the multiplexed output function of port 0 pins. It controls the toggle outputs of timer 6 and timer 7.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE42	00HH HHHH	R/W	P0FCR	T7OE	T6OE	-	-	-	-	-	-

T7OE (bit 7):

This flag is used to control the timer 7 toggle output at pin P07.

This flag is disabled when the pin P07 is in input mode.

When the pin P07 is in output mode:

A 0 in this bit outputs the value of the port data latch.

A 1 in this bit outputs the OR of the value of the port data latch and the waveform which toggles at the interval equal to the period of timer 7.

T6OE (bit 6):

This flag is used to control the timer 6 toggle output at pin P06.

This flag is disabled when pin P06 is in input mode.

When pin P06 is in output mode:

A 0 in this bit outputs the value of the port data latch.

A 1 in this bit outputs the OR of the value of the port data latch and the waveform which toggles at the interval equal to the period of timer 6.

3.7 Serial Interface 1 (SIO1)

3.7.1 Overview

The serial interface 1 (SIO1) incorporated in this series of microcontrollers provides the following four functions:

1) Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire system, transfer clock of 2 to 512 Tcyc)
2) Mode 1: Asynchronous serial (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 Tcyc baudrate)
3) Mode 2: Bus-master (start bit, 8 data bits, transfer clock of 2 to 512 Tcyc)
4) Mode 3: Bus-slave (start detection, 8 data bits, stop detection)

3.7.2 Functions

1) Mode 0: Synchronous 8-bit serial I/O
   - Performs 2- or 3-wire synchronous serial communication. The clock may be an internal or external clock.
   - The frequency of the internal clock is programmable within the range of 2 to 512 Tcyc.

2) Mode 1: Asynchronous serial (UART)
   - Performs half-duplex, 8 data bits, 1 stop bit asynchronous serial communication.
   - The baudrate is programmable within the range of 8 to 2048 Tcyc.

3) Mode 2: Bus-master
   - SIO1 is used as a bus master controller.
   - The start conditions are automatically generated but stop conditions must be generated by manipulating ports.
   - Clock synchronization is used. Since it is possible to verify the transfer-time bus data at the end of transfer, this mode can be combined with mode 3 to provide support for multi-master operation.
   - The period of the output clock is programmable within the range of 2 to 512 Tcyc.

4) Mode 3: Bus-slave
   - SIO1 is used as a slave device of the bus.
   - Start/stop condition detection processing is performed but the detection of an address match condition and the generation of an acknowledge require program intervention.
   - SIO1 can generate an interrupt by forcing the clock line to a low level on the falling edge of the eighth clock determined by the program.

5) Interrupt generation

   An interrupt request is generated at the end of communication if the interrupt request enable flag is set.

6) It is necessary to control the following special function registers to control serial interface 1 (SIO1).
   - SCON1, SBUF1, SBR1
   - P1, P1DDR, P1FCR

Address	Initial Value	R/W	Name	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE34	0000 0000	R/W	SCON1	-	SI1M1	SI1M0	SI1RUN	SI1REC	SI1DIR	SI1OVR	SI1END	SI1IE
FE35	00000 0000	R/W	SBUF1	SBUF18	SBUF17	SBUF16	SBUF15	SBUF14	SBUF13	SBUF12	SBUF11	SBUF10
FE36	0000 0000	R/W	SBR1	-	SBRG17	SBRG16	SBRG15	SBRG14	SBRG13	SBRG12	SBRG11	SBRG10

3.7.3 Circuit Configuration

3.7.3.1 SIO1 control register (SCON1) (8-bit register)

1) This register controls the operation and interrupts of SIO1.

3.7.3.2 SIO1 shift register (SIOSF1) (8-bit shift register)

1) This register is a shift register used to transfer and receive SIO1 data.
2) This register cannot be directly accessed with an instruction. It is accessed via SBUF1.

3.7.3.3 SIO1 data register (SBUF1) (9-bit register)

1) The lower-order 8 bits of SBUF1 are transferred to SIOSF1 at the beginning of data transfer.
2) At the end of data transfer, the contents of SIOSF1 are placed in the lower-order 8 bits of SBUF1. In modes 1, 2, and 3, since the 9th input data is placed in bit 8 of SBUF1, it is possible to check for a stop bit.

3.7.3.4 SIO1 baudrate generator register (SBR1) (8-bit reload counter)

1) This is a reload counter for generating internal clocks.
2) The generator can generate clocks of 2 to 512 Tcyc in modes 0 and 2 and clocks of 8 to 2048 Tcyc in mode 1.

Table 3.7.1 SIO1 Operations and Operating Modes

		Synchronous (Mode 0)		UART (Mode 1)		Bus Master (Mode 2)		Bus Slave (Mode 3)	
		Transfer SI1REC = 0	Receive SI1REC = 1	Transfer SI1REC = 0	Receive SI1REC = 1	Transfer SI1REC = 0	Receive SI1REC = 1	Transfer SI1REC = 0	Receive SI1REC = 1
Start bit		None	None	Output (Low)	Input (Low)	See 1) and 2) below	Not required	Not required	See 2) below
Data output		8 (Shift data)	8 (All 1s)	8 (Shift data)	8 (All 1s)	8 (Shift data)	8 (All 1s)	8 (Shift data)	8 (All 1s)
Data input		8 (Input pin)	←	8 (Input pin)	←	8 (Input pin)	←	8 (Input pin)	←
Stop bit		None	←	Output (High)	Input (H/L)	Input (H/L)	Output (SBUF1 bit8)	Input (H/L)	Output (L)
Clock		8	←	9 (Internal)	←	9	←	Low output on falling edge of 8th clock	←
Operation start		SI1RUN ↑	←	1) SI1RUN ↑ 2) Start bit detected	Start bit detected	1) No start bit on falling edge of SI1END when SI1RUN = 1 2) With start bit on rising edge of SI1RUN when SI1END = 0	1) on left side	1) on right side	1) Clock released on falling edge of SI1END when SI1RUN = 1 2) Start bit detected when SI1RUN = 0 and SI1END = 0
Period		2 to 512 Tcyc	←	8 to 2048 Tcyc	←	2 to 512Tcyc	←	2 to 512Tcyc	←
SI1RUN (bit 5)	Set	Instruction	←	1) Instruction 2) Start bit detected	Start bit detected	Instruction	Already set	Already set	Start bit detected
	Clear	End of processing	←	End of stop bit	←	1) Stop condition detected 2) When arbitration lost (Note 1)	←	1) Stop condition detected 2) Ack=1 detected	←
SI1END (bit 1)	Set	End of processing	←	End of stop bit	←	1) Rising edge of 9th clock 2) Stop condition detected	←	1) Falling edge of 8th clock 2) Stop condition detected	←
	Clear	Instruction	←	Instruction	←	Instruction	←	Instruction	←

Note 1: If internal data output state = "H" and data port state = "L" conditions are detected on the rising edges of the first to 8th clocks, the microcontroller recognizes a bus contention loss and clears SI1RUN (and also stops the generation of the clock immediately).

(Continued on next page)

Table 3.7.1 SIO1 Operations and Operating Modes (cont.)

		Synchronous (Mode 0)		UART (Mode 1)		Bus Master (Mode 2)		Bus Slave (Mode 3)	
		Transfer SI1REC=0	Receive SI1REC=1	Transfer SI1REC=0	Receive SI1REC=1	Transfer SI1REC=0	Receive SI1REC=1	Transfer SI1REC=0	Receive SI1REC=1
SI1OVR (bit 2)	Set	1) Falling edge of clock detected when SI1RUN=0 2) SI1END set conditions met when SI1END=1	←	1) Falling edge of clock detected when SI1RUN=0 2) SI1END set conditions met when SI1END=1	←	1) SI1END set conditions met when SI1END=1	←	1) Falling edge of clock detected when SI1RUN=0 2) SI1END set conditions met when SI1END=1 3) Start bit detected	←
	Clear	Instruction	←	Instruction	←	Instruction	←	Instruction	←
Shifter data update		SBUF1→ Shifter at beginning of operation	←	SBUF1→ Shifter at beginning of operation	←	SBUF1→ Shifter at beginning of operation	←	SBUF1→ Shifter at beginning of operation	←
Shifter→ SBUF1 (bits 0 to 7)		Rising edge of 8th clock	←	When 8-bit data transferred	When 8-bit data received	Rising edge of 8th clock	←	Rising edge of 8th clock	←
Automatic update of SBUF1, bit 8		None	←	Input data read in on stop bit	←	Input data read in on rising edge of 9th clock	←	Input data read in on rising edge of 9th clock	←

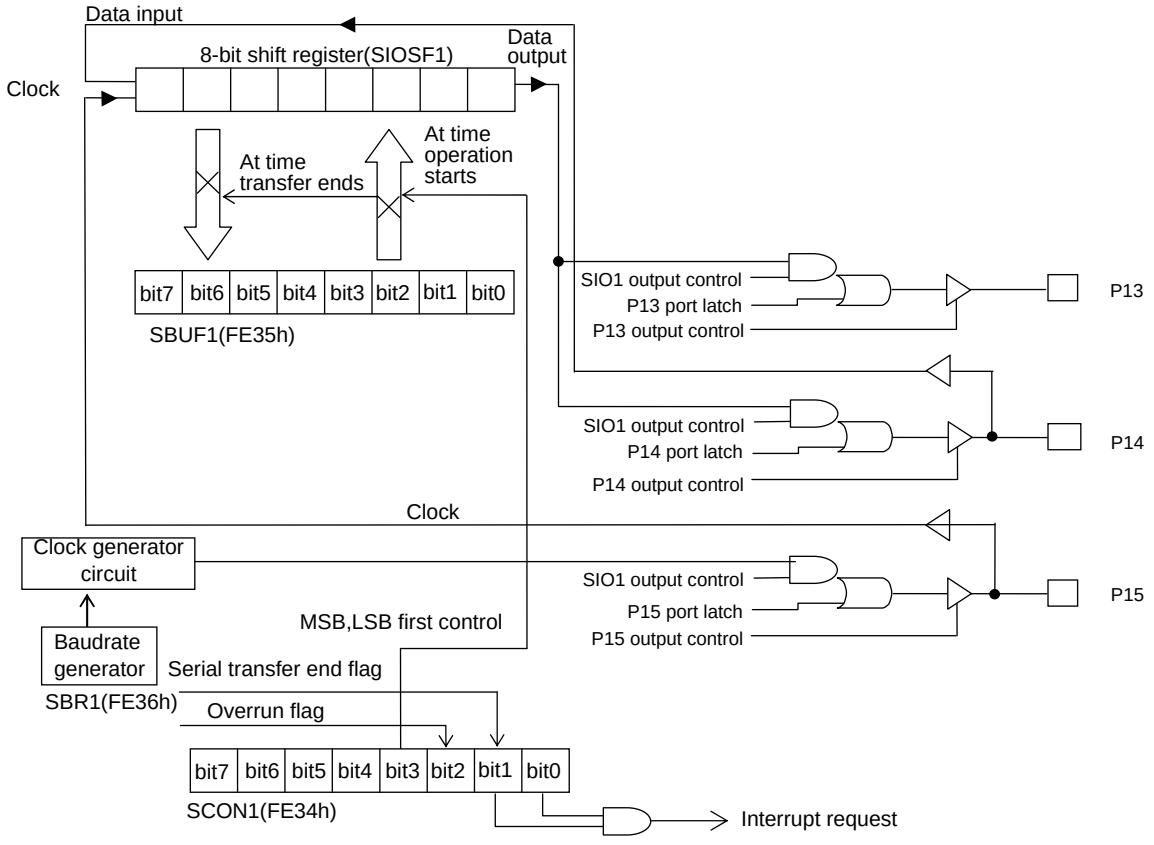


Figure 3.7.1 SIO1 Mode 0: Synchronous 8-bit Serial I/O Block Diagram (SI1M1=0, SI1M0=0)

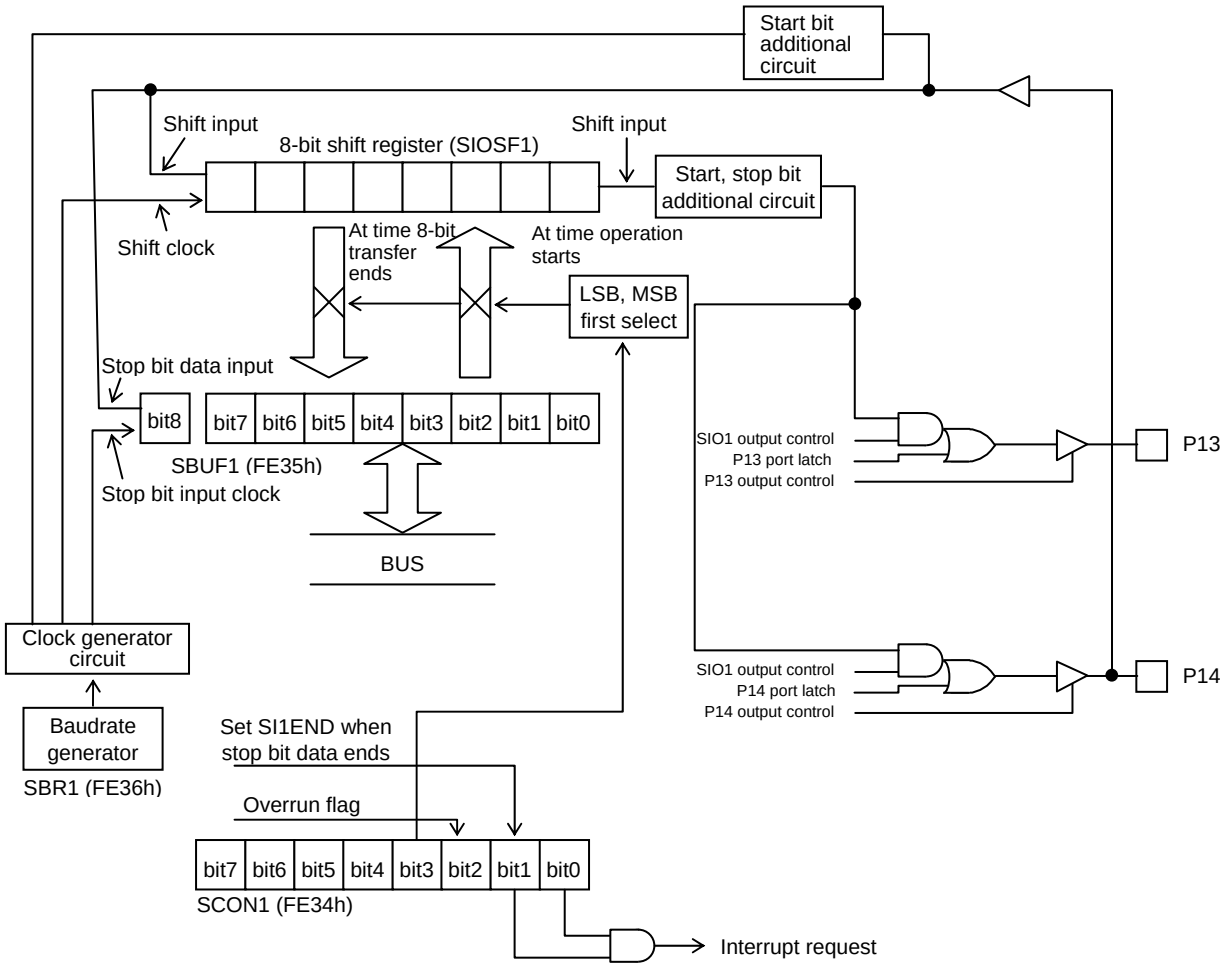


Figure 3.7.2 SIO1 Mode 1: Asynchronous Serial [UART] Block Diagram (SI1M1=0, SI1M0=1)

3.7.4 SIO1 Communication Examples

3.7.4.1 Synchronous serial communication (mode 0)

1) Setting the clock
   - Set up SBR1 when using an internal clock.
2) Setting the mode
   - Set as follows:

     SI1M0 = 0, SI1M1 = 0, SI1DIR, SI1IE = 1
3) Setting up the ports and SI1REC (bit 4)

	Clock Port P15
Internal clock	Output
External clock	Input

	Data Output Port P13	Data I/O Port P14	SI1REC
Data transmission only	Output	–	0
Data reception only	–	Input	1
Data transmission/reception (3-wire)	Output	Input	0
Data transmission/reception (2-wire)	–	N-channel open drain output	0

4) Setting up output data
   - Write output data into SBUF1 in the data transmission mode (SI1REC = 0).
5) Starting operation
   - Set SI1RUN.
6) Reading data (after an interrupt)
   - Read SBUF1. (SBUF1 has been loaded with serial data from the data I/O port even in the transmission mode)
   - Clear SI1END and exit interrupt processing.
   - Return to step 4) when repeating processing.

3.7.4.2 Asynchronous serial communication (mode 1)

1) Setting the baudrate
   - Set up SBR1.
2) Setting the mode
   - Set as follows:

     SI1M0 = 1, SI1M1 = 0, SI1DIR, SI1IE = 1
3) Setting up the ports.

	Data Output Port P13	Data I/O Port P14
Data transmission/reception (2-wire)	Output	Input
Data transmission/reception (1-wire)	–	N-channel open drain output

4) Starting transmission
   - Set SI1REC to 0 and write output data into SBUF1.
   - Set SI1RUN.

Note: Use the SIO1 data I/O port (P14) when using the SIO1 transmission only in mode 1.
In mode 1, transmission is automatically started when a falling edge of receive data is detected. While mode 1 is on, the falling edge of data is always sensed at the data I/O port (P14). Consequently, if the transmit port is assigned to the data output port (P13), it is likely that data transmissions are started unexpectedly according to the changes in the state of P14.

5) Starting receive operation
   - Set SI1REC to 1. (Once SI1REC is set to 1, do not attempt to write data to the SCON1 register until the SI1END flag is set.)
   - Detect the falling edge of receive data.

6) Reading data (after an interrupt)
   - Read SBUF1. (SBUF1 has been loaded with serial data from the data I/O port even in the transmission mode. When SBUF1 is read in, the data about the position of the stop bit is read into bit 1 of the PSW.)
   - Clear SI1END and exit interrupt processing.
   - Return to step 4) when repeating processing.

Note: Make sure that the following conditions are met when performing continuous reception processing with SIO1 in mode 1 (UART):
   - The number of stop bits is set to 2 or greater.
   - Clearing of SI1END during interrupt processing terminates before the next start bit arrives.

3.7.4.3 Bus-master mode (mode 2)

1) Setting the clock
   - Set up SBR1.

2) Setting the mode.
   - Set as follows:

     SI1M0 = 0, SI1M1 = 1, SI1DIR, SI1IE = 1, SI1REC = 0

3) Setting up the ports
   - Designate the clock and data ports as N-channel open drain output ports.

4) Starting communication (sending an address)
   - Load SBUF1 with address data.
   - Set SI1RUN (transfer a start bit + SBUF1 (8 bits) + stop bit (H)).

5) Checking address data (after an interrupt)
   - Read SBUF1. (SBUF1 has been loaded with serial data from the data I/O port even in the transmission mode. When SBUF1 is read in, the data about the position of the stop bit is read into bit 1 of the PSW.)
   - Check for an acknowledge by reading bit 1 of the PSW.

     If a condition for losing the bus contention occurs (see Note 1 in Table 3.7.1), no interrupt will be generated as SI1RUN is cleared in that case. If there is a possibility of a condition for losing the bus contention such as the presence of a separate master mode device, find out such condition by, for example, performing timeout processing using a timer module.

6) Sending data
   - Load SBUF1 with output data.
   - Clear SI1END and exit interrupt processing (transfer SBUF1 (8 bits) + stop bit (H)).

7) Checking sent data (after an interrupt)
   - Read SBUF1. (SBUF1 has been loaded with serial data from the data I/O port even in the transmission mode. When SBUF1 is read in, the data about the position of the stop bit is read into bit 1 of the PSW.)
   - Check for an acknowledge by reading bit 1 of the PSW.
   - If a condition for losing the bus contention occurs (see Note 1 in Table 3.7.1), no interrupt will be generated as SI1RUN is cleared in that case. If there is a possibility of a condition for losing the bus contention such as the presence of a separate master mode device, find out such condition by, for example, performing timeout processing using a timer module.
   - Return to step 6) when continuing data transmission.
   - Go to step 10) to terminate communication.

8) Receiving data
   - Set SI1REC to 1.
   - Clear SI1END and exit interrupt processing (receive (8 bits) + SBUF1 bit 8 (acknowledge) output).

9) Reading received data (after an interrupt)
   - Read SBUF1.
   - Return to step 8) when continuing data reception.
   - Go to * in step 10) to terminate communication. At this moment, SBUF1 bit 8 data has already been presented as acknowledge data and the clock for the master side has been released.

10) Terminating communication
   - Manipulate the clock output port (P15FCR = 0, P15DDR = 1, P15 = 0) and set the clock output to 0.
   - Manipulate the data output port (P14FCR = 0, P14DDR = 1, P14 = 0) and set the data output to 0.
   - Restore the clock output port into the original state (P15FCR = 1, P15DDR = 1, P15 = 0) and release the clock output.
   * • Wait for all slaves to release the clock and the clock to be set to 1.
   - Allow for a data setup time, then manipulate the data output port (P14FCR = 0, P14DDR = 1, P14 = 1) and set the data output to 1. In this case, the SIO1 overrun flag: SI1OVR (SCON1:FE34, bit 2) is set but this will exert no influence on the operation of SIO1.
   - Restore the data output port into the original state (set P14FCR to 1, then P14DDR to 1 and P14 to 0).
   - Clear SI1END and SI1OVR, then exit interrupt processing.
   - Return to step 4) to repeat processing.

3.7.4.4 Bus-slave mode (mode 3)

1) Setting the clock
   - Set up SBR1 (to set the acknowledge data setup time).

2) Setting the mode
   - Set as follows:

     SI1M0 = 1, SI1M1 = 1, SI1DIR, SI1IE = 1, SI1REC = 0

3) Setting up ports
   - Designate the clock and data ports as N-channel open drain output ports.

4) Starting communication (waiting for an address)

*1 • Set SI1REC.

*2 • SI1RUN is automatically set on detection of a start bit.
   - Perform receive processing (8 bits) and set the clock output to 0 on the falling edge of the 8th clock, which generates an interrupt.

5) Checking address data (after an interrupt)
   - Detecting a start condition sets SI1OVR. Check SI1RUN = 1 and SI1OVR = 1 to determine if the address has been received.

     (SI1OVR is not automatically cleared. Clear it by instruction.)
   - Read SBUF1 and check the address.
   - If no address match occurs, clear SI1RUN and SI1END and exit interrupt processing, then wait for a stop condition detection at * in step 8).

6) Receiving data

* • Clear SI1END and exit interrupt processing. (If a receive sequence has been performed, send an acknowledge and release the clock port after the lapse of (SBR1 value + 1) × Tcyc.)
   - When a stop condition is detected, SI1RUN is automatically cleared and an interrupt is generated. Then, clear SI1END to exit interrupt processing and return to *2 in step 4).
   - Perform a receive operation (8 bits), then set the clock output to 0 on the falling edge of the 8th clock, after which an interrupt occurs. The clock counter will be cleared if a start condition is detected in the middle of receive processing. In such a case, another 8 clocks are required to generate an interrupt.
   - Read SBUF1 and store the read data.

   Note: Bit 8 of SBUF1 is not yet updated because the rising edge of 9th clock has not yet occurred.
   - Return to * in step 6) to continue receive processing.

7) Sending data
   - Clear SI1REC.
   - Load SBUF1 with output data.
   - Clear SI1END and exit interrupt processing. (Send an acknowledge for the preceding reception operation and release the clock port after the lapse of (SBR1 value + 1) × Tcyc.)

*1 • Perform a send operation (8 bits) and set the clock output to 0 on the falling edge of the 8th clock, after which an interrupt occurs.

*2 • Go to *3 in step 7) if SI1RUN is set to 1.
   - If SI1RUN is set to 0, implying an interrupt from *4 in step 7), clear SI1END and SI1OVR and return to *1 in step 4).

*3 • Read SBUF1 and check send data as required.

Note: Bit 8 of SBUF1 is not yet updated because the rising edge of 9th clock has not yet occurred.

- Load SBUF1 with the next output data.
- Clear SI1END and exit interrupt processing. (Release the clock port after the lapse of (SBR1 value + 1) × Tcyc).
- Return to *1 in step7) if an acknowledge from the master is present (L).
- If there is no acknowledge presented from the master (H), SIO1, recognizing the end of data transmission, automatically clears SI1RUN and releases the data port.

  * However, in a case that restart condition comes just after the event, SI1REC must be set to "1" before exiting the interrupt (SI1REC is for detecting a start condition and is not set automatically). It may disturb the transmission of address from the master if there is an unexpected restart just after slave's transmission (when SI1REC is not set to 1 by instruction).

*4 • When a stop condition is detected, an interrupt is generated and processing returns to *2 in step 7).

8) Terminating communication

- Set SI1REC.
- Return to * in step 6) to cause communication to automatically terminate.
- To force communication to termination, clear SI1RUN and SI1END (release the clock port).

* • An interrupt occurs when a stop condition is detected. Then, clear SI1END and SI1OVR and return to *2 in step 4).

3.7.5 Related Registers

3.7.5.1 SIO1 control register (SCON1)

1) This register is an 8-bit register that controls the operation and interrupts of SIO1.

Address	Initial Value	R/W	Name	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE34	0000 0000	R/W	SCON1	-	SI1M1	SI1M0	SI1RUN	SI1REC	SI1DIR	SI1OVR	SI1END	SI1IE

SI1M1 (bit 7): SIO1 mode control

SI1M0 (bit 6): SIO1 mode control

Table 3.7.2 SIO1 Operating Modes

Mode	SI1M1	SI1M0	Operating Mode
0	0	0	Synchronous 8-bit SIO
1	0	1	UART (1 stop bit, no parity)
2	1	0	Bus master mode
3	1	1	Bus slave mode

SI1RUN (bit 5): SIO1 operation flag

1) A 1 in this bit indicates that SIO1 is running.
2) See Table 3.7.1 for the conditions for setting and clearing this bit.

SI1REC (bit 4): SIO1 receive/send control

1) Setting this bit to 1 places SIO1 into the receive mode.
2) Setting this bit to 0 places SIO1 into the send mode.

SI1DIR (bit 3): MSB/LSB first select

1) Setting this bit to 1 places SIO1 into the MSB first mode.
2) Setting this bit to 0 places SIO1 into the LSB first mode.

SI1OVR (bit 2): SIO1 overrun flag

1) In modes 0, 1, and 3, this bit is set when a falling edge of the input clock is detected when SI1RUN=0.
2) This bit is set if the conditions for setting SI1END are established when SI1END=1.
3) In mode 3 this bit is set when the start condition is detected.
4) This bit must be cleared with an instruction.

SI1END (bit 1): Serial transfer end flag

1) This bit is set when serial transfer terminates (see Table 3.7.1).
2) This bit must be cleared with an instruction.

SI1IE (bit 0): SIO1 interrupt request enable control

When this bit and SI1END are set to 1, an interrupt request to vector address 003BH is generated.

3.7.5.2 Serial buffer 1 (SBUF1)

1) Serial buffer 1 is a 9-bit register used to store data to be handled during SIO1 serial transfer.
2) The lower-order 8 bits of SBUF1 are transferred to the data shift register for data transmission/ reception at the beginning of transfer processing and the contents of the shift register are placed in the lower-order 8 bits of SBUF1 when 8-bit data is transferred.
3) In modes 1, 2, and 3, bit 8 of SBUF1 is loaded with the 9th data bit that is received (data about the position of the stop bit).

Address	Initial Value	R/W	Name	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE35	00000 0000	R/W	SBUF1	SBUF18	SBUF17	SBUF16	SBUF15	SBUF14	SBUF13	SBUF12	SBUF11	SBUF10

3.7.5.3 Baudrate generator register (SBR1)

1) This register is an 8-bit register that defines the transfer rate of SIO1.
2) Loading this register with data causes the baudrate generating counter to be initialized immediately.
3) The transfer rate depends on the transfer mode (the baudrate generator is disabled in mode 3).

Modes 0 and 2: TSBR1 = (SBR1 value + 1) × 2 Tcyc
(Value range = 2 to 512 Tcyc)

Mode 1: TSBR1 = (SBR1 value + 1) × 8Tcyc
(Value range = 8 to 2048Tcyc)

Address	Initial Value	R/W	Name	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE36	0000 0000	R/W	SBR1	-	SBRG17	SBRG16	SBRG15	SBRG14	SBRG13	SBRG12	SBRG11	SBRG10

3.8 AD Converter (ADC12)

3.8.1 Overview

This series of microcontrollers incorporates a 12-bit resolution AD converter that has the features listed below. It allows the microcontroller to take in analog signals easily.

1) 12-bit resolution
2) Successive approximation
3) AD conversion mode select (resolution switching)
4) 8-channel analog input
5) Conversion time select

3.8.2 Functions

1) Successive approximation
   - The ADC has a resolution of 12 bits.
   - It requires some conversion time after starting conversion processing.
   - The conversion results are placed in the AD conversion result registers (ADRLC, ADRHC).
2) AD conversion mode select (resolution switching)

   The AD converter supports two AD conversion modes: 12- and 8-bit conversion modes so that the appropriate conversion resolution can be selected according to the operating conditions of the application. Conversion mode switching is accomplished through the AD mode register (ADMRC).
3) 8-channel analog input

   The signal to be converted is selected using the AD control register (ADCRC) from 8 types of analog signals that are supplied from P00 to P06 and P70 pins.
4) Conversion time select

   The AD conversion time can be set to 1/1 to 1/128 (frequency division ratio). The AD mode register (ADMRC) and AD conversion result low byte register (ADRLC) are used to select the conversion time for appropriate AD conversion.
5) It is necessary to manipulate the following special function registers to control the AD converter.
   - ADCRC, ADMRC, ADRLC, ADRHC

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE58	0000 0000	R/W	ADCRC	AD CHSEL3	AD CHSEL2	AD CHSEL1	AD CHSEL0	ADCR3	AD START	AD ENDF	ADIE
FE59	0000 0000	R/W	ADMRC	ADMD4	ADMD3	ADMD2	ADMD1	ADMD0	ADMR2	ADTM1	ADTM0
FE5A	0000 0000	R/W	ADRLC	DATAL3	DATAL2	DATAL1	DATAL0	ADRL3	ADRL2	ADRL1	ADTM2
FE5B	0000 0000	R/W	ADRHC	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

3.8.3 Circuit Configuration

3.8.3.1 AD conversion control circuit

1) The AD conversion control circuit runs in two modes: 12- and 8-bit AD conversion modes.

3.8.3.2 Comparator circuit

1) The comparator circuit consists of a comparator that compares the analog input with the reference voltage and a circuit that controls the reference voltage generator circuit and the conversion results. AD conversion end flag (ADENDF) of the AD control register (ADCRC) is set when an analog input channel is selected and the AD conversion terminates in the conversion time designated by the conversion time control register. The conversion results are placed in the AD conversion result registers (ADRHC, ADRLC).

3.8.3.3 Multiplexer 1 (MPX1)

1) Multiplexer 1 is used to select the analog signal to be subject to AD conversion from 8 channels of analog signals.

3.8.3.4 Automatic reference voltage generator circuit

1) The reference voltage generator circuit consists of a network of ladder resistors and a multiplexer (MPX2) and generates the reference voltage that is supplied to the comparator circuit. Generation of the reference voltage is automatically started when an AD conversion starts and stopped when the conversion ends. The reference voltage output ranges from VDD to VSS.

3.8.4 Related Registers

3.8.4.1 AD control register (ADCRC)

1) This register is an 8-bit register that controls the operation of the AD converter.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE58	0000 0000	R/W	ADCRC	AD CHSEL3	AD CHSEL2	AD CHSEL1	AD CHSEL0	ADCR3	AD START	AD ENDF	ADIE

ADCHSEL3 (bit 7):
ADCHSEL2 (bit 6):
ADCHSEL1 (bit 5):
ADCHSEL0 (bit 4):
} **AD conversion input signal select**

These 4 bits are used to select the signal to be subject to AD conversion.

AD CHSEL3	AD CHSEL2	AD CHSEL1	AD CHSEL0	Signal Input Pin
0	0	0	0	P00/AN0
0	0	0	1	P01/AN1
0	0	1	0	P02/AN2
0	0	1	1	P03/AN3
0	1	0	0	P04/AN4
0	1	0	1	P05/AN5
0	1	1	0	P06/AN6
0	1	1	1	–
1	0	0	0	P70/AN8

ADCRC3 (bit 3): Fixed bit

This bit must always be set to 0.

ADSTART (bit 2): AD converter operation control

This bit starts (1) or stops (0) AD conversion processing. Setting this bit to 1 starts AD conversion. The bit is reset automatically when the AD conversion ends. The time specified by the conversion time control register is required to complete the conversion. The conversion time is defined using three bits, i.e., the ADTM2 (bit 0) of the AD conversion result register low byte (ADRLC) and the ADTM1 and ADTM0 of the AD mode register (ADMRC).

Setting this bit to 0 stops the AD conversion. No correct conversion results can be obtained if this bit is cleared when AD conversion is in progress.

Never clear this bit or place the microcontroller in HALT or HOLD mode while the AD conversion processing is in progress.

ADENDF (bit 1): AD conversion end flag

This bit identifies the end of AD conversion. It is set (1) when AD conversion is finished. Then, an interrupt request to vector address 0043H is generated if ADIE is set to 1.

If ADENDF is set to 0, it indicates that no AD conversion operation is in progress.

This flag must be cleared with an instruction.

ADIE (bit 0): AD conversion interrupt request enable control

An interrupt request to vector address 0043H is generated when this bit and ADENDF are set to 1.

Notes:

- *It is inhibited to set ADCHSEL3 to ADCHSEL0 to any value from '1001' to '1111' and '0111.'*
- *Do not place the microcontroller in HOLD mode with ADSTART set to 1. Make sure that ADSTART is set to 0 before putting the microcontroller in HOLD mode.*
- *Never execute any instructions other than the read, branch, and compare on the ADCRC register (FE58h) while conversion processing is in progress. However, this does not hold true when conversion processing is to be stopped.*

3.8.4.2 AD mode register (ADMRC)

1) This register is an 8-bit register that controls AD converter operation mode.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE59	0000 0000	R/W	ADMRC	ADMD4	ADMD3	ADMD2	ADMD1	ADMD0	ADMR2	ADTM1	ADTM0

ADMD4 (bit 7): Fixed bit

This bit must always be set to 0.

ADMD3 (bit 6): AD conversion mode control (resolution select)

This bit selects the AD converter resolution between 12-bit AD conversion mode (0) and 8-bit AD conversion mode (1).

If this bit is set to 1, the AD converter serves as an 8-bit AD converter. The conversion results are placed only in the AD conversion result register high byte (ADRHC); the contents of the AD conversion result register low byte (ADRLC) remain unchanged.

If this bit is set to 0, the AD converter serves as a 12-bit AD converter. The conversion results are placed in the AD conversion result register high byte (ADRHC) and the higher-order 4 bits of the AD conversion result register low byte (ADRLC).

ADMD2 (bit 5): Fixed bit

This bit must always be set to 0.

ADMD1 (bit 4): Fixed bit

This bit must always be set to 0.

ADMD0 (bit 3): Fixed bit

This bit must always be set to 0.

ADMR2 (bit 2): Fixed bit

This bit must always be set to 0.

ADTM1 (bit 1):
ADTM0 (bit 0): } **AD conversion time control**

These bits and ADTM2 (bit 0) of the AD conversion result register low byte (ADRLC) define the conversion time.

ADRLC Register	ADMRC Register		AD Frequency Division Ratio
ADTM2	ADTM1	ADTM0	
0	0	0	1/1
0	0	1	1/2
0	1	0	1/4
0	1	1	1/8
1	0	0	1/16
1	0	1	1/32
1	1	0	1/64
1	1	1	1/128

Conversion time calculation formulas

- 12-bit AD conversion mode: Conversion time = ((52/(AD division ratio)) + 2) × 1/3 × Tcyc
- 8-bit AD conversion mode: Conversion time = ((32/(AD division ratio)) + 2) × 1/3 × Tcyc

Notes:

- *The conversion time is doubled in the following cases:*
  1) *The AD conversion is carried out in the 12-bit AD conversion mode for the first time after a system reset.*
  2) *The AD conversion is carried out for the first time after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode.*
- *The conversion time determined by the above formula is taken in the second and subsequent conversions or in the AD conversions that are carried out in the 8-bit AD conversion mode.*

3.8.4.3 AD conversion result register low byte (ADRLC)

1) This register is used to hold the lower-order 4 bits of the results of an AD conversion carried out in the 12-bit AD conversion mode and to control the conversion time.
2) Since the data in this register is not established during an AD conversion, the conversion results must be read out only after the AD conversion is completed.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE5A	0000 0000	R/W	ADRLC	DATAL3	DATAL2	DATAL1	DATAL0	ADRL3	ADRL2	ADRL1	ADTM2

DATAL3 (bit 7):
DATAL2 (bit 6):
DATAL1 (bit 5):
DATAL0 (bit 4):
AD conversion result lower-order 4 bits

ADRL3 (bit 3): Fixed bit

This bit must always be set to 0.

ADRL2 (bit 2): Fixed bit

This bit must always be set to 0.

ADRL1 (bit 1): Fixed bit

This bit must always be set to 0.

ADTM2 (bit 0): AD conversion time control

This bit and AD mode register (ADMRC) bits ADTM1 (bit 1) and ADTM0 (bit 0) are used to control the conversion time. See the subsection on the AD mode register for the procedure to set the conversion time.

Note:

- *The conversion result data contains some errors (quantization error + combination error). Be sure to use only valid conversion results while referring to the latest "SANYO Semiconductor Data Sheet."*

3.8.4.4 AD conversion result register high byte (ADRHC)

1) This register is used to hold the higher-order 8 bits of the results of an AD conversion that is carried out in the 12-bit AD conversion mode. The register stores the whole 8 bits of an AD conversion that is carried out in the 8-bit AD conversion mode.

2) Since the data in this register is not established during an AD conversion, the conversion results must be read out only after the AD conversion is completed.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE5B	0000 0000	R/W	ADRHC	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

3.8.5 AD Conversion Example

3.8.5.1 12-bit AD conversion mode

1) Setting up the 12-bit AD conversion mode
   - Set the ADMD3 bit (bit 6) of the AD mode register (ADMRC) to 0.
2) Setting up the conversion time
   - To set the conversion time to 1/32 frequency division, set ADTM2 (bit 0) of the AD conversion result register low byte (ADRLC) to 1, ADTM1 (bit 1) of the AD mode register (ADMRC) to 0, and ADTM0 (bit 0) of the AD mode register (ADMRC) to 1.
3) Setting up the input channel
   - When using AD channel input AN5, set AD control register ADCRC: ADCHSEL3 (bit 7) to 0, ADCHSEL2 (bit 6) to 1, ADCHSEL1 (bit 5) to 0, and ADCHSEL0 (bit 4) to 1.
4) Starting AD conversion
   - Set ADSTART (bit 2) of the AD control register (ADCRC) to 1.
   - The conversion time is doubled after a system reset and when the AD conversion is carried out for the first time after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode. The conversion time determined by the formula is taken in the second and subsequent conversions.
5) Testing AD conversion end flag
   - Monitor ADENDF (bit 1) of the AD control register (ADCRC) until it is set to 1.
   - Clear AD conversion end flag (ADENDF) to 0 after confirming that the ADENDF flag (bit 1) is set to 1.
6) Reading in the AD conversion results
   - Read the AD conversion result high byte register (ADRHC) and AD conversion result register low byte (ADRLC). Since the conversion result data contains some errors (quantization error + combination error), use only the valid part of the conversion data selected according to the specifications given in the latest “SANYO Semiconductor Data Sheet.”
   - Pass the above read data to the application software processing.
   - Return to step 4) to repeat the conversion processing.

3.8.6 Hints on the Use of the ADC

1) The conversion time that the user can select varies depending on the frequency of the cycle clock. When preparing a program, refer to the latest “SANYO Semiconductors Data Sheet” to select an appropriate conversion time.

2) Setting ADSTART to 0 while conversion is in progress will stop the conversion function.

3) Do not place the microcontroller in HOLD mode while AD conversion is in progress. Make sure that ADSTART is set to 0 before putting the microcontroller in HOLD mode.

4) ADSTART is automatically reset and the AD converter stops operation if a reset is triggered while AD conversion processing is in progress.

5) When conversion is finished, AD conversion end flag (ADENDF) is set and, at the same time, the AD conversion operation control bit (ADSTART) is reset. The end of conversion condition can be identified by monitoring ADENDF. Setting ADIE generates an interrupt request to vector address 0043H at the end of conversion.

6) Never execute any instructions other than the read, branch, and compare on the ADCRC register (FE58h) while conversion processing is in progress. However, this does not hold true when conversion processing is to be stopped.

7) The conversion time is doubled in the following cases:
   - The AD conversion is carried out in the 12-bit AD conversion mode for the first time after a system reset.
   - The AD conversion is carried out for the first time after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode.
   - The conversion time determined using the "conversion time calculation formula" is adopted in the second and subsequent conversions or in the AD conversions that are carried out in the 8-bit AD conversion mode.

8) The conversion result data contains some errors (quantization error + combination error). Be sure to use only valid conversion results while referring to the latest “SANYO Semiconductor Data Sheet.”

9) Make sure that only input voltages that fall within the specified range are supplied to pins P00/AN0 to P06/AN6 and P70/AN8. Application of a voltage higher than VDD or lower than VSS to an input pin may exert adverse influences on the converted value of the channel in question or other channels.

10) Take the following preventive actions as countermeasures to keep the reduction in conversion accuracy due to noise interferences as low as possible:
   - Be sure to add external bypass capacitors several μF and several thousand pF near the VDD1 and VSS1 pins (as close as possible, desirably 5 mm or less).
   - Add external low-pass filters (RC) or capacitors, most suitable for noise reduction, immediately close to the analog input pins. To avert the adverse coupling influences, use a ground that is free of noise interferences as the ground for the capacitors (rough standard values are: R = less than 5 kΩ, C=1000 pF to 0.1μF).
   - Do not lay analog signal lines close to, in parallel with, or in a crossed arrangement with digital pulse signal lines or signal lines in which large current changes can occur. Shield both ends of analog signal lines with noise-free ground shields.
   - Make sure that no digital pulses are applied to or generated out of pins adjacent to the analog input pin that is being subject to conversion.

- Correct conversion results may not be obtained because of noise interferences if the state of port outputs is changing. To minimize the adverse influences of noise interferences, it is necessary to keep the line resistance across the power supply and the VDD pins of the microcontroller at minimum. This should be kept in mind when designing an application circuit.
- Adjust the amplitudes of the voltage at the oscillator pin and the I/O voltages at the other pins so that they fall within the voltage range between VDD and VSS.

11) To obtain valid conversion data, perform conversion operations on the input several times, discard the maximum and minimum values of the conversion results, and take an average of the remaining data.

4. Control Functions

4.1 Interrupt Function

4.1.1 Overview

This series of microcontrollers has the capability to control three levels of multiple interrupts, i.e., low level (L), high level (H), and highest level (X). The master interrupt enable register (IE) and interrupt priority control register (IP) are used to enable or disable interrupts and to determine the priority of interrupts.

4.1.2 Functions

1) Interrupt processing
   - Peripheral modules generate an interrupt request to the predetermined vector address when the interrupt request and interrupt request enable flags are set to 1.
   - When the microcontroller receives an interrupt request from a peripheral module, it determines the interrupt level, priority and interrupt enable status. If the interrupt request is legitimate for processing, the microcontroller saves the value of PC in the stack and causes a branch to the predetermined vector address.
   - The return from the interrupt routine is accomplished by the RETI instruction, which restores the old state of the PC and interrupt level.
2) Multilevel interrupt control
   - The interrupt function supports three levels of interrupts, that is, the low level (L), high level (H), and highest level (X). The interrupt function will not accept any interrupt requests of the same level or lower level than that of the interrupt that is currently being processed.
3) Interrupt priority
   - When interrupt requests to two or more vector addresses occur at the same time, the interrupt request of the highest level takes precedence over the other interrupt requests. When interrupts of the same level occur at the same time, an interrupt with a smaller vector address is given priority.
4) Interrupt request enable control
   - The master interrupt enable register (IE) can be used to control the enabling/disabling of H- and L-level interrupt requests.
   - Interrupt requests of the X level cannot be disabled.
5) Interrupt disable period
   - Interrupts are held disabled for a period of 2Tcyc after a write is made to the IE (FE08H) or IP (FE09H) register, or HOLD mode is released.
   - No interrupt can occur during the interval between the execution of an instruction that loads the PCON (FE07H) register and the execution of the next instruction.
   - No interrupt can occur during the interval between the execution of a RETI instruction and the execution of the next instruction.

6) Interrupt level control
   - Interrupt levels can be selected on a vector address basis.

Table of Interrupts

No.	Vector Address	Selectable Level	Interrupt Sources
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3
5	00023H	H or L	T0H
6	0002BH	H or L	None
7	00033H	H or L	None
8	0003BH	H or L	SIO1
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0

- Priority levels: X > H > L
- When interrupts of the same level occur at the same time, the interrupt with the smallest vector address is given priority.

7) It is necessary to manipulate the following special function registers to enable interrupts and to specify their priority.
   - IE, IP

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE08	0000 HH00	R/W	IE	IE7	XFLG	HFLG	LFLG	-	-	XCNT1	XCNT0
FE09	0000 0000	R/W	IP	IP4B	IP43	IP3B	IP33	IP2B	IP23	IP1B	IP13

4.1.3 Circuit Configuration

4.1.3.1 Master interrupt enable control register (IE) (6-bit register)

1) This register enables and disables H- and L-level interrupts.
2) The interrupt level flag of the register can be read.
3) The register selects the level (L or X) of interrupts to vector addresses 00003H and 0000BH.

4.1.3.2 Interrupt priority control register (IP) (8-bit register)

1) This register selects the level (H or L) of interrupts to vector addresses 00013H to 0004BH.

4.1.4 Related Registers

4.1.4.1 Master interrupt enable control register (IE)

1) This register is a 6-bit register for controlling the interrupts. Bits 6 to 4 are read only.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE08	0000 HH00	R/W	IE	IE7	XFLG	HFLG	LFLG	-	-	XCNT1	XCNT0

IE7 (bit 7): H-/L-level interrupt enable/disable control

- A 1 in this bit enables H- and L-level interrupt requests to be accepted.
- A 0 in this bit disables H- and L-level interrupt request to be accepted.
- X-level interrupt requests are always enabled regardless of the state of this bit.

XFLG (bit 6): X-level interrupt flag (R/O)

- This bit is set when an X-level interrupt is accepted and reset when execution returns from the processing of the X-level interrupt.
- This bit is read only. No instruction can rewrite the value of this bit directly.

HFLG (bit 5): H-level interrupt flag (R/O)

- This bit is set when an H-level interrupt is accepted and reset when execution returns from the processing of the H-level interrupt.
- This bit is read only. No instruction can rewrite the value of this bit directly.

LFLG (bit 4): L-level interrupt flag (R/O)

- This bit is set when an L-level interrupt is accepted and reset when execution returns from the processing of the L-level interrupt.
- This bit is read only. No instruction can rewrite the value of this bit directly.

(Bits 3, 2): These bits do not exist. They are always read as 1.

XCNT1 (bit 1): 0000BH interrupt level control flag

- A 1 in this bit sets all interrupts to vector address 0000BH to the L-level.
- A 0 in this bit sets all interrupts to vector address 0000BH to the X-level.

XCNT0 (bit 0): 00003H interrupt level control flag

- A 1 in this bit sets all interrupts to vector address 00003H to the L-level.
- A 0 in this bit sets all interrupts to vector address 00003H to the X-level.

4.1.4.2 Interrupt priority control register (IP)

1) This register is an 8-bit register that selects the interrupt level (H/L) of interrupts to vector addresses 00013H to 0004BH.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE09	0000 0000	R/W	IP	IP4B	IP43	IP3B	IP33	IP2B	IIP23	IP1B	IP13

	Interrupt Vector Address	IP Bit	Value	Interrupt Level
7	0004BH	IP4B	0	L
			1	H
6	00043H	IP43	0	L
			1	H
5	0003BH	IP3B	0	L
			1	H
4	00033H	IP33	0	L
			1	H
3	0002BH	IP2B	0	L
			1	H
2	00023H	IP23	0	L
			1	H
1	0001BH	IP1B	0	L
			1	H
0	00013H	IP13	0	L
			1	H

4.2 System Clock Generator Function

4.2.1 Overview

This series of microcontrollers incorporates three systems of oscillator circuits, i.e., the main clock oscillator, medium-speed RC oscillator, and variable modulation frequency (VMRC) RC oscillator as system clock generator circuits. The medium-speed RC and variable modulation frequency RC oscillator circuits have internal resistors and capacitors, so that no external circuit is required.

The system clock can be selected from these three types of clock sources under program control.

4.2.2 Functions

1) System clock select
   - Allows the system clock to be selected under program control from three types of clocks generated by the main clock oscillator, medium-speed RC oscillator, and variable modulation frequency RC oscillator.

2) System clock frequency division
   - Divides frequency of the oscillator clock selected as the system clock and supplies the resultant clock as the system clock.
   - The frequency divider circuit is made up of two stages:

     The first stage allows the selection of division ratios of $\frac{1}{1}$ and $\frac{1}{2}$.

     The second stage allows the selection of division ratios of $\frac{1}{1}$, $\frac{1}{2}$, $\frac{1}{4}$, $\frac{1}{8}$, $\frac{1}{16}$, $\frac{1}{32}$, $\frac{1}{64}$, and $\frac{1}{128}$.

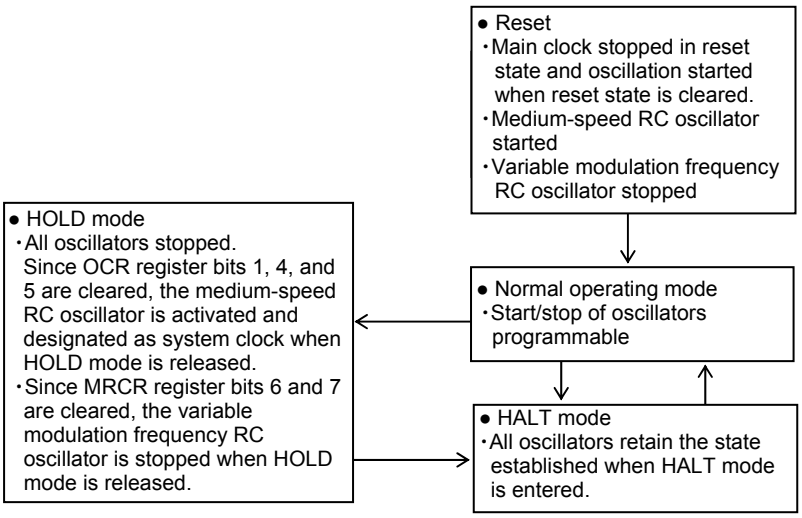
3) Oscillator circuit control
   - Allows the start/stop control of the three systems of oscillators to be executed independently through microcontroller instructions.
   - The CF oscillator circuit may be either a low power dissipation type CF oscillation low amplifier or a CF oscillation normal amplifier.

4) Multiplexed input pin function
   - The CF oscillation pins (CF1and CF2) can also be used as general-purpose input ports.

5) Oscillator circuit states and operating modes

Mode/Clock	Main Clock	Medium-speed RC Oscillator	VMRC Oscillator	System Clock
Reset	Stopped	Running	Stopped	Medium-speed RC oscillator
Reset released	Running	Running	Stopped	Medium-speed RC oscillator
Normal mode	Programmable	Programmable	Programmable	Programmable
HALT	State established at entry time	State established at entry time	State established at entry time	State established at entry time
HOLD	Stopped	Stopped	Stopped	Stopped
Immediately after exit from HOLD mode	State established at entry time	Running	Stopped	Medium-speed RC oscillator

Note: See Section 4.3," Standby Function," for the procedures to enter and exit the microcontroller operating modes



6) It is necessary to manipulate the following special function registers to control the system clock.
   - PCON, OCR, CLKDIV, MRCR, XT2PC, SLWRC

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE07	HHHH HH00	R/W	PCON	-	-	-	-	-	-	PDN	IDLE
FE0C	HHHH H000	R/W	CLKDIV	-	-	-	-	-	CLKDV2	CLKDV1	CLKDV0
FE0D	00HX XXXX	R/W	MRCR	MRCSEL	MRCST	-	RCCTD4	RCCTD3	RCCTD2	RCCTD1	RCCTD0
FE0E	0H00 XX00	R/W	OCR	CLKSGL	-	CLKCB5	CLKCB4	XT2IN	XT1IN	RCSTOP	CFSTOP
FE43	HHHH 0HHH	R/W	XT2PC	-	-	-	-	XTCFIN	-	-	-
FE7C	HHHH H0HH	R/W	SLWRC	-	-	-	-	-	CFLAMP	-	-

4.2.3 Circuit Configuration

4.2.3.1 Main clock oscillator circuit

1) This circuit is activated for oscillation by connecting a ceramic resonator and a capacitor to the CF1and CF2 pins and controlling the OCR and XT2PC registers.
2) The data at the CF1and CF2 pins can be read as bits 2 and 3 of the OCR register.
3) If they are not used for the main clock or as general-purpose input ports, the general-purpose input configuration must be selected and the CF1 and CF2 pins must be pulled down to the VSS1 level with a 100 kΩ.

4.2.3.2 Internal medium-speed RC oscillator circuit (conventional RC oscillator circuit)

1) This oscillator oscillates according to the internal resistor and capacitor (at 1 MHz standard).
2) The clock from the medium-speed RC oscillator is selected as the system clock after the reset state or after HOLD mode is released.
3) Unlike main clock oscillator, the medium-speed RC oscillator starts oscillation at a normal frequency immediately after starting oscillation.

4.2.3.3 Variable modulation frequency RC oscillator circuit

1) This circuit oscillates according to the internal resistor and capacitor.
2) The circuit counts the clocks with a source oscillation frequency of 16 MHz with a 5-bit counter. The maximum allowable clock rate is 8 MHz.
3) The circuit toggles the clock output each time the counter value matches the preset count value.
4) The variable modulation frequency RC oscillator circuit is suited to generate a main clock which does not require the precision in frequency that the external CF oscillator would provide.

4.2.3.4 Power control register (PCON) (2-bit register)

1) This register specifies the operating mode (normal/HALT/HOLD).

4.2.3.5 Oscillation control register (OCR) (7-bit register)

1) This register controls the start/stop operation of the oscillator circuits.
2) This register selects the system clock.
3) This register sets the division ratio of the oscillation clock to be used as the system clock to $\frac{1}{1}$ or $\frac{1}{2}$.
4) The state of the CF1 and CF2 pins can be read as bits 2 and 3 of this register.

4.2.3.6 Low-speed RC oscillation control register (SLWRC) (1 bit)

1) This register selects the amplifier size of the CF oscillator circuit. The CF oscillator low amplification is effective for reducing power dissipation under such conditions as low voltage, CF= 4 MHz, system frequency division ratio = 1/4 to 1/16.

4.2.3.7 CF1 and CF2 general-purpose port input control register (XT2PC) (1-bit register)

1) This register controls the general-purpose input at the CF1 and CF2 pins.

4.2.3.8 Variable modulation frequency RC oscillation control register (MRCR) (7-bit register)

1) This register controls the start/stop operation of the variable modulation frequency RC oscillator circuit.
2) The register selects either CF or variable modulation frequency RC oscillator as the main clock source.
3) The register also defines the frequency of the variable modulation frequency RC oscillator clock.

4.2.3.9 System clock division control register (CLKDIV) (3-bit register)

1) This register controls the operation of the system clock divider circuit. The division ratios of $\frac{1}{1}$, $\frac{1}{2}$, $\frac{1}{4}$, $\frac{1}{8}$, $\frac{1}{16}$, $\frac{1}{32}$, $\frac{1}{64}$, and $\frac{1}{128}$ are supported.

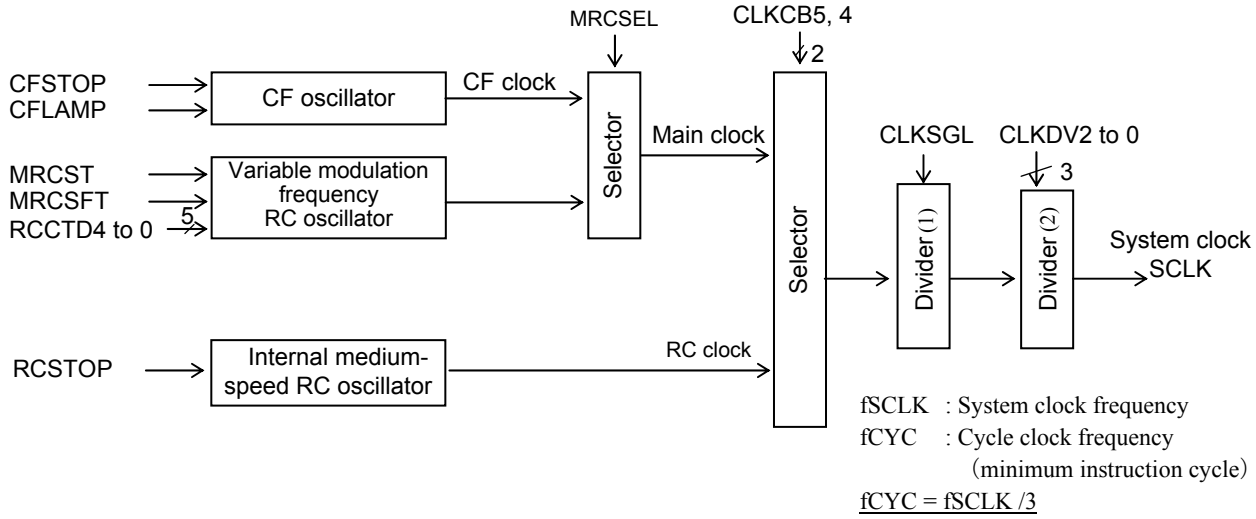


Fig. 4.2.1 System Clock Generator Block Diagram

4.2.4 Related Registers

4.2.4.1 Power control register (PCON) (2-bit register)

1) This register is a 2-bit register used to specify the operating mode (normal/HALT/HOLD).
   - See Section 4.3, Standby Function, for the procedures to enter and exit the microcontroller operating modes.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE07	HHHH HH00	R/W	PCON	-	-	-	-	-	-	PDN	IDLE

(Bits 7 to 2): These bits do not exist. They are always read as 1.

PDN (bit 1): HOLD mode setting flag

1) This bit must be set with an instruction.
   - When the microcontroller enters HOLD mode, all oscillations (main clock, medium-speed RC, and variable modulation frequency RC) are suspended and the OCR register, bits 1, 4, and 5 and the MRCR register, bits 7 and 6 are cleared.
   - When the microcontroller exits HOLD mode, the medium-speed RC oscillator starts oscillation and is used a system clock source.
2) PDN is cleared when a HOLD mode releasing signal (INT0, INT1, INT2, INT4, or P0INT) is generated or a reset occurs.
3) Bit 0 is automatically set when PDN is set.

IDLE (bit 0): HALT mode setting flag

1) Setting this bit places the microcontroller into HALT mode.
2) This bit is automatically set when bit 1 is set.
3) This bit is cleared on acceptance of an interrupt request or on receipt of a reset signal.

PDN	IDLE	Operating mode
0	0	Normal mode
0	1	HALT mode
1	1	HOLD mode

4.2.4.2 Oscillation control register (OCR) (7-bit register)

1) This register is a 7-bit register that controls the operation of the oscillator circuits, selects the system clock, and reads data from the CF1 and CF2 pins. Bits 3 and 2 are read-only.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE0E	0H00 XX00	R/W	OCR	CLKSGL	-	CLKCB5	CLKCB4	XT2IN	XT1IN	RCSTOP	CFSTOP

CLKSGL (bit 7): Clock division ratio select

1) When this bit is set to 1, the clock selected by bits 4 and 5 is used as the system clock as is.
2) When this bit is set to 0, the clock having a clock rate of $\frac{1}{2}$ of the clock selected by bits 4 and 5 is used as the system clock.

(Bit 6): This bit does not exist. It is always read as 1.

CLKCB5 (bit 5): System clock select

CLKCB4 (bit 4): System clock select

1) CLKCB5 and CLKCB4 are used to select the system clock.
2) CLKCB5 and CLKCB4 are cleared at reset time or when HOLD mode is entered.

CLKCB5	CLKCB4	System clock
0	0	Medium-speed RC oscillator
0	1	Main clock
1	0	Inhibited
1	1	Main clock

XT2IN (bit 3): CF2 pin data (read-only)

XT1IN (bit 2): CF1 pin data (read-only)

RCSTOP (bit 1)): Internal medium-speed RC oscillator circuit control

1) Setting this bit to 1 stops the internal medium-speed RC oscillator circuit.
2) Setting this bit to 0 starts the internal medium-speed RC oscillator circuit.
3) When a reset occurs, this bit is cleared and the internal RC oscillator circuit is enabled for oscillation.

CFSTOP (bit 0): Main clock oscillator circuit control

1) Setting this bit to 1 stops the oscillation of the main clock oscillator circuit.
2) Setting this bit to 0 starts the oscillation of the main clock oscillator circuit.
3) This bit is cleared on a reset.

OCR Register	XT2PC Register	CF1, CF2 State	OCR Register (FE0EH)	
CFSTOP	XTCFIN		XT2IN	XT1IN
0	0	Main clock oscillator active	CF2 pin data	CF1 pin data
1	0	Main clock oscillator stopped	Undefined	Undefined
0	1	Inhibited	CF2 pin data	CF1 pin data
1	1	General-purpose input	CF2 pin data	CF1 pin data

Note: To use the CF1 and CF2 pins as general-purpose input port pins, set XTCFIN (XT2PC register (FE43H), bit 3) to 1, and CFSTOP (OCR register (FE0EH), bit 0) to 1.

4.2.4.3 Low-speed RC oscillator control register (SLWRC) (1-bit register)

1) This register is a 1-bit register that controls the amplifier size of the CF oscillator circuit.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE7C	HHHH H0HH	R/W	SLWRC	-	-	-	-	-	CFLAMP	-	-

(Bits 7 to 3, 1, and 0): These bits do not exist. They are always read as 1.

CFLAMP (bit 2): CF oscillator amplifier size select control

1) A 1 in this bit selects the low amplifier size for the CF oscillator circuit.
2) A 0 in this bit selects the normal amplifier size for the CF oscillator circuit.

* See Subsection 4.2.5 as a predefined procedure is required to switch the selection.

4.2.4.4 CF1, CF2 general-purpose port input control register (XT2PC) (1-bit register)

1) This register is a 1-bit register that controls the general-purpose input at the CF1and CF2 pins.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE43	HHHH 0HHH	R/W	XT2PC	-	-	-	-	XTCFIN	-	-	-

(Bits 7 to 4, and 2 to 0): These bits do not exist. They are always read as 1.

XTCFIN (bit 3): CF1 and CF2 input control

1) This bit and CFSTOP (OCR register (FE0EH), bit 0) are used to select the function of the CF1 and CF2 pins between main clock and general-purpose input port pins. (See 4.2.4.2, "Oscillation control register," for details.)

4.2.4.5 Variable modulation frequency RC oscillator control register (MRCR) (7-bit register)

1) This register is a 7-bit register that controls the operation of the variable modulation frequency RC oscillator circuit and selects the main clock.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE0D	00HX XXXX	R/W	MRCR	MRCSEL	MRCST	-	RCCTD4	RCCTD3	RCCTD2	RCCTD1	RCCTD0

MRCSEL (bit 7): Variable modulation frequency RC oscillator clock select

1) When this bit is set to 1, the variable modulation frequency RC oscillator is selected as the main clock. The variable modulation frequency RC oscillator clock will be the system clock if the main clock is selected as the system clock in the above-mentioned OCR register.
2) When this bit is set to 0, the variable modulation frequency RC oscillator clock is not selected as the main clock; CF is selected as the main clock.
3) This bit is cleared when the microcontroller enters HOLD mode.

MRCST (bit 6): Variable modulation frequency RC oscillation start control

1) A 1 in this bit starts the variable modulation frequency RC oscillator circuit.
2) A 0 in this bit stops the variable modulation frequency RC oscillator circuit.
3) This bit is cleared when the microcontroller enters HOLD mode.

RCCTD4 (bit 4):
RCCTD3 (bit 3):
RCCTD2 (bit 2):
RCCTD1 (bit 1):
RCCTD0 (bit 0):

} **Variable modulation frequency RC oscillator frequency select**

1) These bits set up the source oscillator clock counter value.
2) The frequency of the clock generated by the variable modulation frequency RC oscillator is:
   Source oscillation frequency / ((RCCTD value + 1) × 2)
3) The initial value of RCCTD is undefined.

Note 1: The system clock may set to an excessively high rate depending on the count value configured. This may cause malfunctions if it exceeds the operating clock range.

Note 2: Data may not be set up properly if the internal medium-speed RC oscillator is selected as the system clock and RCCTD is rewritten with MRCSEL (bit 7) set to "H."

Be sure to set MRCSEL (bit 7) to "L" when rewriting RCCTD while selecting the medium-speed RC oscillator clock as the system clock.

Note 3: When switching the system clock, secure an oscillation stabilization time of 100 µs or longer after the variable modulation frequency RC oscillator circuit switches from the "oscillation stopped" to "oscillation enabled" state.

Note 4: The variable modulation frequency RC oscillator circuit may be of 6- or 5-bit counter type which is dependent on the type of the microcontroller. You need to pay attention to this fact and to the correct set of development tools when using this function. This series adopts a 5-bit counter.

Note 5: Depending on the type of SANYO microcontrollers, the initial value of RCCTD is set to a frequency that is close to that of the internal (medium-speed) RC oscillator or it is undefined. The initial value of RCCTD of this series of microcontrollers is undefined.

4.2.4.6 System clock divider control register (CLKDIV) (3-bit register)

1) This register controls the frequency division processing of the system clock.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE0C	HHHH H000	R/W	CLKDIV	-	-	-	-	-	CLKDV2	CLKDV1	CLKDV0

(Bits 7 to 3): These bits do not exist. They are always read as 1.

CLKDV2 (bit 2):
CLKDV1 (bit 1):
CLKDV0 (bit 0):
} **Define the division ratio of the system clock.**

CLKDV2	CLKDV1	CLKDV0	Division Ratio
0	0	0	$\frac{1}{1}$
0	0	1	$\frac{1}{2}$
0	1	0	$\frac{1}{4}$
0	1	1	$\frac{1}{8}$
1	0	0	$\frac{1}{16}$
1	0	1	$\frac{1}{32}$
1	1	0	$\frac{1}{64}$
1	1	1	$\frac{1}{128}$

4.2.5 Example of Switching the CF Oscillator Amplifier Size

1) System clock state
   - Put the system clock into a state other than the CF oscillator (main).
2) Switch the CF oscillation amplifier size to "low."
   - Set CFLAMP (bit 2) of the low-speed RC oscillator control register to 1.
3) Wait for the CF oscillation stabilization time.
   - Wait for the CF oscillation stabilization time specified in the "SANYO Semiconductor Data Sheet."
4) Switch the system clock source.
   - Set oscillator control register, CLKCB4 (bit 4) to 1 and CLKCB5 (bit 5) to 0 to switch the system clock source to "CF oscillator (main)."

Note 1 Do not switch the amplifier size of the CF oscillator when the system clock is set to "CF oscillator (main)." Switching the amplifier size in this case may cause unstable oscillation, resulting in a system malfunction.

Note 2: The operating voltage range differs for the CF oscillator low and normal size amplifiers. Refer to the latest edition of "SANYO Semiconductor Data Sheet" before using the low size CF oscillator amplifier.

4.3 Standby Function

4.3.1 Overview

This series of microcontrollers supports two standby modes, called HALT and HOLD modes, that are used to reduce current consumption at power-failure time or in program standby mode. In a standby mode, the execution of all instructions is suspended.

4.3.2 Functions

1) HALT mode
   - The microcontroller suspends the execution of instructions but its peripheral circuits continue processing (Some serial transfer functions are suspended.)
   - HALT mode is entered by setting bit 0 of the PCON register to 1.
   - Bit 0 of the PCON register is cleared and the microcontroller returns to the normal operating mode when a reset occurs or an interrupt request is accepted.

2) HOLD mode
   - All oscillations are suspended. The microcontroller suspends the execution of instructions and the peripheral circuits stop processing. (Note 1)
   - HOLD mode is entered by setting bit 1 of the PCON register to 1. In this case, bit 0 of the PCON register (HALT mode setting flag) is automatically set.
   - When a reset occurs or a HOLD mode release signal (INT0, INT1, INT2, INT4, or P0INT) is generated, bit 1 of the PCON register is cleared and the microcontroller switches into HALT mode.

Note 1: Do not allow the microcontroller to enter HALT or HOLD mode while AD conversion is in progress. Make sure that ADSTART (ADCRC register, bit 2) is set to 0 before placing the microcontroller into one of the above-mentioned standby modes.

4.3.3 Related Registers

4.3.3.1 Power control register (PCON) (2-bit register)

1) This register is a 2-bit register that specifies the operating mode (normal/HALT/HOLD).
   - See Section 4.3, "Standby Function," for the procedures to enter and exit the microcontroller operating modes.

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE07	HHHH HH00	R/W	PCON	-	-	-	-	-	-	PDN	IDLE

(Bits 7 to 2): These bits do not exist. They are always read as 1.

PDN (bit 1): HOLD mode setting flag

1) This bit must be set with an instruction.
   - When the microcontroller enters HOLD mode, all oscillations (main clock, medium-speed RC, and variable modulation frequency RC) are suspended and the OCR register, bits 1, 4, and 5 and the MRCR register, bits 7 and 6 are cleared.
   - When the microcontroller exits HOLD mode, the medium-speed RC oscillator starts oscillation and is used as the system clock source.
2) PDN is cleared when a HOLD mode release signal (INT0, INT1, INT2, INT4, or P0INT) is generated or a reset occurs.
3) Bit 0 is automatically set when PDN is set.

IDLE (bit 0): HALT mode setting flag

1) Setting this bit places the microcontroller into HALT mode.
2) This bit is automatically set when bit 1 is set.
3) This bit is cleared on acceptance of an interrupt request or on receipt of a reset signal.

PDN	IDLE	Operating mode
0	0	Normal mode
0	1	HALT mode
1	1	HOLD mode

Table 4.3.1 Standby Mode Operations

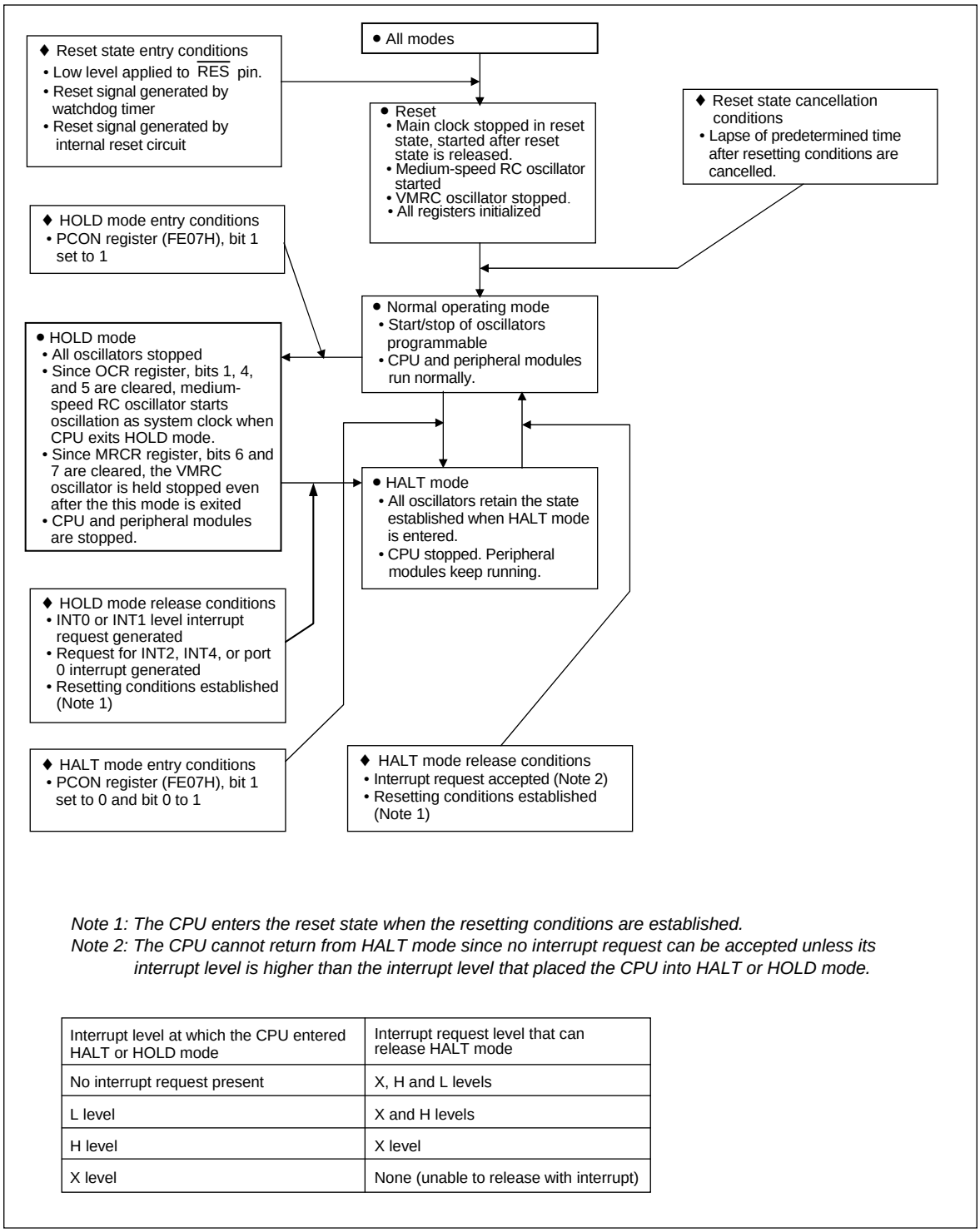
Item/Mode	Reset State	HALT Mode	HOLD Mode
Entry conditions	• $\overline{\text{RES}}$ signal applied • Reset from watchdog timer • Reset generated by the internal reset circuit	PCON register Bit 1=0 Bit 0=1	PCON register Bit 1=1
Data changed on entry	Initialized as shown in separate table.	WDT bits 2 to 0 are cleared if WDT register (FE0F), bit 4 is set.	• WDT bits 2 to 0 are cleared if WDT register (FE0F), bit 4 is set. • PCON, bit 0 turns to 1. • OCR register (FE0E), bits 5, 4, and 1 are cleared • MRCR register (FE0D), bits 7 and 6 are cleared.
Main clock oscillation	Stopped	State established at entry time	Stopped
Internal medium-speed RC oscillation	Running	State established at entry time	Stopped
Variable modulation frequency RC oscillation	Stopped	State established at entry time	Stopped
CPU	Initialized	Stopped	Stopped
I/O pin state	See Table 4.3.2.	←	←
RAM	• $\overline{\text{RES}}$: Undefined • When watchdog timer reset: Data preserved	Data preserved	Data preserved
Peripheral modules	Stopped	State established at entry time (Note 2)	Stopped
Exit conditions	Entry conditions canceled.	• Interrupt request accepted. • Reset/entry conditions established	• Interrupt request from INT0 to INT2, INT4, or P0INT • Reset/entry conditions established
Returned mode	Normal mode	Normal mode (Note1)	HALT (Note1)
Data changed on exit	None	PCON register, bit 0 = 0	PCON register, bit 1 = 0

Note 1: The microcontroller switches into the reset state if it exits the current mode on the establishment of reset/entry conditions.

Note 2: Some serial transfer functions are suspended.

Table 4.3.2 Pin States and Operating Modes (this series)

Pin Name	Reset Time	Normal Mode	HALT Mode	HOLD Mode	On Exit from HOLD
$\overline{\text{RES}}$	• Input	←	←	←	←
CF1	• CF oscillation inverter input • Oscillation not started • Feedback resistor inserted between CF1 and CF2.	• CF oscillation inverter input/general-purpose input controlled by bit 3 of register XT2PC (FE43H). • Oscillation enable/ disable controlled by register OCR (FE0EH). • Feedback resistor between CF1 and CF2 controlled by a program.	←	• CF oscillation inverter input/general-purpose input in setting established at entry time. • Feedback resistor between CF1 and CF2 is in the state established when HOLD mode is entered	• State established when HOLD mode is entered.
CF2	• CF oscillation inverter output • Oscillation not started • Feedback resistor inserted between CF1 and CF2. • VDD level output present regardless of CF1 state.	• CF oscillation inverter input/general-purpose input controlled by bit 3 of register XT2PC (FE43H). • Oscillation enable/ disable controlled by register OCR (FE0EH). • Feedback resistor between CF1 and CF2 controlled by a program.	←	• CF oscillation inverter output/general-purpose input is in the state established when HOLD mode is entered. • Feedback resistor between CF1 and CF2 is in the state established when HOLD mode is entered.	• State established when HOLD mode is entered.
P00-P07	• Input mode • Pull-up resistor off	• Input/output/pull-up resistor controlled by a program	←	←	←
P10-P17	• Input mode • Pull-up resistor off	• Input/output/pull-up resistor controlled by a program	←	←	←
P20-P21	• Input mode • Pull-up resistor off	• Input/output/pull-up resistor controlled by a program	←	←	←
P70	• Input mode • Pull-up resistor off	• Input/output/pull-up resistor controlled by a program • N-channel output transistor for watchdog timer controlled by a program (since on-time is automatically extended, it takes 1920 to 2048 Tcyc for the transistor to go off).	• Input mode • Pull-up resistor off • N-channel output transistor for watchdog timer is off (automatic on-time extension function is reset)	←	• Same as in normal mode.



Note 1: The CPU enters the reset state when the resetting conditions are established.
Note 2: The CPU cannot return from HALT mode since no interrupt request can be accepted unless its interrupt level is higher than the interrupt level that placed the CPU into HALT or HOLD mode.

Interrupt level at which the CPU entered HALT or HOLD mode	Interrupt request level that can release HALT mode
No interrupt request present	X, H and L levels
L level	X and H levels
H level	X level
X level	None (unable to release with interrupt)

Fig. 4.3.1 Standby Mode State Transition Diagram

4.4 Reset Function

4.4.1 Overview

The reset function initializes the microcontroller when it is powered on or when it is running.

4.4.2 Functions

This series of microcontrollers provides the following three types of reset function.

1) External reset via the $\overline{\text{RES}}$ pin

   The microcontroller is reset without fail by applying and holding a low level to the $\overline{\text{RES}}$ pin for 200 μs or longer. Note, however, that a low level of a small duration (less than 200 μs) is likely to trigger a reset.

   The $\overline{\text{RES}}$ pin can be used as a power-on reset pin when it is provided with an external time constant element.

2) Internal reset

   The internal reset function is available in two types: the power-on reset (POR) that triggers a reset when power is turned on and the low-voltage detection reset (LVD) that triggers a reset when the power voltage falls below a certain level. Options are available to set the power-on reset resetting level, to enable and disable the low-voltage detection reset function, and its threshold level.

3) Runaway detection/reset function using a watchdog timer

   The watchdog timer of this series of microcontrollers can be used to detect and reset runaway conditions by connecting a resistor and a capacitor to its external interrupt pin (P70/INT0/T0LCP) and making an appropriate time constant element.

An example of a reset circuit is shown in Figure 4.4.1. The external circuit connected to the reset pin shows an example that the internal reset function is disabled and an external power-on reset circuit is configured.

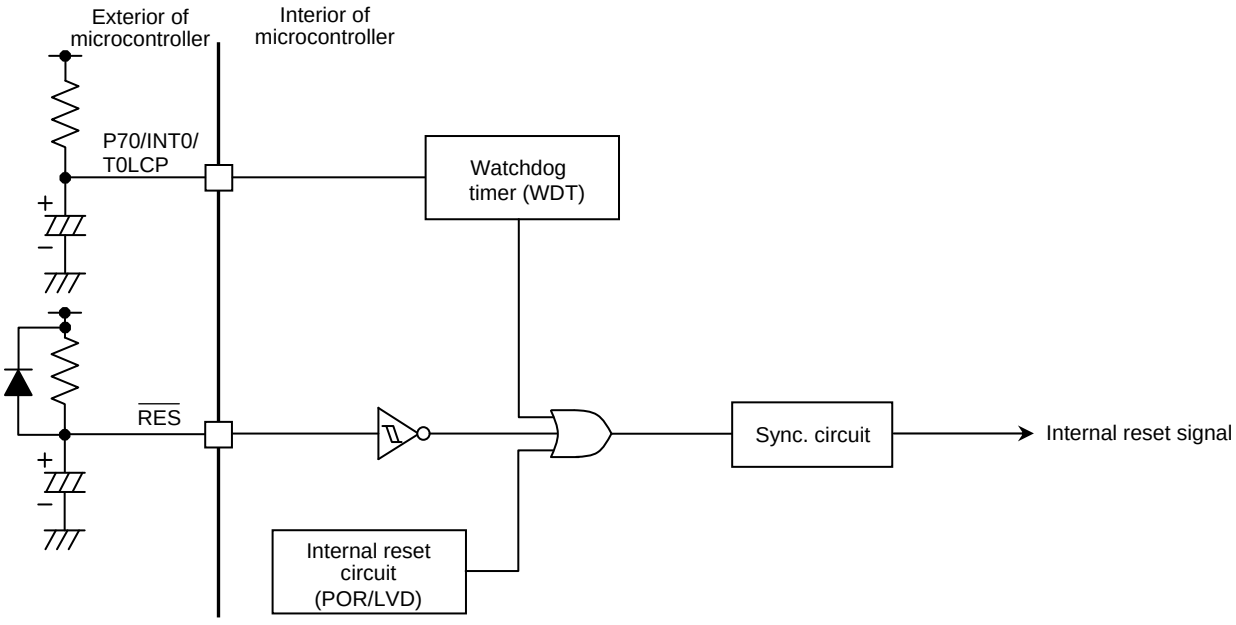


Figure 4.4.1 Sample Reset Circuit Block Diagram

4.4.3 Reset State

When a reset is generated by the $\overline{\text{RES}}$ pin, internal reset circuit, or watchdog timer, the hardware functional blocks of the microcontroller are initialized by a reset signal that is in synchronization with the system clock.

Since the system clock is switched to the internal medium-speed RC oscillator when a reset occurs, hardware initialization is also carried out immediately even at power-on time. Switch the system clock to the main clock after the main clock is stabilized.

On reset, the program counter is initialized to the program start address that is selected by a user option. See Appendix (A-I), “Special Function Register Map,” for the initial values of the special function registers (SFR).

<Notes and precautions>

- *The stack pointer is initialized to 0000H.*
- *Data RAM is never initialized by a reset. Consequently, the contents of RAM are undefined at power-on time.*
- *When using the internal reset function, it is necessary to implement and connect an external circuit to the reset pin according to the user's operating environment. Be sure to review and observe the operating specifications, circuit configuration, precautions, and considerations discussed in Section 4.6, "Internal Reset Function."*

4.5 Watchdog Timer Function

4.5.1 Overview

This series of microcontrollers incorporates a watchdog timer that, with an external RC circuit, detects program runaway conditions.

The watchdog timer charges the external RC circuit that is connected to the P70/INT0/T0LCP pin and, when the level at the pin reaches the high level, triggers a reset or interrupt regarding that a program runaway occurred.

4.5.2 Functions

1) Detection of a runaway condition

   A program that discharges the RC circuit periodically needs to be prepared. If such a program runaways, it will not execute instructions that discharge the RC circuit. This produces a high potential at the P70/INT0/T0LCP pin and the watchdog timer detects a program runaway condition.

2) Actions to be taken following the detection of a runaway condition

   The microcontroller can take one of the following actions when the watchdog timer detects a runaway condition:

   - Reset (program reexecution)
   - External interrupt INT0 generation (program continuation)

     The priority of the external interrupt INT0 can be changed using the master interrupt enable control register (IE).

4.5.3 Circuit Configuration

The watchdog timer is made up of a high-threshold buffer, a pulse stretcher circuit, and a watchdog timer control register. Its configuration diagram is shown in Figure 4.5.1.

- High-threshold buffer

  The high-threshold buffer detects the charging voltage of the external capacitor.

- Pulse stretcher circuit

  The pulse stretcher circuit discharges the external capacitor for longer than the specified time to ensure reliable discharging. The stretching time is from 1920 to 2048 Tcyc.

- Watchdog timer control register (WDT)

  This register controls the operation of the watchdog timer.

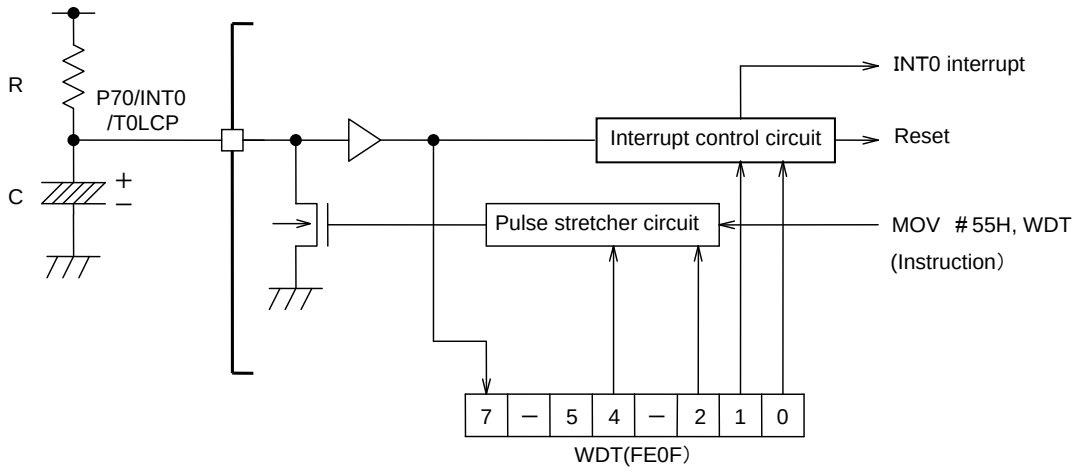


Fig. 4.5.1 Watchdog Timer Circuit

4.5.4 Related Registers

4.5.4.1 Watchdog timer control register (WDT)

Address	Initial value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE0F	0H00 H000	R/W	WDT	WDTFLG	-	WDTB5	WDTHLT	-	WDTCLR	WDTRST	WDTRUN

Bit Name	Function
WDTFLG (bit 7)	Runaway detection flag 0: No runaway 1: Runaway
WDTB5 (bit 5)	General-purpose flag Can be used as a general-purpose flag.
WDTHLT (bit 4)	HALT/HOLD mode function control 0: Enables the watchdog timer. 1: Disables the watchdog timer.
WDTCLR (bit 2)	Watchdog timer clear control 0: Disables clearing of the watchdog timer. 1: Enables clearing of the watchdog timer.
WDTRST (bit 1)	Runaway-time reset control 0: Disables a reset when a runaway condition is detected. 1: Triggers a reset when a runaway condition is detected.
WDTRUN (bit 0)	Watchdog timer operation control 0: Maintains watchdog timer operating state. 1: Starts the watchdog timer operation.

WDTFLG (bit 7): Runaway detection flag

This bit is set when a program runaway condition is detected by the watchdog timer. The application can identify the occurrence of a runaway condition by monitoring this bit (provided that WDTRST is set to 1).

This bit is not reset automatically. It must be reset with an instruction.

WDTB5 (bit 5): General-purpose flag

This bit can be used as a general-purpose flag.

Manipulating this bit exerts no influence on the operation of the functional block.

WDTHLT (bit 4): HALT/HOLD mode function control

This bit enables (0) or disables (1) the watchdog timer when the microcontroller is in HALT or HOLD state. When this bit is set to 1, WDTCLR, WDTRST, and WDTRUN are reset and the watchdog timer is stopped in HALT or HOLD state. When this bit is set to 0, WDTCLR, WDTRST, and WDTRUN remain unchanged and the watchdog timer continues operation even when the microcontroller enters HALT or HOLD state.

To use the watchdog timer function after the microcontroller returns to the normal operating mode from HALT or HOLD mode with this bit set to 1, initialize and set up the watchdog timer again for starting the watchdog timer function.

WDTCLR (bit 2): Watchdog timer clear control

This bit enables (1) or disables (0) the discharge of capacitance from the external capacitor when the watchdog timer is running (WDTRUN=1). Setting this bit to 1 turns on the N-channel transistor at pin P70/INT0/T0LCP when the watchdog timer clear instruction is executed, discharging the external capacitors and clearing the watchdog timer. The pulse stretcher circuit also functions during this process. Setting the bit to 0 disables turning on the N-channel transistor at pin P70/INT0/T0LCP and clearing of the watchdog timer.

If this bit is set to 1 when the watchdog timer is inactive (WDTRUN=0), the N-channel transistor at pin P70/INT0/T0LCP is turned on, discharging the external capacitors and clearing the watchdog timer.

WDTRST (bit 1): Runaway-time reset control

This bit enables (1) or disables (0) the reset sequence when the watchdog timer detects a program runaway condition. When this bit is set to 1, a reset is triggered when a program runaway condition is detected and the microcontroller reexecutes the program starting at the program start address selected by a user option. When this bit is set to 0, no reset occurs when a program runaway is detected. Instead, an external interrupt INT0 is generated and a call is made to vector address 0003H.

WDTRUN (bit 0): Watchdog timer operation control

This bit starts (1) or maintains (0) the state of the watchdog timer. A 1 in this bit starts the watchdog timer function and a 0 exerts no influence on the operation of the watchdog timer. This means that, once the watchdog timer is started, a program will not be able to stop the watchdog timer (stopped by a reset).

Caution

If WDTRST is set to 1, a reset is triggered when the pin P70/INT0/TOLCP goes to the high level even if the watchdog timer is inactive.
The N-channel transistor at pin P70/INT0/T0LCP is turned on if the watchdog timer clear control bit (WDTCLR) is set to 1 when the watchdog timer is inactive (WDTRUN = 0).
Keep this in mind when programming if the watchdog timer function is not to be used. More current than usual may be consumed depending on the program or application circuit.

4.5.4.2 Master interrupt enable control register (IE)

See subsubsection 4.1.4.1, "Master interrupt enable control register," for details.

4.5.4.3 Port 7 control register (P7)

See subsubsection 3.4.3.1, "Port 7 control register," for details.

4.5.5 Using the Watchdog Timer

Code a program so that instructions for clearing the watchdog timer periodically are executed. Select the resistance R and the capacitance C such that the time constant of the external RC circuit is greater than the time interval required to clear the watchdog timer.

1) Initializing the watchdog timer

   All bits of the watchdog timer control register (WDT) are reset when an external reset is triggered through the $\overline{\text{RES}}$ pin. If the P70/INT0/T0LCP pin has been charged up to the high level, discharge it down to the low level before starting the watchdog timer. The internal N-channel transistor is used for discharging. Since it has an on-resistance, a discharging time equal to the time constant of the external capacitance is required.

   Set bits 0 and 4 of the port 7 control register (P7:FE5C) to 0, 0 or 1, 1 to make the P70 port output open.

   - Starting discharge

     Load WDT with 04H to turn on the N-channel transistor at the P70/INT0/T0LCP pin to start discharging the capacitor.

   - Checking the low level

     Checking for data at the P70/INT0/T0LCP pin

     Read the data at the P70/INT0/T0LCP pin with an LD or similar instruction. A 0 indicates that the P70/INT0/T0LCP pin is at the low level.

2) Starting the watchdog timer

   (1) Set bit 2 (WDTCLR) and bit 0 (WDTRUN) to 1.

   (2) Also set bit 1 (WDTRST) to 1 at the same time when a reset is to be triggered when a runaway condition is detected.

   (3) To suspend the operation of the watchdog timer in HOLD or HALT mode, set bit 4 (WDTHLT) at the same time.

   The watchdog timer starts functioning when bit 0 (WDTRUN) is set to 1. Once the watchdog timer starts operation, the watchdog timer control register (WDT) is disabled for write; it is allowed only to clear the watchdog timer and read the watchdog timer control register (WDT). Consequently, the watchdog timer can never be stopped with an instruction. The function of the watchdog timer is stopped only when a reset occurs or when the microcontroller enters HALT or HOLD mode with WDTHLT being set. In this case, bits WDTCLR, WDTRST, and WDTRUN are reset.

3) Clearing the watchdog timer

Immediately when power is turned on, charging the external RC circuit that is connected to the P70/INT0/T0LCP pin is started. When voltage at this pin reaches the high level, a reset or interrupt is generated as specified in the watchdog timer control register (WDT). To run the program in the normal mode, it is necessary to periodically discharge the RC circuit before the voltage at the P70/INT0/T0LCP pin reaches the high level (clearing the watchdog timer). Execute the following instruction to clear the watchdog timer while it is running:

```
MOV   #55H,WDT
```

This instruction turns on the N-channel transistor at the P70/INT0/T0LCP pin. Owing to the pulse stretcher function (keeps the transistor on after the MOV instruction is executed), the capacitor keeps discharging for a period from a minimum of 1920 cycle times to a maximum of 2048 cycle times.

4) Detecting a runaway condition

Unless the above-mentioned instruction is executed periodically, the external RC circuit keeps charging because the watchdog timer is not cleared. As charging proceeds and the voltage at the P70/INT0/T0LCP pin reaches the high level, the watchdog timer considers that a program runaway has occurred and triggers a reset or interrupt. In this case, the runaway detection flag (WDTFLG) is set (provided that WDTRST is set to 1).
If WDTRST is found to be 1 in this case, a reset occurs and execution restarts at the program start address which is selected through a user option. If WDTRST is 0, an external interrupt (INT0) is generated and control is transferred to vector address 0003H.

- **Hints on Use**

1) To realize ultra-low-power operation using HOLD mode, it is necessary not to use the watchdog timer at all or to disable the watchdog timer from running in HOLD mode by setting WDTHLT to 1.

   Be sure to set WDTCLR to 0 when the watchdog timer is not to be used.

2) The P70/INT0/T0LCP pin has two input levels. The threshold level of the input pins of the watchdog timer circuit is higher than that of the port inputs and the interrupt detection level.

   Refer to the latest "SANYO Semiconductor Data Sheet" for the input levels..

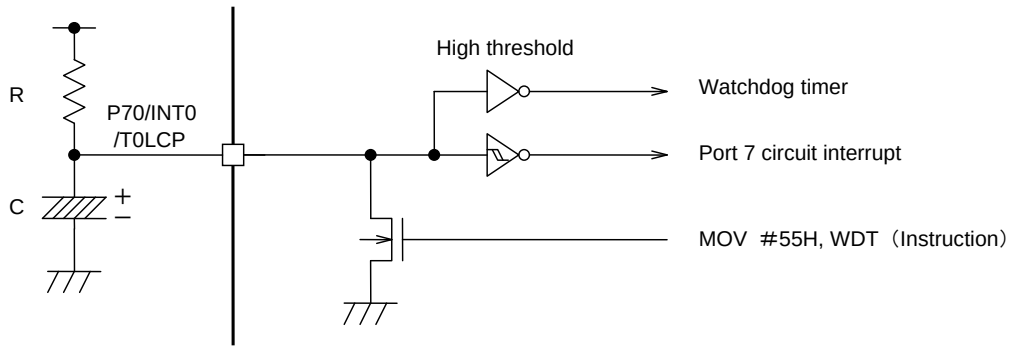


Figure 4.5.2 P70/INT0/T0LCP Pin (P70 Setting: Pull-up Resistor OFF)

3) The external resistor to be connected to the watchdog timer can be omitted by setting bits 4 and 0 of the port 7 control register (P7:FE5C) to 0 and 1 and connecting a programmable pull-up resistor to the P70/INT0/T0LCP pin (see Figure 4.5.3).

The resistance of the pull-up resistor to be adopted in this case varies according to the power source voltage VDD. Calculate the time constant of the watchdog timer while referring to the latest "SANYO Semiconductor Data Sheet."

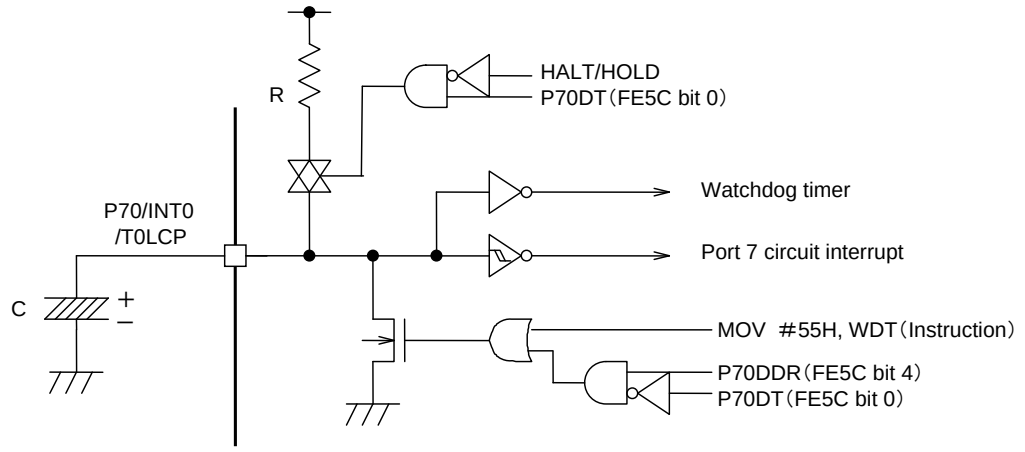


Figure 4.5.3 Sample Application Circuit with a Programmable Pull-up Resistor

4) When the microcontroller enters HALT or HOLD mode with WDTHLT being set to 1, bits WDTCLR, WDTRST, and WDTRUN are reset. To use the watchdog timer function after the microcontroller returns to the normal operating mode from HALT or HOLD mode, initialize and set up the watchdog timer again for starting the operation.

4.6 Internal Reset Function

4.6.1 Overview

This series of microcontrollers incorporates internal reset functions called the power-on reset (POR) and low-voltage detection reset (LVD). The use of these functions contribute to a reduction in the number of externally required reset circuit components (reset IC, etc.).

4.6.2 Functions

1) Power-on reset (POR) function

POR is a hardware feature that generates a reset to the microcontroller when the power is turned on. This function allows the user to select the POR release level by option only when "Disable" of the low voltage detection reset function is selected. It is necessary to use the below-mentioned low voltage detection reset function together with this function, or to configure an external reset circuit if chatter or a temporary power interruption may occur when the power is turned on.

2) Low voltage detection reset (LVD) function

This function, when used together with the POR function, can generate a reset when power is turned on and when the power level lowers. As a user option, "Enable" (use) or "Disable" (non-use) and the detection levels of this function can be specified.

4.6.3 Circuit Configuration

The internal reset circuit consists of the POR, LVD, pulse stretcher circuit, capacitor C_{RES} discharging transistor, external capacitor C_{RES} + pull-up resistor $R_{RES,}$ or pull-up resistor R_{RES} alone. The diagram of the internal reset circuit is provided in Figure 4.6.1.

- Pulse stretcher circuit

  The pulse stretcher circuit stretches the POR and LVD reset signals. It is used to stretch the internal reset period and discharge the external capacitor C_{RES} connected to the reset pin. The stretching time lasts from 30 μs to 100 μs.

- Capacitor C_{RES} discharging transistor

  This is an N-channel transistor used to discharge the external capacitor C_{RES} connected to the reset pin. If the capacitor C_{RES} is not to be connected to the reset pin, it is possible to monitor the internal reset signal by connecting only the external pull-up resistor R_{RES}.

- Option selector circuit

  The option selector circuit is used to configure the LVD options. This circuit selects whether to "Enable" (use) or "Disable" (non-use) the LVD and its detection levels. See Subsection 4.6.4.

- External capacitor C_{RES} + Pull-up resistor R_{RES}

  After the reset signal from the internal reset circuit is released, the reset period is further stretched according to the external CR time constant. This enables the microcontroller to avoid repetitive entries and releases of the reset state from occurring when power-on chatter occurs. The circuit configuration shown in Figure 4.6.1, in which the capacitor C_{RES} and pull-up resistor R_{RES} are externally connected, is recommended when both POR and LVD functions are to be used. The recommended constant values are: C_{RES} = 0.022 μF and R_{RES} = 510 kΩ. The external pull-up resistor R_{RES} must always be installed even when the set's specifications inhibit the installation of the external capacitor C_{RES} to the reset pin.

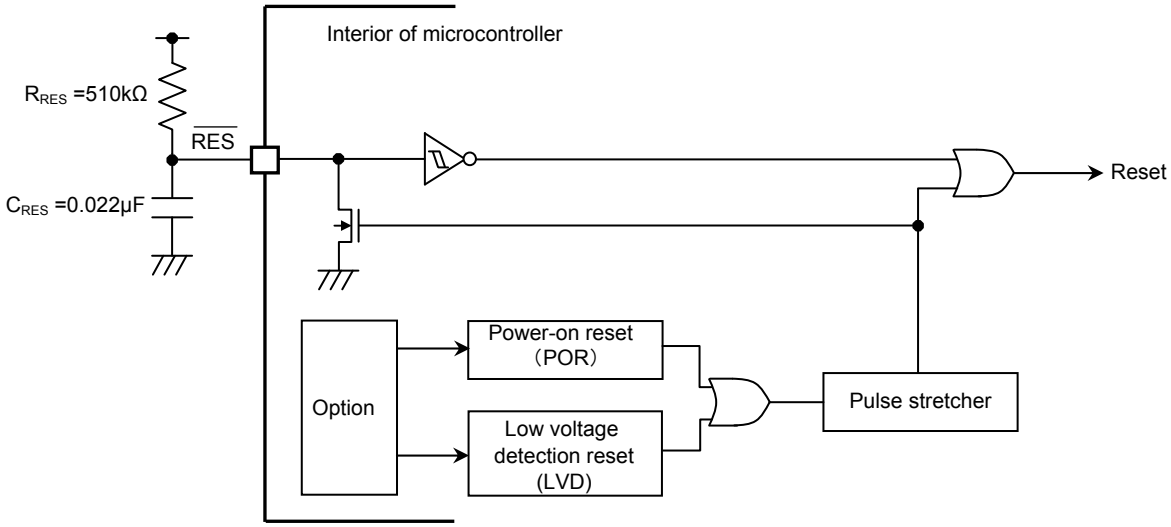


Figure 4.6.1 Internal Reset Circuit Configuration

4.6.4 Options

The POR and LVD options are available for the reset circuit.

1) LVD Reset Function Options			
Enable: Use		**Disable: Non-use**	
2) LVD Reset Level Option		3) POR Release Level Option	
Typical Value of Selected Option	Min. Operating VDD Value (*)	Typical Value of Selected Option	Min. Operating VDD Value (*)
—	—	"1.67V"	1.8V to
"1.91V"	2.1V to	"1.97V"	2.1V to
"2.01V"	2.2V to	"2.07V"	2.2V to
"2.31V"	2.5V to	"2.37V"	2.5V to
"2.51V"	2.7V to	"2.57V"	2.7V to
"2.81V"	3.0V to	"2.87V"	3.0V to
"3.79V"	4.0V to	"3.86V"	4.0V to
"4.28V"	4.5V to	"4.35V"	4.5V to

* The minimum operating VDD value specifies the approximate lower limit of the VDD value that the selected POR release level or LVD reset level can be effected without generating a reset.

1) LVD reset function option

When “Enable” is selected, a reset is generated at the voltage that is selected by the LVD reset level option.

Note 1: In this configuration, an operating current of several μA always flows in all modes.

When "Disable" is selected, no LVD reset is generated.

Note 2: In this configuration, no operating current will flow in all modes.

* See the sample operating waveforms of the reset circuit shown in Subsection 4.6.5 for details.

2) LVD reset level option

The LVD reset level can be selected from 7 level values only when “Enable” is selected in the LVD reset function options. Select the appropriate detection level according to the user's operating conditions.

3) POR release level option

The POR release level can be selected from 8 levels only when “Disable” is selected in the LVD reset function options. When not using the internal reset circuit, set the POR release level to the lowest level (1.67V) that will not affect the minimum guaranteed operating voltage.

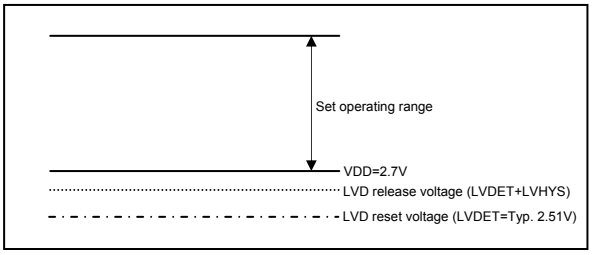
Note 3: No operating current flows when the POR reset state is released.

Note 4: See the notes in paragraph 2) of Subsection 4.6.6 when selecting a POR release level that is lower than the minimum guaranteed operating voltage (1.67V).

- **Selection example 1**

  Selecting the optimum LVD reset level to keep the microcontroller running without resetting it until VDD falls below 2.7V according to the set's requirements

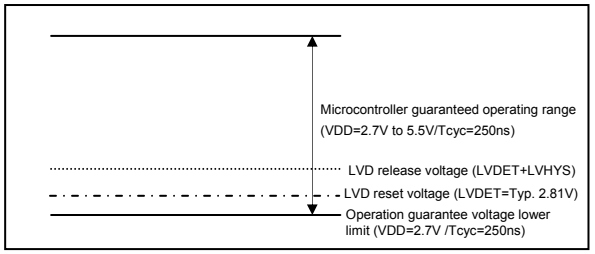
  Set the LVD reset function option to "Enable" and select "2.51V" as the LVD reset level.



- **Selection example 2**

  Selecting the optimum LVD reset level that meets the guaranteed operating conditions to VDD= 2.7V/Tcyc=250 ns

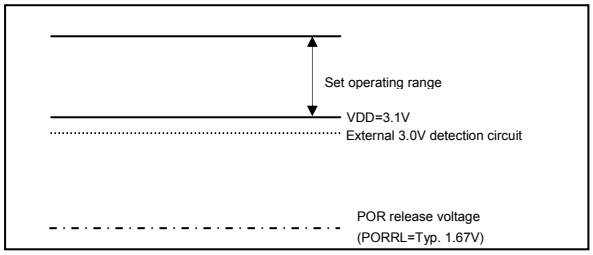
  Set the LVD reset function option to "Enable" and select "2.81V" as the LVD reset level.



- **Selection example 3**

  Disabling the internal reset circuit and using an external reset IC that can detect and react at 3.0V (see also paragraph 1) of Subsection 4.6.7)

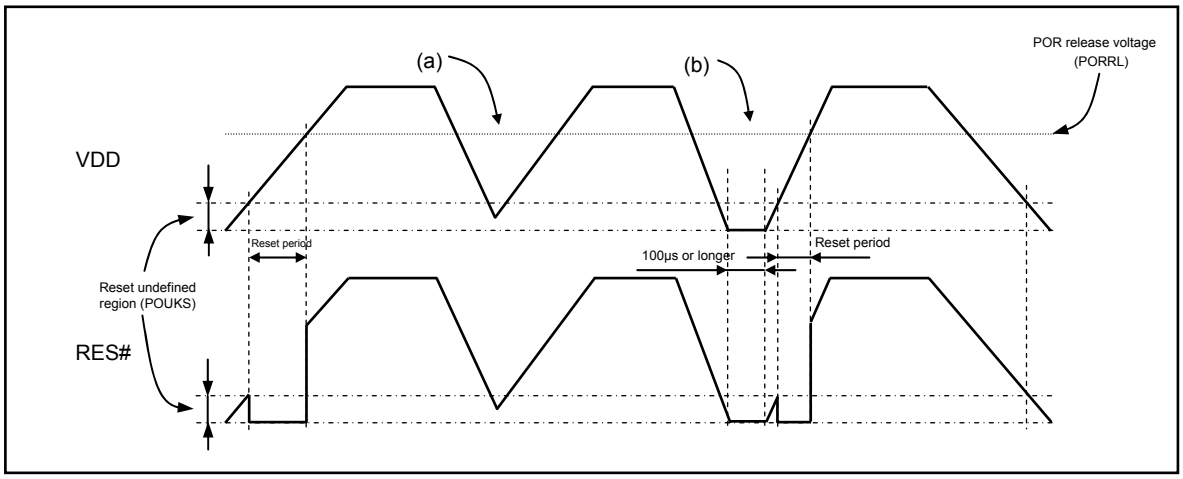
  Set the LVD reset function option to "Disable" and select "1.67V" as the POR release level.



Note 5: The operation guarantee values (voltage/operating frequency) shown in the examples vary with the microcontroller type. Be sure to see the latest "SANYO Semiconductor Data Sheet" and select the appropriate voltage level.

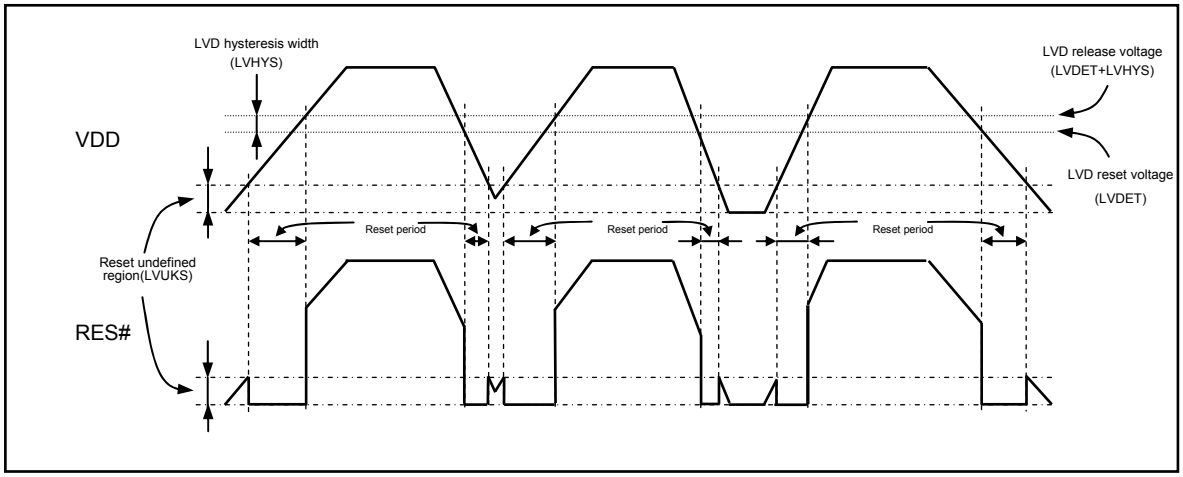
4.6.5 Sample Operating Waveforms of the Internal Reset Circuit

1) Waveform observed when only POR is used (LVD not used)
(Reset pin: Pull-up resistor R_{RES} only)



- There exists an undefined region (POUKS), before the POR transistor starts functioning normally.
- The POR function generates a reset only when the power is turned on starting at the VSS level. The reset release voltage in this case may have some range. Refer to the latest "SANYO Semiconductor Data Sheet" for details.
- No stable reset will be generated if power is turned on again if the power level does not go down to the VSS level as shown in (a). If such a case is anticipated, use the LVD function together as explained in 2) or implement an external reset circuit.
- A reset is generated only when the power level goes down to the VSS level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.

2) Waveform observed when both POR and LVD functions are used
(Reset pin: Pull-up resistor R_{RES} only)



- There also exists an undefined region (LVUKS), before the transistor starts functioning normally when both POR and LVD functions are used.
- Resets are generated both when power is turned on and when the power level lowers. The reset release voltage and entry voltage in this case may have some range. Refer to the latest "SANYO Semiconductor Data Sheet" for details.
- A hysteresis width (LVHYS) is provided to prevent repetitions of reset release and entry cycles near the detection level.

4.6.6 Notes on the Use of the Internal Reset Circuit

1) When generating resets only with the internal POR function

When generating resets using only the internal POR function, do not short the reset pin directly to VDD as when using it with the LVD function. Be sure to use an external capacitor C_{RES} of an appropriate capacitance and a pull-up resistor R_{RES} or the pull-up resistor R_{RES} alone. Test the circuit extensively under the anticipated power supply conditions to verify that resets are reliably generated.

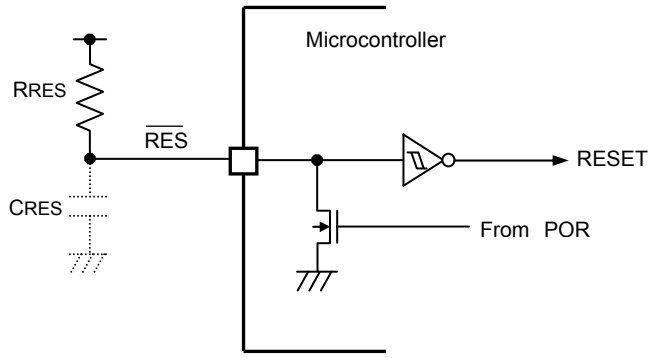


Figure 4.6.2 Reset Circuit Configuration Using Only the Internal POR Function

2) When selecting a release voltage level of 1.67V only with the internal POR function

When selecting an internal POR release level of 1.67V, connect the external capacitor C_{RES} and pull-up resistor R_{RES} of the values that match the power supply rise time to the reset pin and make necessary adjustments so that the reset state is released after the release voltage exceeds the minimum guaranteed operating voltage. Alternatively, set and hold the voltage level of the reset pin at the low level until the release voltage exceeds the minimum guaranteed operating voltage.

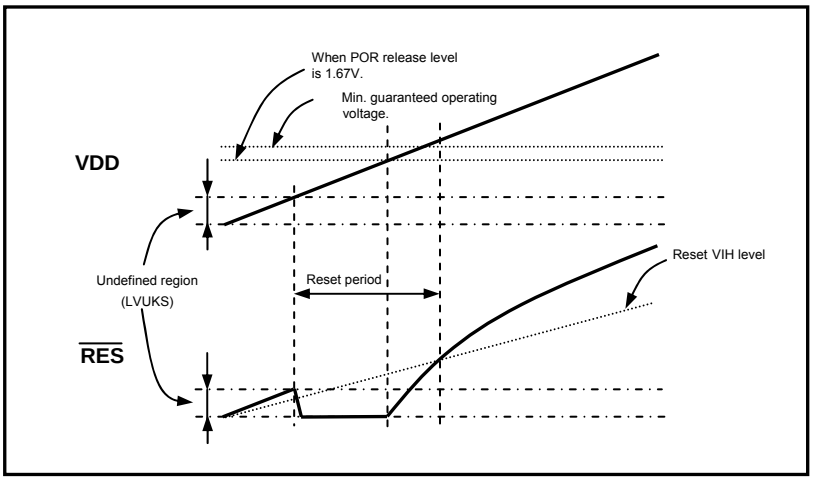


Figure 4.6.3 Sample Release Level Waveform in Internal POR Only Configuration

3) When temporary power interruption or voltage fluctuations shorter than several hundred μs are anticipated

The response time measured from the time the LVD senses a power voltage drop at the option-selected level until it generates a reset signal is defined as the minimum low-voltage detection width TLVDW shown in Figure 4.6.4 (see "SANYO Semiconductor Data Sheet"). If temporary power interruption or power voltage fluctuations shorter than this minimum low-voltage detection width are anticipated, be sure to take the preventive measures shown in Figure 4.6.5 or other necessary measures.

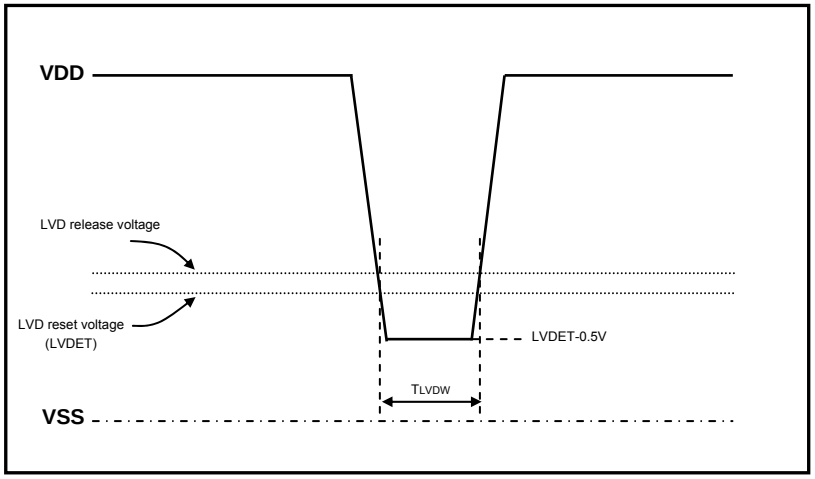


Figure 4.6.4 Example of Power Interruption or Voltage Fluctuation Waveform

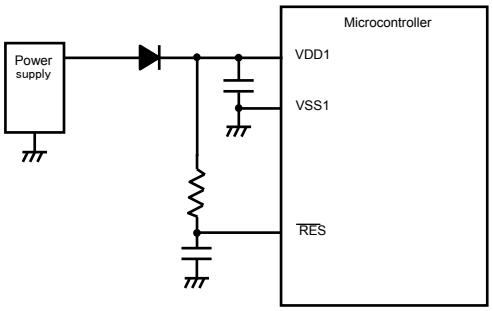


Figure 4.6.5 Example of Power Interruption/Voltage Fluctuation Countermeasures

4.6.7 Notes to be Taken When Not Using the Internal Reset Circuit

1) When configuring an external reset IC without using the internal reset circuit

The internal POR function is activated and the capacitor CRES discharging N-channel transistor connected to the reset pin turns on when power is turned on even if the internal reset circuit is not used. For this reason, when connecting an external reset IC, adopt a reset IC of a type whose detection level is not lower than the minimum guaranteed operating voltage level and select the lowest POR release level (1.67V) that does not affect the minimum guaranteed operating voltage. The figures provided below show sample reset circuit configurations that use reset ICs of N-channel open drain and CMOS types, respectively.

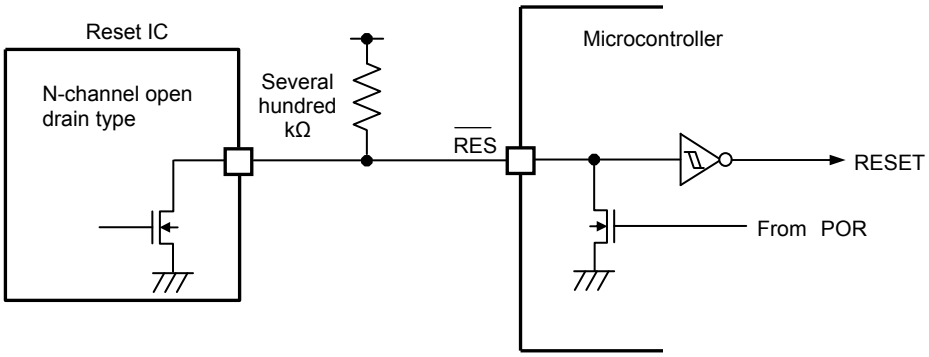


Figure 4.6.6 Sample Reset Circuit Configuration Using an N-channel Open Drain Type Reset IC

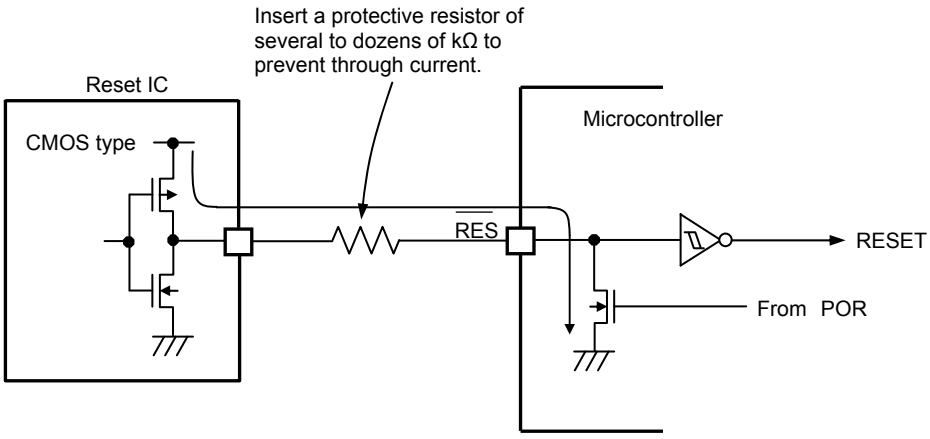


Figure 4.6.7 Sample Reset Circuit Configuration Using a CMOS Type Reset IC

2) When configuring the external POR circuit without using the internal reset circuit

The internal POR is active when power is turned on even if the internal reset circuit is not used as in case 1) in Subsection 4.6.7. When configuring an external POR circuit with a C_{RES} value of 0.1µF or larger to obtain a longer reset period than with the internal POR, however, be sure to connect an external diode D_{RES} as shown in Figure 4.6.8.

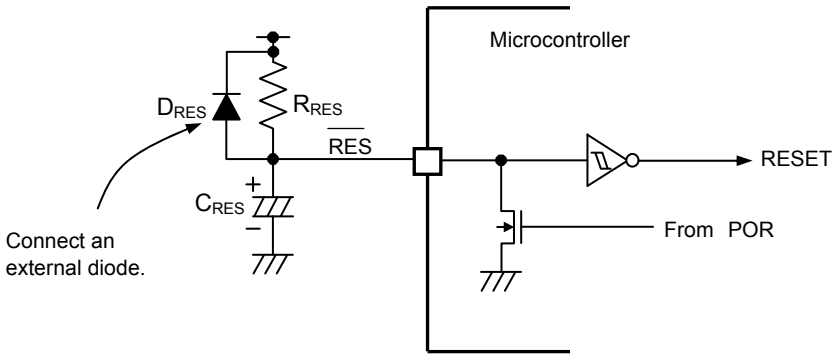


Figure 4.6.8 Sample External POR Circuit Configuration

Internal Reset

Appendixes

Table of Contents

Appendix-I

Appendix-II

Address	Initial value	R/W	LC872R00	Remarks	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0-007F	XXXX XXXX	R/W	RAM128B	9-bit long									
FE00	0000 0000	R/W	AREG		-	AREG7	AREG6	AREG5	AREG4	AREG3	AREG2	AREG1	AREG0
FE01	0000 0000	R/W	BREG		-	BREG7	BREG6	BREG5	BREG4	BREG3	BREG2	BREG1	BREG0
FE02	0000 0000	R/W	CREG		-	CREG7	CREG6	CREG5	CREG4	CREG3	CREG2	CREG1	CREG0
FE03													
FE04													
FE05													
FE06	0000 0000	R/W	PSW		-	CY	AC	PSWB5	PSWB4	LDCBNK	OV	P1	PARITY
FE07	HHHH HH00	R/W	PCON		-	-	-	-	-	-	-	PDN	IDLE
FE08	0000 HH00	R/W	IE		-	IE7	XFLG	HFLG	LFLG	-	-	XCNT1	XCNT0
FE09	0000 0000	R/W	IP		-	IP4B	IP43	IP3B	IP33	IP2B	IP23	IP1B	IP13
FE0A	0000 0000	R/W	SPL		-	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
FE0B	0000 0000	R/W	SPH		-	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8
FE0C	HHHH H000	R/W	CLKDIV		-	-	-	-	-	-	CLKDV2	CLKDV1	CLKDV0
FE0D	00HX XXXX	R/W	MRCR		-	MRCSEL	MRCST	-	RCCTD4	RCCTD3	RCCTD2	RCCTD1	RCCTD0
FE0E	0H00 XX00	R/W	OCR	XT1 and XT2 read at bits 2 and 3	-	CLKSGL	-	CLKCB5	CLKCB4	XT2IN	XT1IN	RCSTOP	CFSTOP
FE0F	0H00 H000	R/W	WDT		-	WDTFLG	-	WDTB5	WDTHLT	-	WDTCLR	WDTRST	WDTRUN
FE10	0000 0000	R/W	TOCNT		-	TOHRUN	TOLRUN	TOLONG	TOLEXT	TOHCMP	TOHIE	TOLCMP	TOLIE
FE11	0000 0000	R/W	TOPRR	Prescaler is 8 bits long. (max.256Tcyc)	-	TOPRR7	TOPRR6	TOPRR5	TOPRR4	TOPRR3	TOPRR2	TOPRR1	TOPRR0
FE12	0000 0000	R	TOL		-	TOL7	TOL6	TOL5	TOL4	TOL3	TOL2	TOL1	TOL0
FE13	0000 0000	R	TOH		-	TOH7	TOH6	TOH5	TOH4	TOH3	TOH2	TOH1	TOH0
FE14	0000 0000	R/W	TOLR		-	TOLR7	TOLR6	TOLR5	TOLR4	TOLR3	TOLR2	TOLR1	TOLR0
FE15	0000 0000	R/W	TOHR		-	TOHR7	TOHR6	TOHR5	TOHR4	TOHR3	TOHR2	TOHR1	TOHR0
FE16	XXXX XXXX	R	TOCAL	Timer 0 capture register L	-	TOCAL7	TOCAL6	TOCAL5	TOCAL4	TOCAL3	TOCAL2	TOCAL1	TOCAL0
FE17	XXXX XXXX	R	TOCAH	Timer 0 capture register H	-	TOCAH7	TOCAH6	TOCAH5	TOCAH4	TOCAH3	TOCAH2	TOCAH1	TOCAH0
FE18													
FE19													
FE1A													
FE1B													
FE1C													
FE1D													

Address	Initial value	R/W	LC872R00	Remarks	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE1E													
FE1F													
FE20													
FE21													
FE22													
FE23													
FE24													
FE25													
FE26													
FE27													
FE28													
FE29													
FE2A													
FE2B													
FE2C													
FE2D													
FE2E													
FE2F													
FE30													
FE31													
FE32													
FE33													
FE34	0000 0000	R/W	SCON1		-	SI1M1	SI1M0	SI1RUN	SI1REC	SI1DIR	SI1OVR	SI1END	SI1IE
FE35	00000 0000	R/W	SBUF1	9-bit register	SBUF18	SBUF17	SBUF16	SBUF15	SBUF14	SBUF13	SBUF12	SBUF11	SBUF10
FE36	0000 0000	R/W	SBR1		-	SBRG17	SBRG16	SBRG15	SBRG14	SBRG13	SBRG12	SBRG11	SBRG10
FE37													
FE38													
FE39													
FE3A													
FE3B													
FE3C													
FE3D													

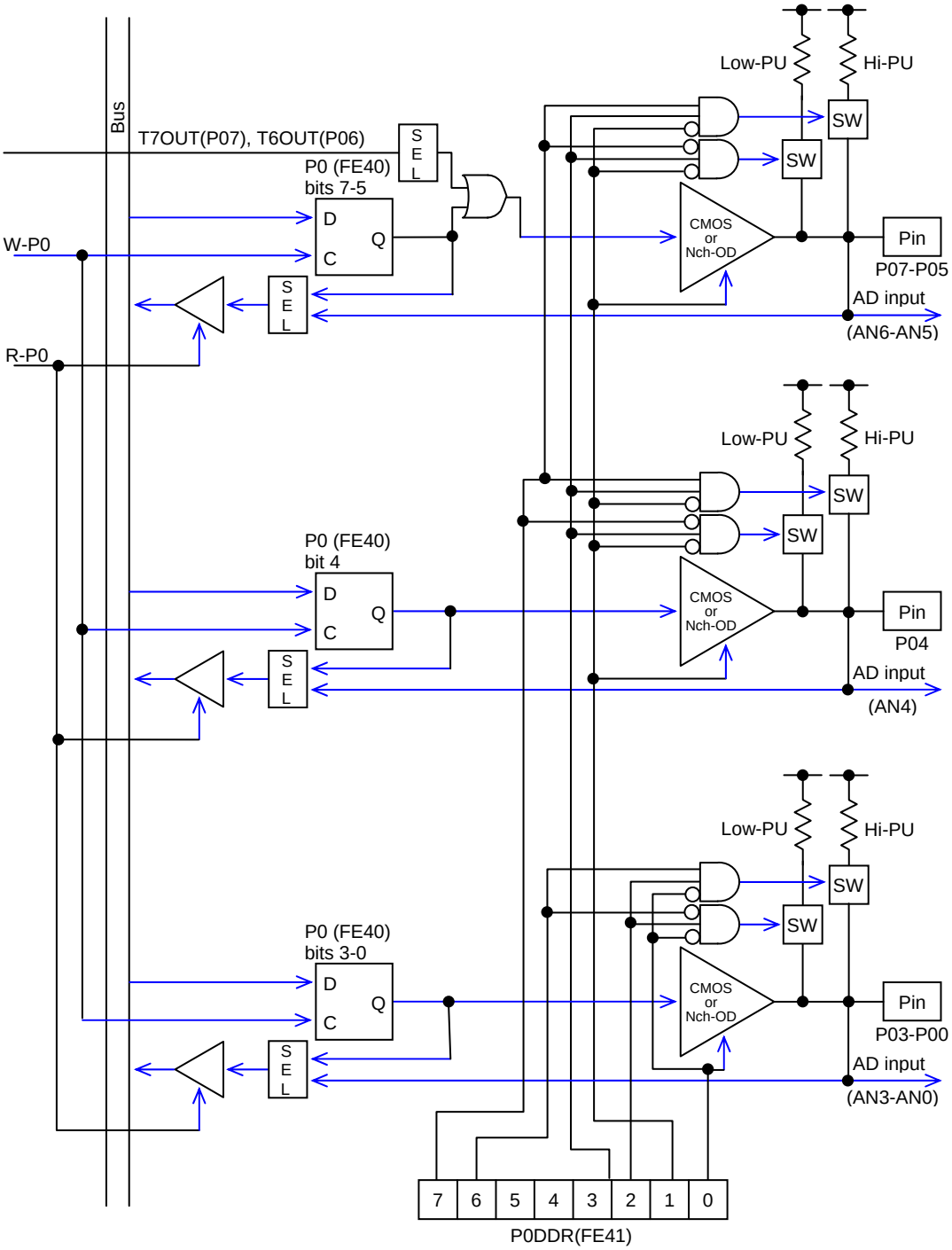
Address	Initial value	R/W	LC872R00	Remarks	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE3E													
FE3F													
FE40	0000 0000	R/W	P0		-	P07	P06	P05	P04	P03	P02	P01	P00
FE41	0000 0000	R/W	P0DDR		-	P0HPUS	P0LPUS	P0FLG	P0IE	P0HPU	P0LPU	P0HDDR	P0LDDR
FE42	00HH HHHH	R/W	P0FCR		-	T70E	T60E	-	-	-	-	-	-
FE43	HHHH 0HHH	R/W	XT2PC	Oscillation pin/general-purpose port input control	-	-	-	-	-	XTCFIN	-	-	-
FE44	0000 0000	R/W	P1		-	P17	P16	P15	P14	P13	P12	P11	P10
FE45	0000 0000	R/W	P1DDR		-	P17DDR	P16DDR	P15DDR	P14DDR	P13DDR	P12DDR	P11DDR	P10DDR
FE46	HH00 0HHH	R/W	P1FCR		-	-	-	P15FCR	P14FCR	P13FCR	-	-	-
FE47	0000 HHH0	R/W	P1TST		-	FIX0	FIX0	FIX0	FIX0	-	-	-	FIX0
FE48	HHHH HH00	R/W	P2		-	-	-	-	-	-	-	P21	P20
FE49	HHHH HH00	R/W	P2DDR		-	-	-	-	-	-	-	P21DDR	P20DDR
FE4A	0000 0000	R/W	I45CR		-	FIX0	FIX0	FIX0	FIX0	INT4HEG	INT4LEG	INT4IF	INT4IE
FE4B	0000 0000	R/W	I45SL		-	FIX0	FIX0	FIX0	FIX0	I4SL3	I4SL2	I4SL1	I4SL0
FE4C													
FE4D													
FE4E													
FE4F													
FE50													
FE51													
FE52													
FE53													
FE54													
FE55													
FE56													
FE57													
FE58	0000 0000	R/W	ADCRC	12-bit AD control	-	ADCHSEL3	ADCHSEL2	ADCHSEL1	ADCHSEL0	ADCR3	ADSTART	ADENDF	ADIE
FE59	0000 0000	R/W	ADMRC	12-bit AD mode	-	ADMD4	ADMD3	ADMD2	ADMD1	ADMD0	ADMR2	ADTM1	ADTM0
FE5A	0000 0000	R/W	ADRLC	12-bit AD conversion result L	-	DATAL3	DATAL2	DATAL1	DATAL0	ADRL3	ADRL2	ADRL1	ADTM2
FE5B	0000 0000	R/W	ADRHC	1-2bit AD conversion result H	-	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
FE5C	HHH0 HHH0	R/W	P7	1-bit IO (4:DDR 0:DATA)	-	-	-	-	P70DDR	-	-	-	P70DT
FE5D	0000 0000	R/W	I01CR		-	INT1LH	INT1LV	INT1IF	INT1IE	INT0LH	INT0LV	INT0IF	INT0IE

Address	Initial value	R/W	LC872R00	Remarks	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE5E	0000 0000	R/W	I23CR		-	INT3HEG	INT3LEG	INT3IF	INT3IE	INT2HEG	INT2LEG	INT2IF	INT2IE
FE5F	00HH H000	R/W	ISL		-	STOHCP	STOLCP	-	-	-	NFSEL	NFON	STOIN
FE60													
FE61													
FE62													
FE63													
FE64													
FE65													
FE66													
FE67													
FE68													
FE69													
FE6A													
FE6B													
FE6C													
FE6D													
FE6E													
FE6F													
FE70													
FE71													
FE72													
FE73													
FE74													
FE75													
FE76													
FE77													
FE78	0000 0000	R/W	T67CNT		-	T7C1	T7C0	T6C1	T6C0	T7OV	T7IE	T6OV	T6IE
FE79													
FE7A	0000 0000	R/W	T6R		-	T6R7	T6R6	T6R5	T6R4	T6R3	T6R2	T6R1	T6R0
FE7B	0000 0000	R/W	T7R		-	T7R7	T7R6	T7R5	T7R4	T7R3	T7R2	T7R1	T7R0
FE7C	HHHH HOHH	R/W	SLWRC		-	-	-	-	-	-	CFLAMP	-	-

Address	Initial value	R/W	LC872R00	Remarks	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE7D													
FE7E	0000 0000	R/W	FSR0	Flash control (bit 4 is R/0)	-	FSR0B7 Fix to 0	FSR0B6 Fix to 0	FSAERR	FSWOK	INTHIGH	FSLDAT	FSPGL	FSWREQ
FE7F													
FE80													
FE81													
FE82													
FE83													
FE84													
FE85													
FE86													
FE87													
FE88													
FE89													
FE8A													
FE8B													
FE8C													
FE8D													
FE8E													
FE8F													
FE90													
FE91													
FE92													
FE93													
FE94													
FE95													
FE96													
FE97													
FE98													
FE99													
FE9A													
FE9B													

Address	Initial value	R/W	LC872R00	Remarks	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE9C													
FE9D													
FE9E													
FE9F													
FEA0													
FEA1													
FEA2													
FEA3													
FEA4													
FEA5													
FEA6													
FEA7													
FEA8													
FEA9													
FEAA													
FEAB													
FEAC													
FEAD													
FEAE													
FEAF													
FEB0													
FEB1													
FEB2													
FEB3													
FEB4													
FEB5													
FEB6													
FEB7													
FEB8													
FEB9													
FEBA													
FEBB													

ｱﾄﾞﾚｽ	Initial value	R/W	LC872R00	Remarks	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FEBC													
FEBD													
FEBE													
FEBF													
FEC0													
FEC1													
FEC2													
FEC3													
FEC4													
FEC5													
FEC6													
FEC7													
FEC8													
FEC9													
FECA													
FECB													
FECC													
FECD													
FECE													
FECF													
FED0													
FED1													
FED2													
FED3													
FED4													
FED5													
FED6													
FED7													
FED8													
FED9													
FEDA													
FEDB													



Port	Special Function Input	Function Output
P07	None	Timer 7 toggle output
P06	AD analog 6 input	Timer 6 toggle output
P05	AD analog 5 input	None
P04	AD analog 4 input	None
P03	AD analog 3 input	None
P02	AD analog 2 input	None
P01	AD analog 1 input	None
P00	AD analog 0 input	None

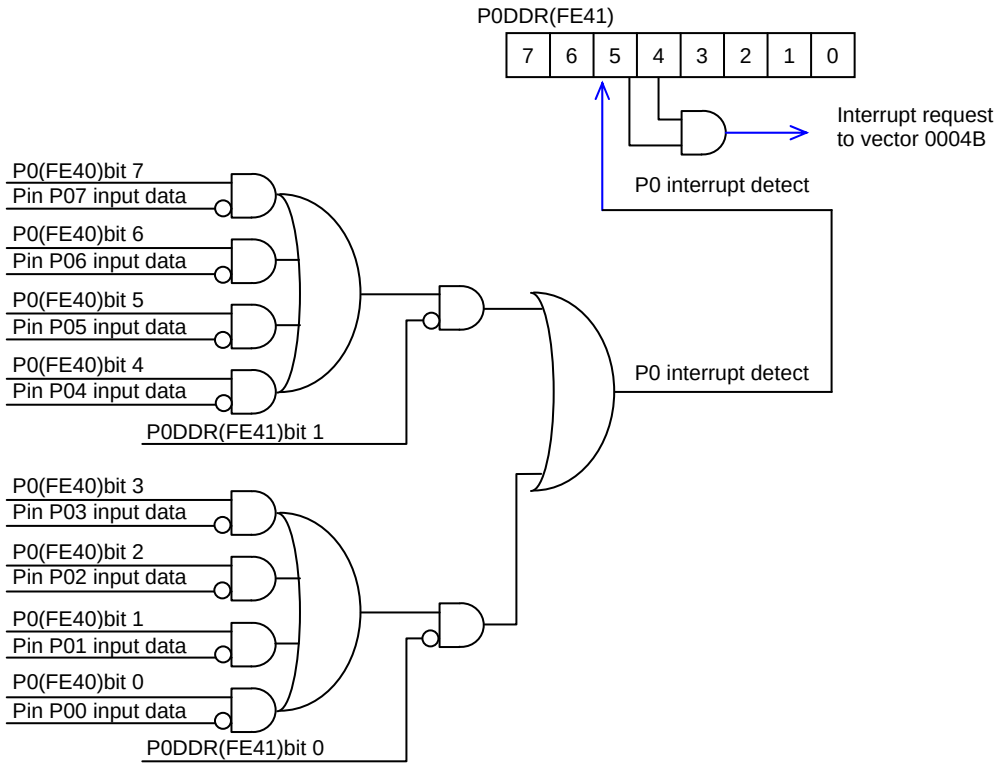
Table of Port 0 multiplexed pin functions

Pull-up resistor is:
Not attached if Nch-OD option is selected.
Programmable if CMOS option is selected.

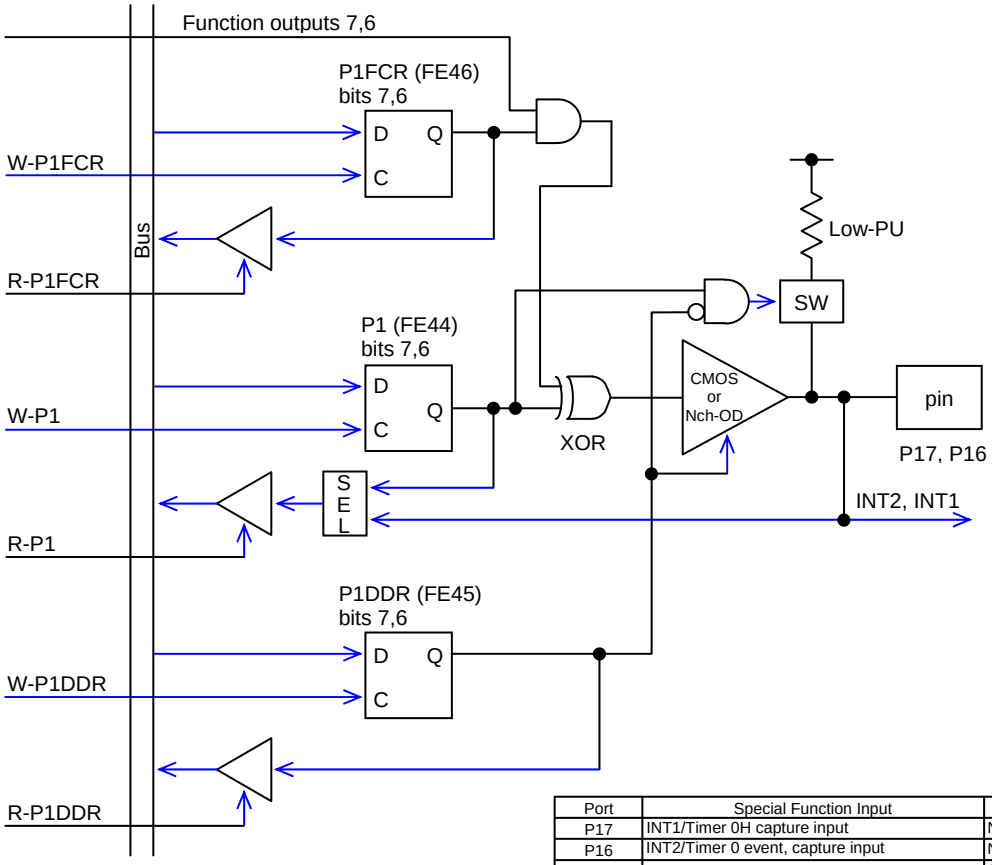
Port 0 Block Diagram

Option: Output type (CMOS or N-channel OD) selectable in 1-bit units

Port Block Diagram

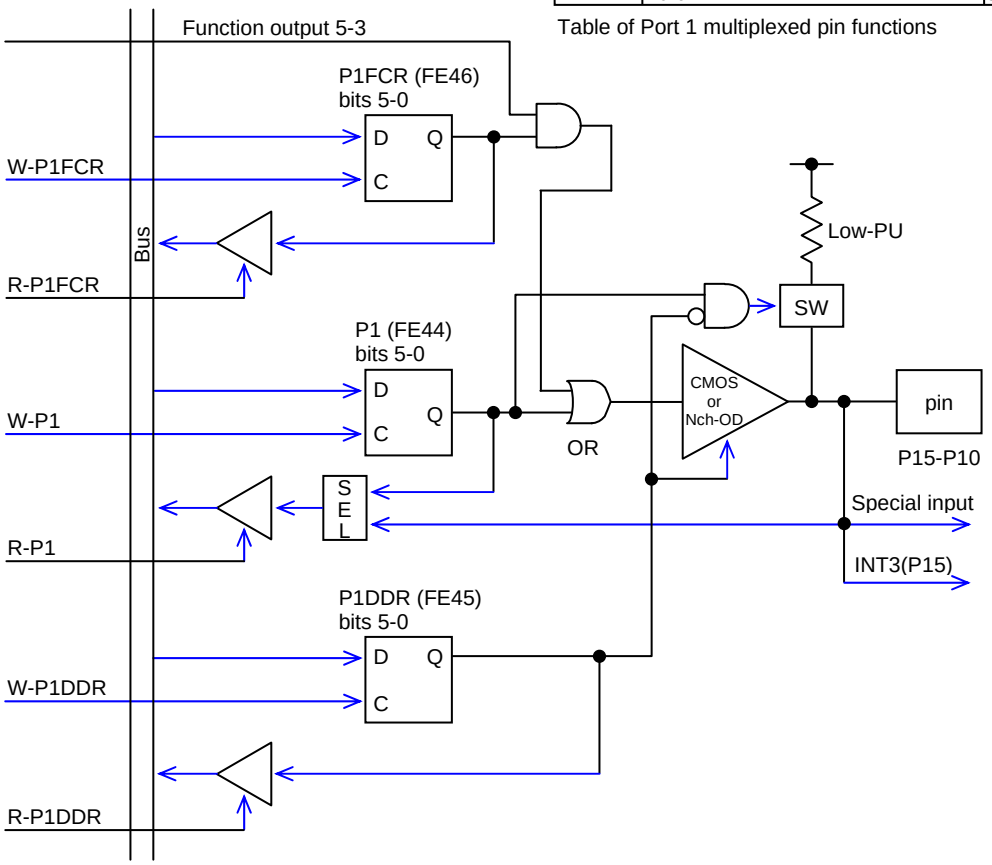


Port 0 (Interrupt) Block Diagram



Port	Special Function Input	Function Output
P17	INT1/Timer 0H capture input	None
P16	INT2/Timer 0 event, capture input	None
P15	INT3/SIO1 clock/Timer 0 event, capture input	SIO1 clock output
P14	SIO1 data input	SIO1 data output
P13	None	SIO1 data output

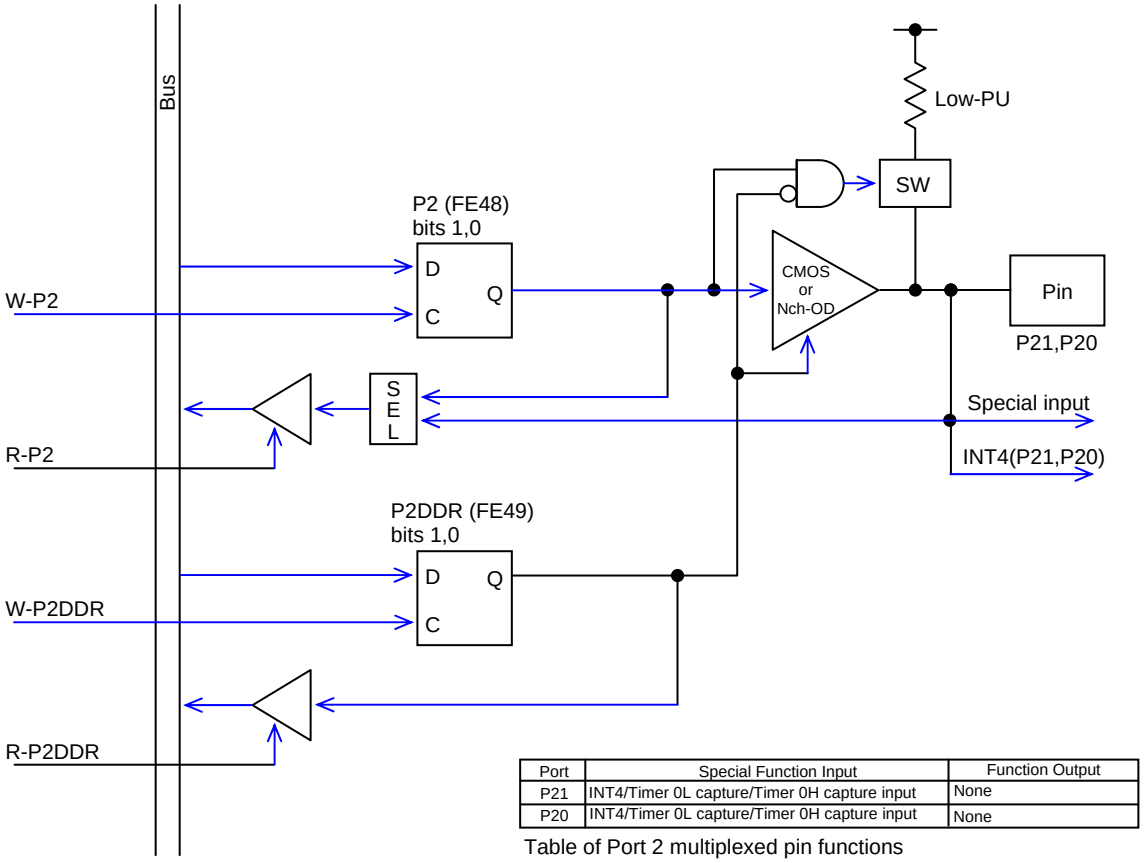
Table of Port 1 multiplexed pin functions



Port 1 Block Diagram

Option: Output type (CMOS or N-channel-OD) selectable in 1-bit units

Port Block Diagram

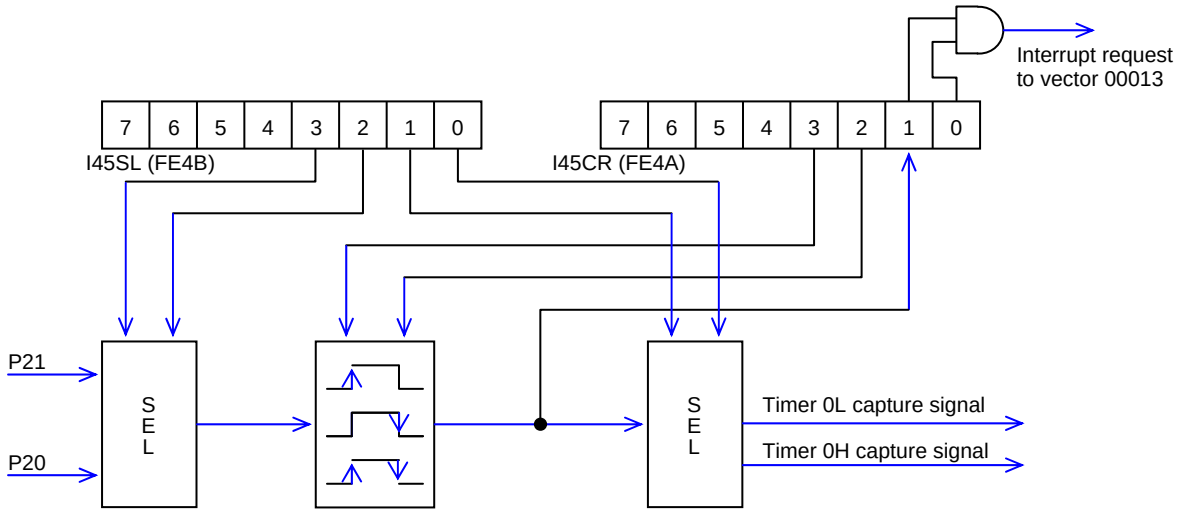


Port	Special Function Input	Function Output
P21	INT4/Timer 0L capture/Timer 0H capture input	None
P20	INT4/Timer 0L capture/Timer 0H capture input	None

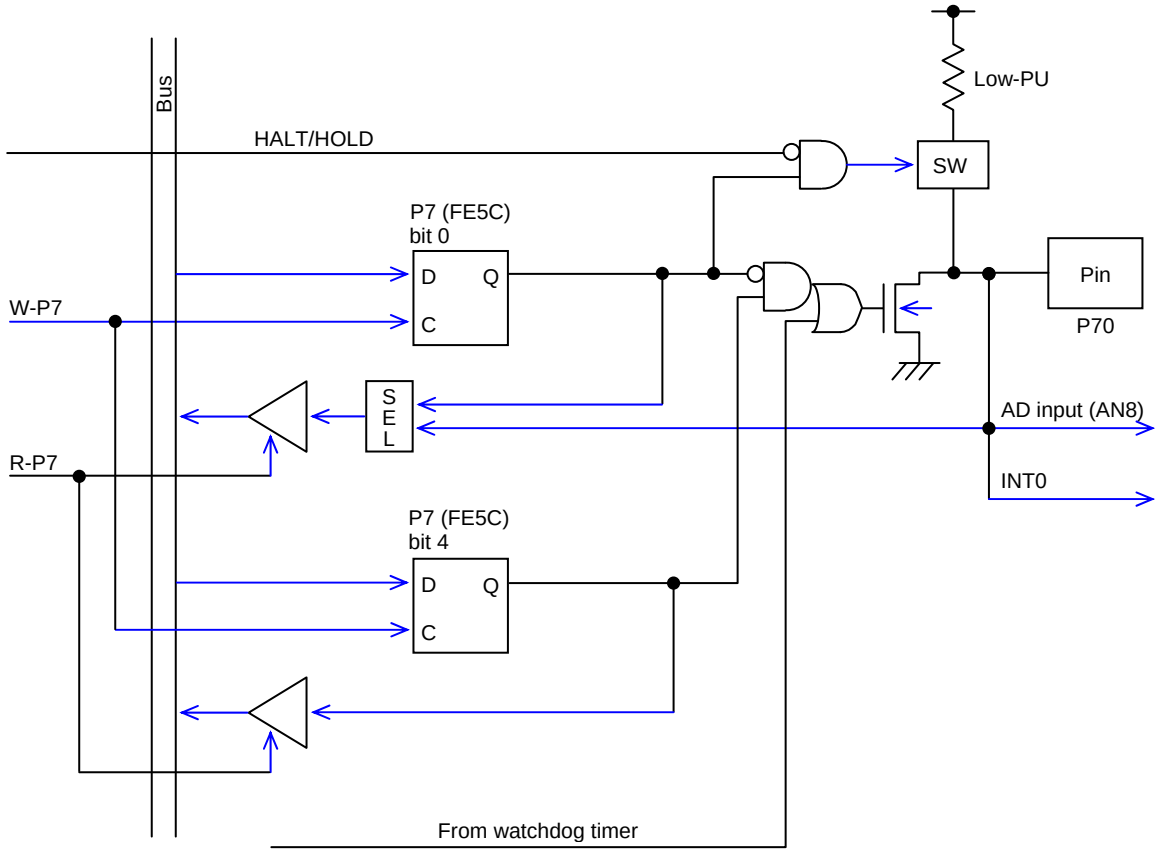
Table of Port 2 multiplexed pin functions

Port 2 Block Diagram

Option: Output type (CMOS or N-channel-OD) selectable in 1-bit units



Port 2 (Interrupt) Block Diagram

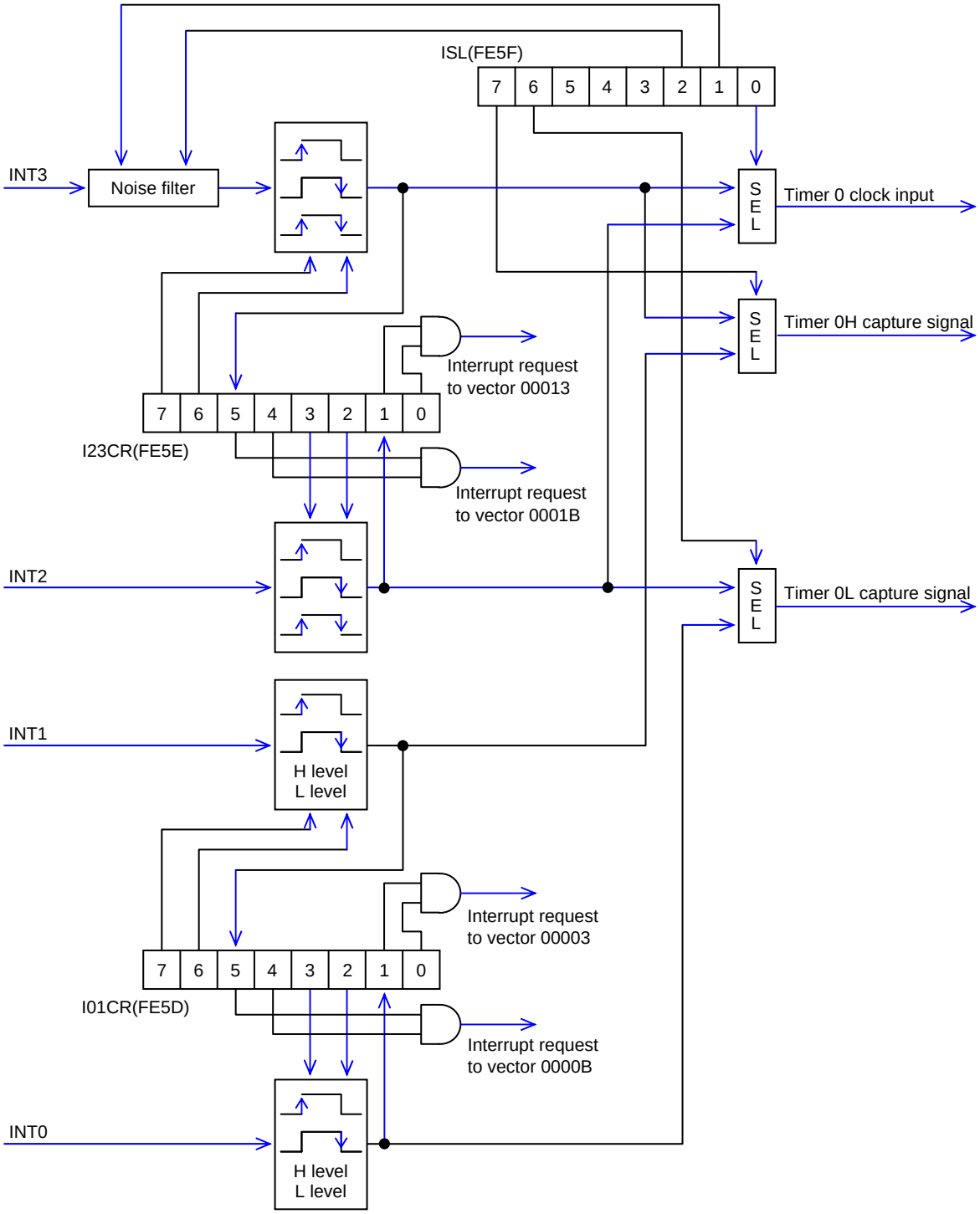


Port	Special Function Input	Function Output
P70	INT0/Timer 0L capture/AD analog 8 input	None

Table of Port 7 multiplexed pin functions

Port 7 Block Diagram
Option: None

Port Block Diagram



Port 1, Port 7 (Interrupt) Block Diagram

Important Note

This document is designed to provide the reader with accurate information in easily understandable form regarding the device features and the correct device implementation procedures.
The sample configurations included in the various descriptions are intended for reference only and should not be directly incorporated in user product configurations.
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LC872R00 SERIES USER'S MANUAL

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ON Semiconductor

Digital Solution Division

Microcontroller & Flash Business Unit