AX5043 ERRATA

Errata
Silicon Errata for AX5043

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ON Semiconductor®

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Introduction

This document lists silicon erratas, as well as features of the AX5043 that may be unexpected to the user.

The issues listed in this document are for the silicon revisions listed in the table below.

Table 1.

Revision	REVISION Register
V1	0x51

Issues

Radio Controller may not Properly Release FIFO Read or Write Port

When the AX5043 is directly switched from receive to transmit without powering down, the radio controller may under some circumstances not properly release the FIFO write port, thereby preventing SPI writes to the FIFO. When switching from transmit to receive without powering down, the radio controller may under some circumstances not properly release the FIFO read port, thereby preventing SPI reads from the FIFO.

Workaround: Write a second time a different value to the PWRMODE register. For example, when changing from receive to transmit mode, do the following:

1. Write 0x05 to PWRMODE to turn off the receiver
2. Write 0x07 to PWRMODE to release FIFO ports and to make sure the FIFO is enabled
3. Fill FIFO
4. Write 0x0D to PWRMODE to start transmission

Affected Revisions: V1

Zero Length Payload Packets with Hardware Address Matching and CRC

Packets where the hardware matched address is immediately followed by the hardware checked CRC are dropped, even if the CRC is correct.

Workarounds:

1. The transmitter may insert a padding byte between address and CRC
2. Shorten the AX5043 hardware matched address by one byte, and check the last byte in software
3. Check the CRC in software

Affected Revisions: V1

Gaussian Frequency Shift Keying (GFSK)

GFSK works as expected between AX5043 devices with both settings (BT = 0.3 and BT = 0.5). Both settings comply with transmission regulations. However, the AX5043 uses a slightly different shaping function than many non−ON Semiconductor chips, that may cause these chips to have difficulties receiving AX5043 transmissions. In this case, it is recommended to use the BT = 0.3 setting for the AX5043 and a BT = 0.5 setting for the non−ON Semiconductor chip.

Affected Revisions: V1

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