

ON Semiconductor

Is Now

onsemi™

To learn more about onsemi™, please visit our website at
www.onsemi.com

onsemi and **onsemi** and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

CAT28C17A

16 kb CMOS Parallel EEPROM

Description

The CAT28C17A is a fast, low power, 5 V-only CMOS Parallel EEPROM organized as 2K x 8-bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. \overline{DATA} Polling and a $\overline{RDY}/\overline{BSY}$ pin signal the start and end of the self-timed write cycle. Additionally, the CAT28C17A features hardware write protection.

The CAT28C17A is manufactured using ON Semiconductor's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 28-pin DIP and SOIC or 32-pin PLCC packages.

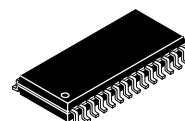
Features

- Fast Read Access Times: 200 ns
- Low Power CMOS Dissipation:
 - Active: 25 mA Max.
 - Standby: 100 μ A Max.
- Simple Write Operation:
 - On-chip Address and Data Latches
 - Self-timed Write Cycle with Auto-clear
- Fast Write Cycle Time: 10 ms Max
- End of Write Detection:
 - \overline{DATA} Polling
 - $\overline{RDY}/\overline{BSY}$ Pin
- Hardware Write Protection
- CMOS and TTL Compatible I/O
- 10,000 Program/Erase Cycles
- 10 Year Data Retention
- Commercial, Industrial and Automotive Temperature Ranges

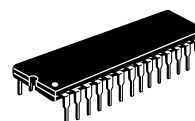


ON Semiconductor®

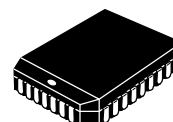
<http://onsemi.com>



SOIC-28
J, K, W, X SUFFIX
CASE 751BM



PDIP-28
P, L SUFFIX
CASE 646AE



PLCC-32
N, G SUFFIX
CASE 776AK

PIN FUNCTION

Pin Name	Function
A_0 - A_{10}	Address Inputs
I/O_0 - I/O_7	Data Inputs/Outputs
$\overline{RDY}/\overline{BUSY}$	Ready/ \overline{BUSY} Status
\overline{CE}	Chip Enable
\overline{OE}	Output Enable
\overline{WE}	Write Enable
V_{CC}	5 V Supply
V_{SS}	Ground
NC	No Connect

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

CAT28C17A

PIN CONFIGURATION

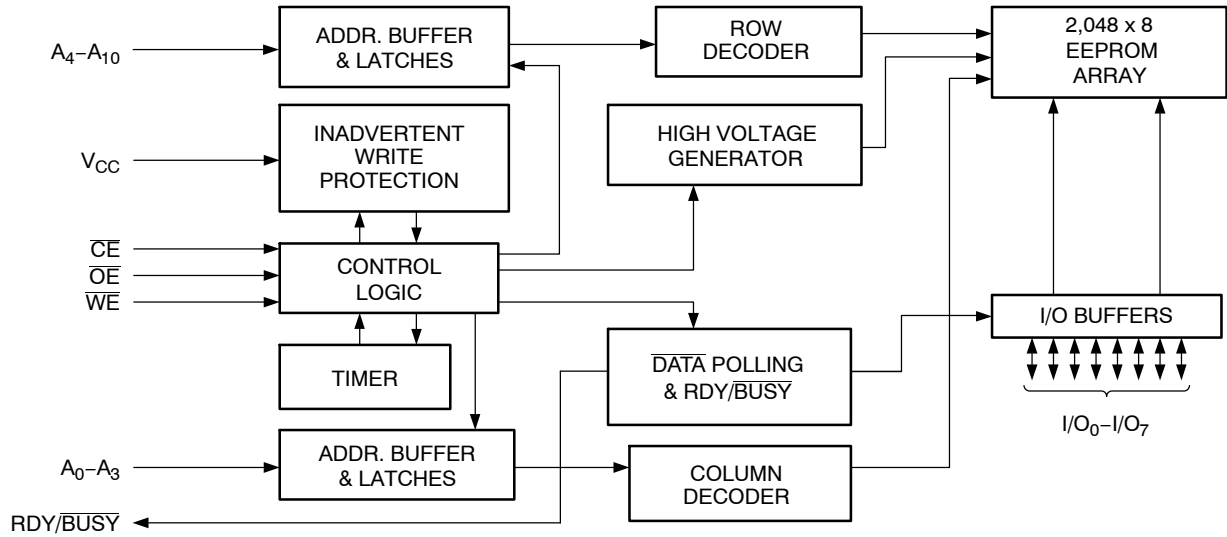
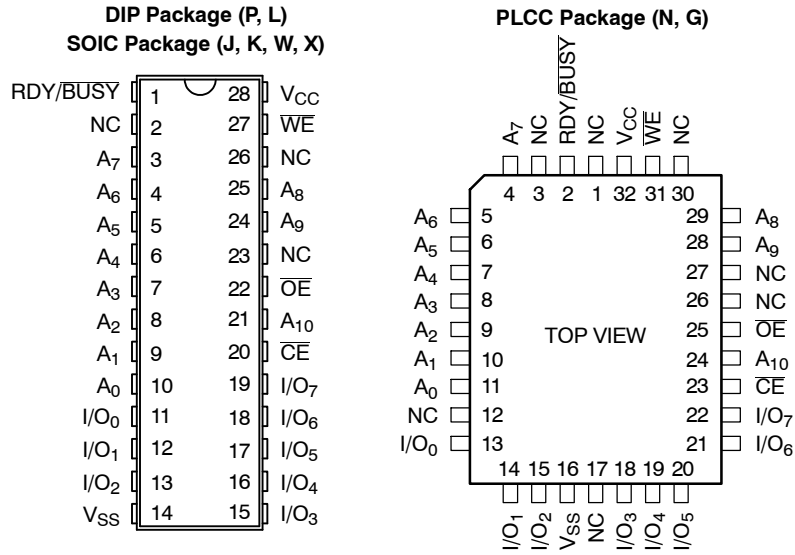


Figure 1. Block Diagram

CAT28C17A

Table 1. MODE SELECTION



Mode	CE	WE	OE	I/O	Power
Read	L	H	L	D _{OUT}	ACTIVE
Byte Write (\overline{WE} Controlled)	L		H	D _{IN}	ACTIVE
Byte Write (\overline{CE} Controlled)		L	H	D _{IN}	ACTIVE
Standby and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

Table 2. CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$, $V_{CC} = 5\text{ V}$)

Symbol	Test	Max	Conditions	Units
C _{I/O} (Note 1)	Input/Output Capacitance	10	V _{I/O} = 0 V	pF
C _{IN} (Note 1)	Input Capacitance	6	V _{IN} = 0 V	pF

1. This parameter is tested initially and after a design or process change that affects the parameter.

Table 3. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Temperature Under Bias	-55 to +125	°C
Storage Temperature	-65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 2)	-2.0 V to +V _{CC} + 2.0 V	V
V _{CC} with Respect to Ground	-2.0 to +7.0	V
Package Power Dissipation Capability ($T_A = 25^\circ\text{C}$)	1.0	W
Lead Soldering Temperature (10 secs)	300	°C
Output Short Circuit Current (Note 3)	100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- The minimum DC input voltage is -0.5 V. During transitions, inputs may undershoot to -2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods of less than 20 ns.
- Output shorted for no more than one second. No more than one output shorted at a time.

CAT28C17A

Table 4. RELIABILITY CHARACTERISTICS (Note 4)

Symbol	Parameter	Test Method	Min	Max	Units
N_{END}	Endurance	MIL-STD-883, Test Method 1033	10,000		Cycles/Byte
T_{DR}	Data Retention	MIL-STD-883, Test Method 1008	10		Years
V_{ZAP}	ESD Susceptibility	MIL-STD-883, Test Method 3015	2,000		V
I_{LTH} (Note 5)	Latch-Up	JEDEC Standard 17	100		mA

4. This parameter is tested initially and after a design or process change that affects the parameter.
 5. Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1 V to $V_{CC} + 1$ V.

Table 5. D.C. OPERATING CHARACTERISTICS ($V_{CC} = 5$ V $\pm 10\%$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
I_{CC}	V_{CC} Current (Operating, TTL)	$\overline{CE} = \overline{OE} = V_{IL}$, $f = 1/t_{RC}$ min, All I/O's Open			35	mA
I_{CCC} (Note 6)	V_{CC} Current (Operating, CMOS)	$\overline{CE} = \overline{OE} = V_{ILC}$, $f = 1/t_{RC}$ min, All I/O's Open			25	mA
I_{SB}	V_{CC} Current (Standby, TTL)	$\overline{CE} = V_{IH}$, All I/O's Open			1	mA
I_{SBC} (Note 7)	V_{CC} Current (Standby, CMOS)	$\overline{CE} = V_{IHC}$, All I/O's Open			100	μ A
I_{LI}	Input Leakage Current	$V_{IN} = GND$ to V_{CC}	-10		10	μ A
I_{LO}	Output Leakage Current	$V_{OUT} = GND$ to V_{CC} , $\overline{CE} = V_{IH}$	-10		10	μ A
V_{IH} (Note 7)	High Level Input Voltage		2		$V_{CC} + 0.3$	V
V_{IL} (Note 6)	Low Level Input Voltage		-0.3		0.8	V
V_{OH}	High Level Output Voltage	$I_{OH} = -400$ μ A	2.4			V
V_{OL}	Low Level Output Voltage	$I_{OL} = 2.1$ mA			0.4	V
V_{WI}	Write Inhibit Voltage		3.0			V

6. $V_{ILC} = -0.3$ V to $+0.3$ V
 7. $V_{IHC} = V_{CC} - 0.3$ V to $V_{CC} + 0.3$ V

Table 6. A.C. CHARACTERISTICS, READ CYCLE ($V_{CC} = 5$ V $\pm 10\%$, unless otherwise specified.)

Symbol	Parameter	28C17A-20		Units
		Min	Max	
t_{RC}	Read Cycle Time	200		ns
t_{CE}	\overline{CE} Access Time		200	ns
t_{AA}	Address Access Time		200	ns
t_{OE}	\overline{OE} Access Time		80	ns
t_{LZ} (Note 8)	\overline{CE} Low to Active Output	0		ns
t_{OLZ} (Note 8)	\overline{OE} Low to Active Output	0		ns
t_{HZ} (Notes 8, 9)	\overline{CE} High to High-Z Output		55	ns
t_{OHZ} (Notes 8, 9)	\overline{OE} High to High-Z Output		55	ns
t_{OH} (Note 8)	Output Hold from Address Change	0		ns

8. This parameter is tested initially and after a design or process change that affects the parameter.
 9. Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.

CAT28C17A

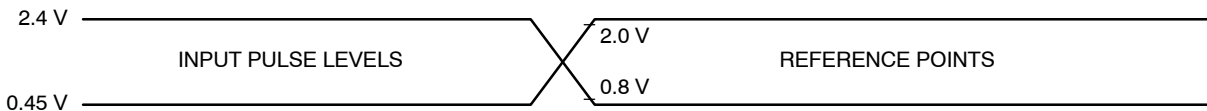
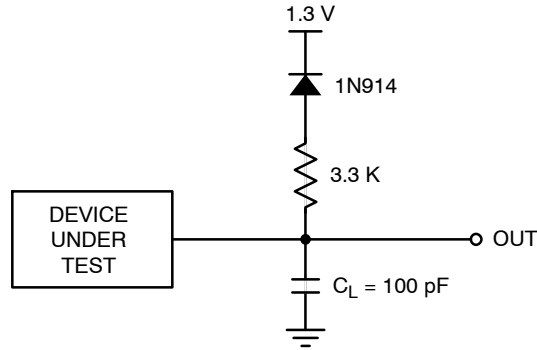


Figure 2. A.C. Testing Input/Output Waveform (Note 10)

10. Input rise and fall times (10% and 90%) < 10 ns.



C_L INCLUDES JIG CAPACITANCE

Figure 3. A.C. Testing Load Circuit (example)

Table 7. A.C. CHARACTERISTICS, WRITE CYCLE ($V_{CC} = 5 V \pm 10\%$, unless otherwise specified.)

Symbol	Parameter	28C17A-20		Units
		Min	Max	
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	10		ns
t_{AH}	Address Hold Time	100		ns
t_{CS}	\overline{CE} Setup Time	0		ns
t_{CH}	\overline{CE} Hold Time	0		ns
t_{CW} (Note 11)	\overline{CE} Pulse Time	150		ns
t_{OES}	\overline{OE} Setup Time	15		ns
t_{OEH}	\overline{OE} Hold Time	15		ns
t_{WP} (Note 11)	\overline{WE} Pulse Width	150		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{DL}	Data Latch Time	50		ns
t_{INIT} (Note 12)	Write Inhibit Period After Power-up	5	20	ms
t_{DB}	Time to Device Busy		80	ns

11. A write pulse of less than 20 ns duration will not initiate a write cycle.

12. This parameter is tested initially and after a design or process change that affects the parameter.

CAT28C17A

DEVICE OPERATION

Read

Data stored in the CAT28C17A is transferred to the data bus when \overline{WE} is held high, and both \overline{OE} and \overline{CE} are held low. The data bus is set to a high impedance state when either \overline{CE} or \overline{OE} goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Ready/ \overline{BUSY} (RDY/ \overline{BUSY})

The RDY/ \overline{BUSY} pin is an open drain output which indicates device status during programming. It is pulled low during the write cycle and released at the end of programming. Several devices may be OR-tied to the same RDY/ \overline{BUSY} line.

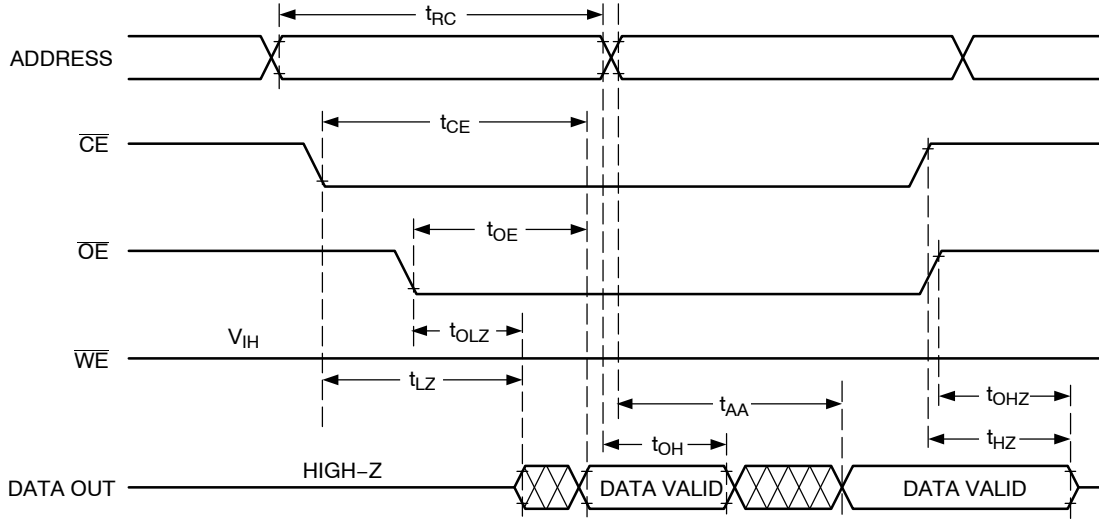


Figure 4. Read Cycle

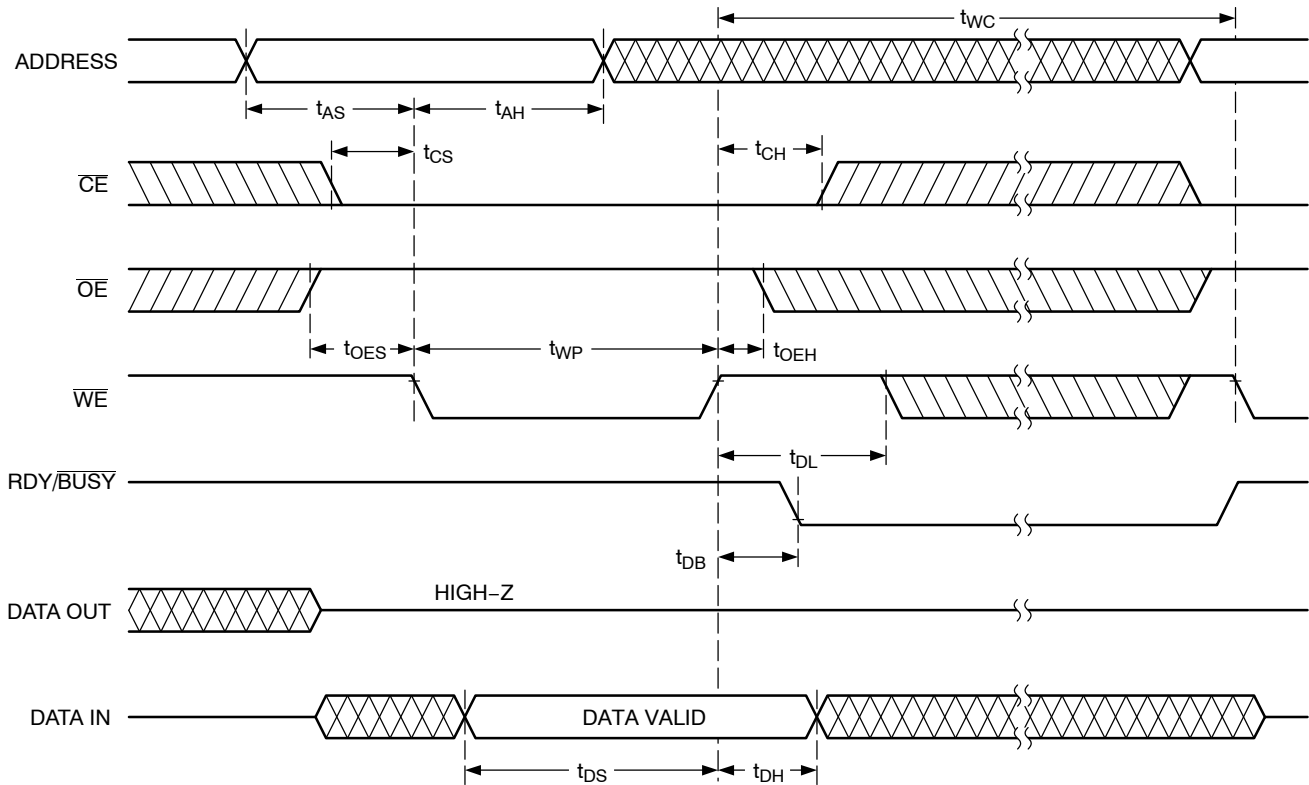


Figure 5. Byte Write Cycle [\overline{WE} Controlled]

CAT28C17A

Byte Write

A write cycle is executed when both \overline{CE} and \overline{WE} are low, and \overline{OE} is high. Write cycles can be initiated using either \overline{WE} or \overline{CE} , with the address input being latched on the falling edge of \overline{WE} or \overline{CE} , whichever occurs last. Data, conversely, is latched on the rising edge of \overline{WE} or \overline{CE} , whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 10 ms.

DATA Polling

\overline{DATA} polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O₇ (I/O₀–I/O₆ are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle, all I/O's will output true data during a read cycle.

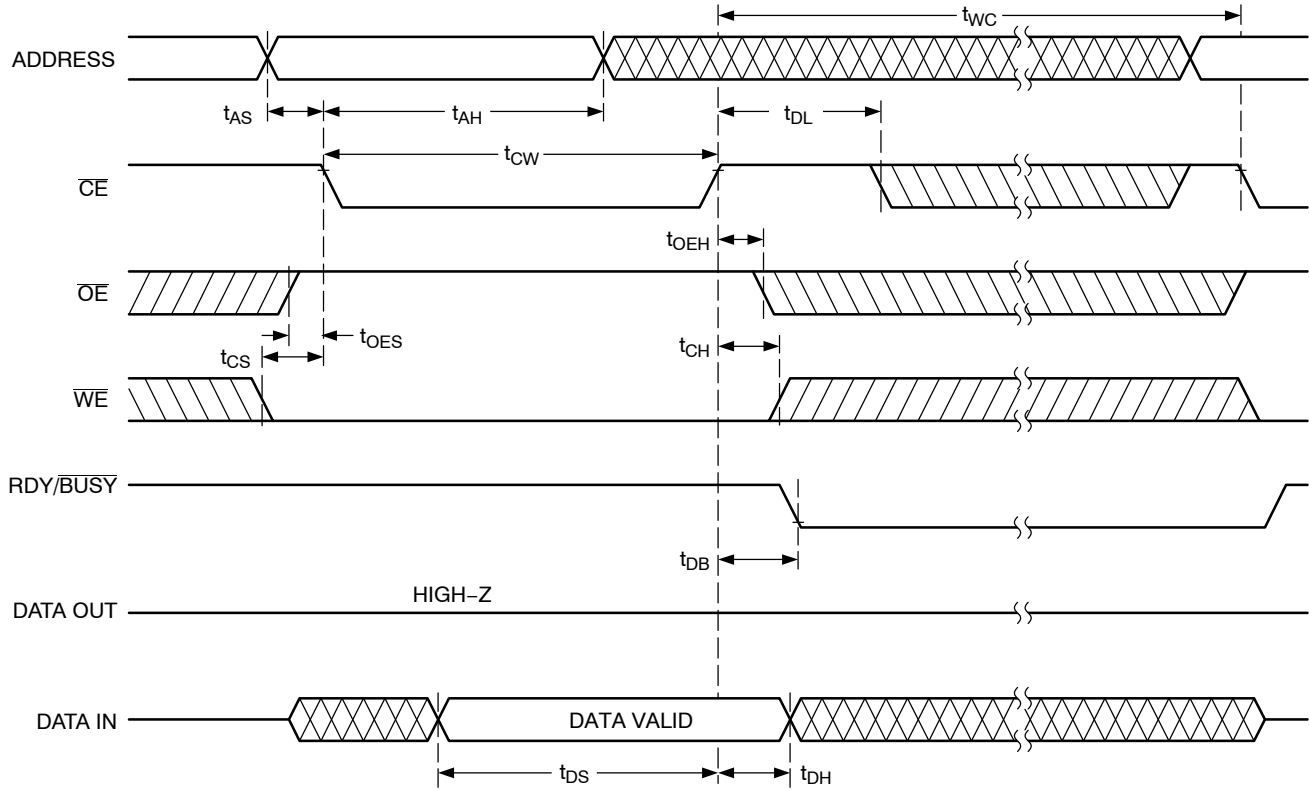


Figure 6. Byte Write Cycle [\overline{CE} Controlled]

CAT28C17A

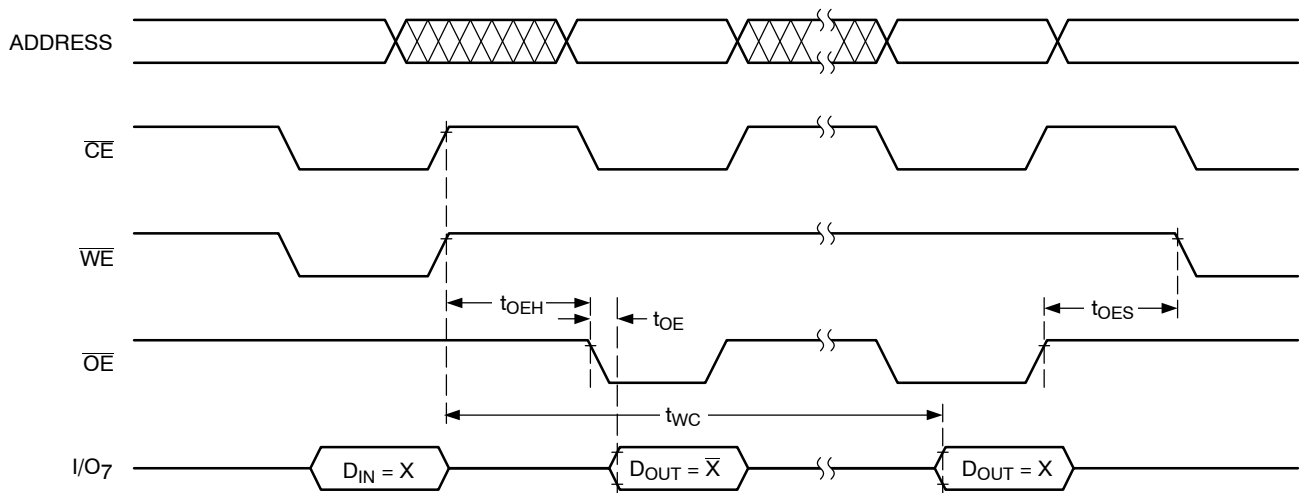


Figure 7. \overline{DATA} Polling

Hardware Data Protection

The following is a list of hardware data protection features that are incorporated into the CAT28C17A.

1. V_{CC} sense provides for write protection when V_{CC} falls below 3.0 V min.
2. A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 20 ms delay before

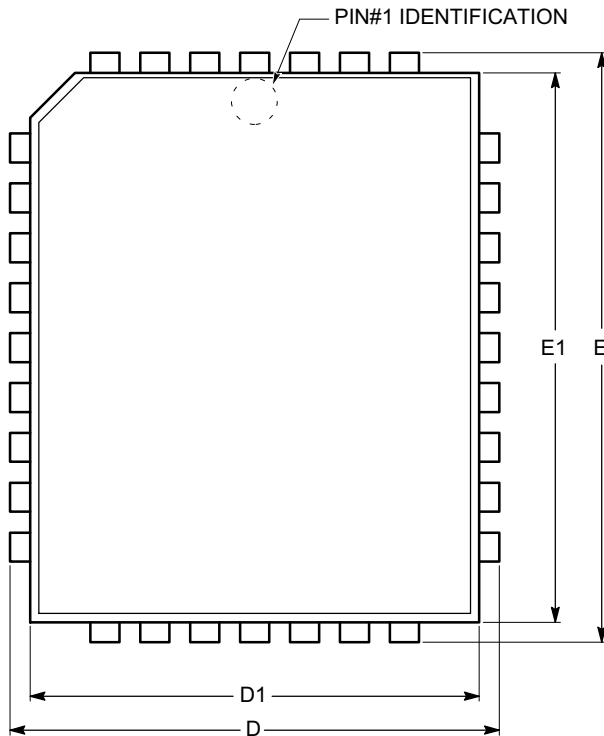
a write sequence, after V_{CC} has reached 3.0 V min.

3. Write inhibit is activated by holding any one of \overline{OE} low, \overline{CE} high or \overline{WE} high.
4. Noise pulses of less than 20 ns on the \overline{WE} or \overline{CE} inputs will not result in a write cycle.

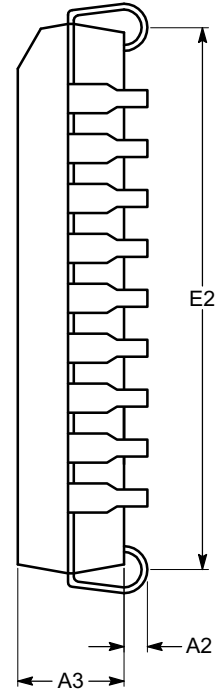
CAT28C17A

PACKAGE DIMENSIONS

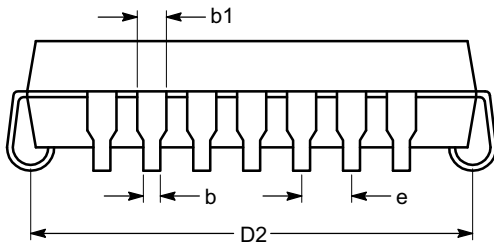
PLCC 32
CASE 776AK-01
ISSUE O



TOP VIEW



END VIEW



SIDE VIEW

Notes:

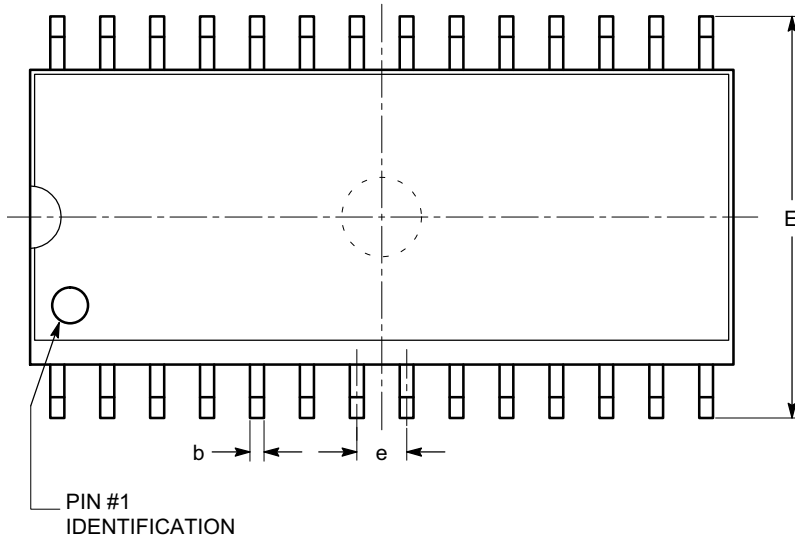
- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MS-016.

SYMBOL	MIN	NOM	MAX
A2	0.38		
A3	2.54		2.80
b	0.33		0.54
b1	0.66		0.82
D	12.32		12.57
D1	11.36		11.50
D2	9.56		11.32
E	14.86		15.11
E1	13.90		14.04
E2	12.10		13.86
e	1.27 BSC		

CAT28C17A

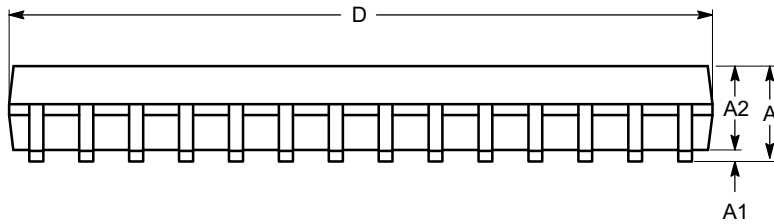
PACKAGE DIMENSIONS

SOIC-28, 300 mils
CASE 751BM-01
ISSUE O

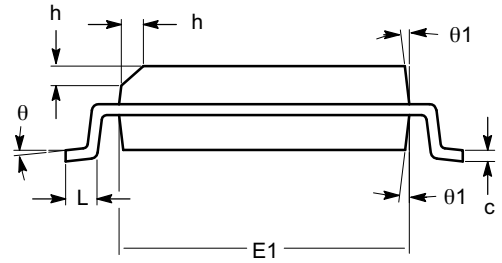


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.35		2.65
A1	0.10		0.30
A2	2.05		2.55
b	0.31		0.51
c	0.20		0.33
D	17.78		18.03
E	10.11		10.51
E1	7.34		7.60
e	1.27 BSC		
h	0.25		0.75
L	0.40		1.27
θ	0°		8°
$\theta 1$	5°		15°



SIDE VIEW



END VIEW

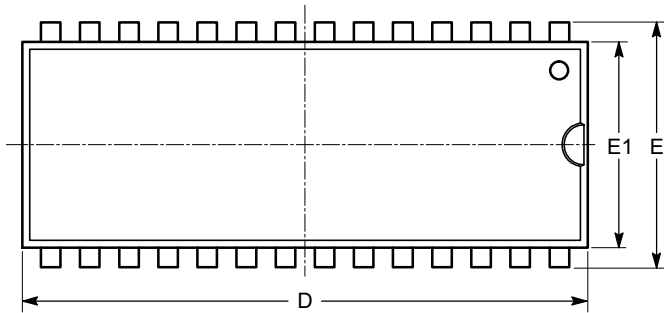
Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-013.

CAT28C17A

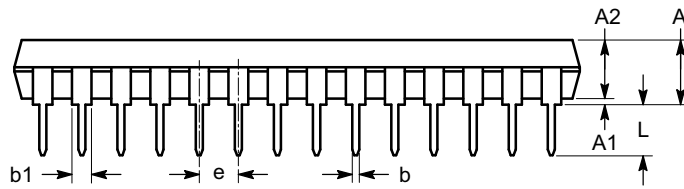
PACKAGE DIMENSIONS

PDIP-28, 600 mils
CASE 646AE-01
ISSUE A

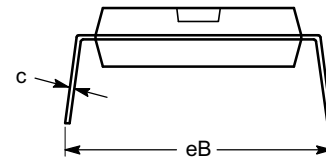


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			6.35
A1	0.39		
A2	3.18		4.95
b	0.36		0.55
b1	0.77		1.77
c	0.21		0.38
D	35.10		39.70
E	15.24		15.87
E1	12.32		14.73
e	2.54 BSC		
eB	15.24		17.78
L	2.93		5.08



SIDE VIEW



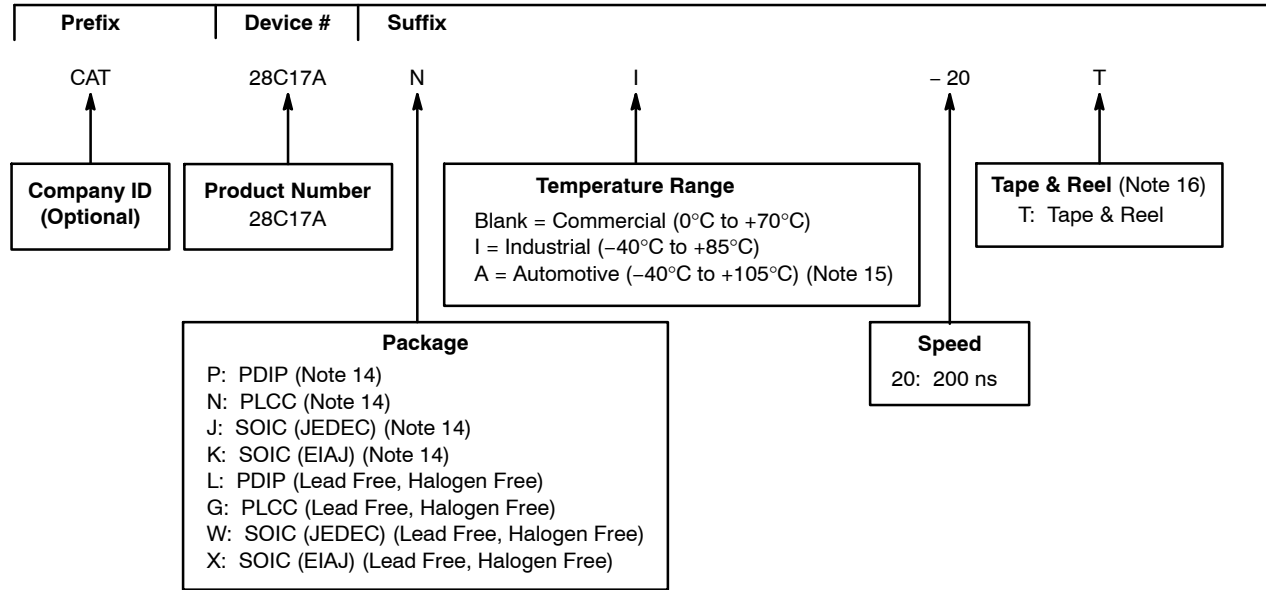
END VIEW

Notes:

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MS-011.

CAT28C17A

Example of Ordering Information



13. The device used in the above example is a CAT28C17ANI-20T (PLCC, Industrial Temperature, 200 ns Access Time, Tape & Reel).

14. Solder-plate (tin-lead) packages, contact Factory for availability.

15. -40°C to +125°C is available upon request.

16. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ON Semiconductor and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
 P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
 USA/Canada
Europe, Middle East and Africa Technical Support:
 Phone: 421 33 790 2910
Japan Customer Focus Center
 Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative