ON Semiconductor

Is Now

To learn more about onsemi™, please visit our website at www.onsemi.com

CS51031DEMO1/D

Demonstration Note for CS51031 (5 A)

A 5 V to 3.3 V/5 A DC/DC Buck Regulator Converter Using the CS51031 Switching Controller

ON Semiconductor®

http://onsemi.com

DEMONSTRATION NOTE

Description

The CS51031 Demonstration Board is a 5 V–in, 3.3 V–out DC/DC converter that delivers 5 A. It monitors Vcc and output voltage ripple to control the PWM. The 1.0 A power driver assures quick, efficient switching of the gate of a discrete P–channel FET. Utilizing buck topology, this demonstration board delivers excellent performance and protection and represents an extremely low cost solution. The CS51031 DC/DC buck converter responds to current transients in a very short period of time, providing a constant output voltage. The CS51031 provides hiccup mode short–circuit protection, eliminating the expense of a current sense resistor. The components and layout on the CS51031 demo board have been optimized to deliver performance and price in the hands of every motherboard manufacturer. The surface mount components and PCB layout on the CS51031 demo board have been optimized to deliver maximum performance in the minimum footprint. The board is two–layer, 2″ × 3″ PCB with the DC/DC converter area being 1.25″ × 1″.

Features

- Provides 5 Amps of Output Current
- Low External Component Count
- Provides > 85% Efficiency Across Wide Load Range
- 3% DC regulation, 5% AC regulation
- 1 ms Soft Start Ramps Power Up for Lower System Noise and Component Stress
- Single P–Channel MOSFET Design
- 5 V Supply Input with 4.25 V UVL
- 625 kHz Switching Frequency Allows Compact, Low Loss Magnetics
- All Surface Mount Components

Figure 1. CS51031 Demonstration Board

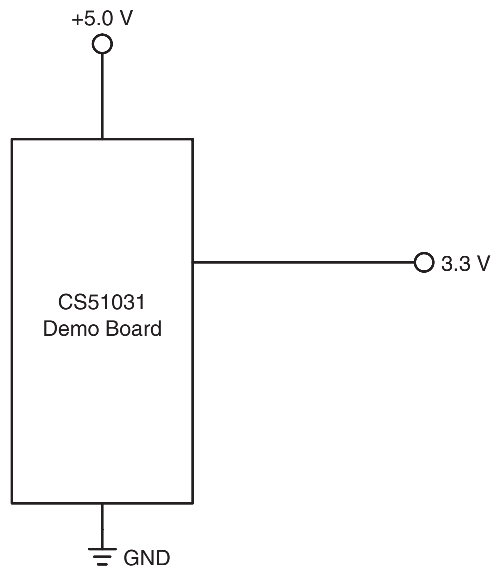


Figure 2. Application Diagram

MAXIMUM RATINGS

Pin Name	Maximum Voltage	Maximum Current
+5 V	+20 V/–0.3 V	4.0 Amp DC
3.3	+5.0 V/–0.3 V	5.0 Amp DC
GND	0 V	5.0 Amp DC

ELECTRICAL CHARACTERISTICS (4.75 V < 5 V_{IN} < 5.25 V, Iout = 0 (No Load), unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
DC Output Voltage	0 < Iout < 5.0 A	3.201 –3.0	3.300 Vref	3.399 +3.0	Volts %
AC Voltage Regulation	2.5 A Load Step	3.135 –5.0	3.300 Vnom	3.465 +5.0	Volts %
Load Transient Response	Time required to settle to ±5% of Vout	–	10	20	µs
Ripple and Noise	0 < Iout < 5.0 A, 20 MHz BW	8.0	30	50	mVpp
Load Regulation (DC)	0 < Iout < 5.0 A	–	30	50	mV
Line Regulation	4.75 V < 5.0 Vin < 5.25 V, Iout = 5.0 A	–	2.0	10	mV
Switching Frequency	0 < Iout < 5.0 A	465	625	785	kHz
Duty Cycle (Positive)	Measure (TON/T) × 100 of Switching FET during load transient response 0 < Iout < 5.0 A	0	–	80	%
Efficiency P(Vout)/P(5 Vin)	Iout = 5.0 A Iout = 0.1 A	84 60	87 65	90 70	% %
+5 V Start Threshold	Switching	4.2	4.4	4.6	V
+5 V Stop Threshold	Not switching	4.065	4.300	4.515	V
Hysteresis	Start – Stop	65	130	200	mV
Power–Up/Soft Start Time	0 < Iout < 5.0 A	0.5	1.0	3.0	ms

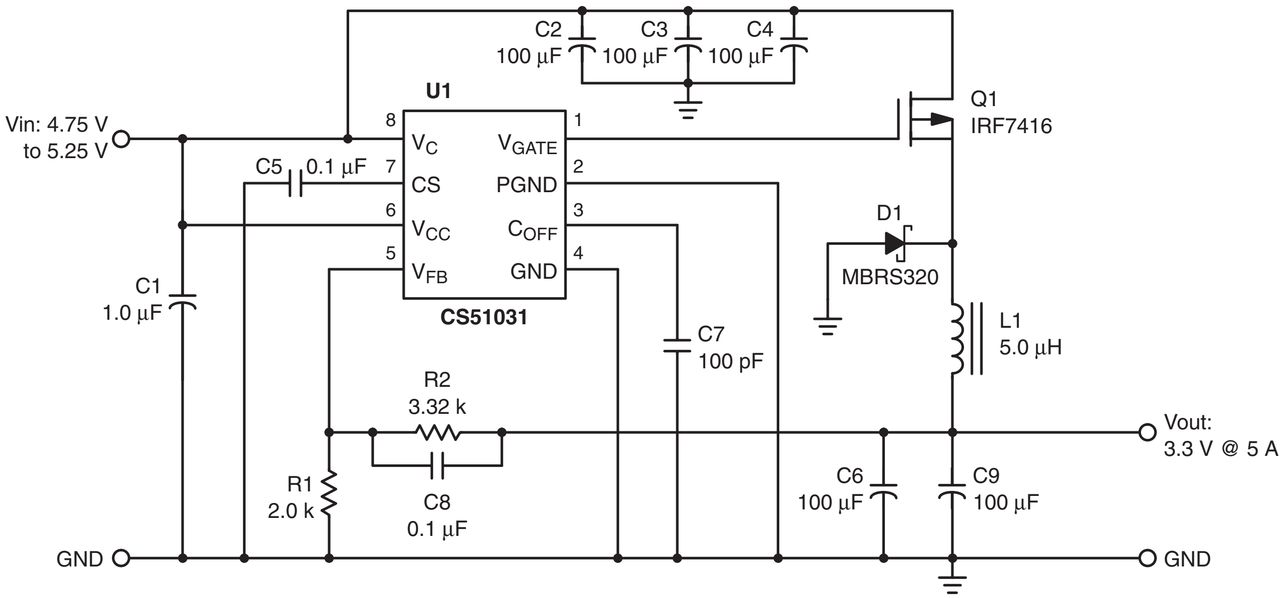


Figure 3. Demonstration Board Schematic

OPERATION GUIDELINES

The CS51031 Demonstration Board is configured to exhibit all the unique performance features of the CS51031 Buck Controller IC. The +5 V input terminal is located on the left side of the board, and simple alligator, or banana clip connections are needed to power up the demo board. The output terminals are located right next to the load resistors, and simple alligator, or banana clip connections are required to monitor the output voltage.

THEORY OF OPERATION

Control Method

In this demonstration board, the output is controlled by the CS51031, which drives a PFET to step the input voltage down to the desired level. This output is generated using a nonsynchronous buck topology that utilizes a constant frequency. The CS51031 regulates the 3.3 V output by adjusting the duty cycle of the switch to maintain regulation. A special digital control scheme eliminates the need for a traditional feedback loop with internal error amplifier. This significantly simplifies the design and operation of the power solution by removing the complex analysis and design in compensating the feedback loop. The conversion efficiency for the power solution will not be as high as a fully synchronous design. A nonsynchronous converter will typically have efficiencies in the mid 80% range. Replacing the Schottky diode with a synchronous FET will increase the converter efficiency by 3% to 7%. Efficiency gains are significant as the output voltage becomes lower and the diode is on for a longer duration each cycle.

Startup

The CS51031 has an externally programmable soft start feature that controls the rate of output voltage increase upon initial power up as well as following fault conditions. This prevents voltage overshoot at the output, which in turn protects devices connected to Vout. The soft start capacitor, Css, along with soft start charge current, Ics, sets the rate of voltage rise. With the Css value of 0.1 μF, the soft start time is approximately 1 ms.

Fault Operation

When the demonstration board output Vout is shorted to ground, and the CS51031 is placed in hiccup mode, whereby gate pulses are delivered to the PFET as the soft start capacitor charges, and cease while it discharges. The typical charge time is 3 ms, while the discharge lasts for 90 ms typically. If the short–circuit condition persists, the regulator output will not achieve the 1 V low Vfb comparator threshold before the soft start capacitor is charged to its upper 2.5 V threshold. Then the cycle will repeat itself until the short is removed. If the short–circuit condition is removed, the output voltage will rise above the 1 V threshold, preventing the FAULT latch from being set, and allowing normal operation to resume.

The CS51031 implements short circuit protection by means of a lossless short circuit protection scheme. In this scheme, the short circuit comparator senses the output voltage and initiates hiccup operation when this voltage decreases below a pre–set threshold, due to the short circuit condition.

DESIGN GUIDELINES

Component Selection

Magnetics: This design uses only one inductor. This provides a 'low–pass filter' to the output switching ripple, to turn the AC to DC. The designer must be very aware of maximum current expected across the inductor. Switching frequency must also be considered in the core selection. Simple ferrite toroids, such as supplied by Koolµ and Micrometals can withstand the 100 k–1 MHz frequencies selected. The number of turns to use is an exercise in tradeoff between output voltage ripple levels and response time to load transients. An additional inductor may be inserted at the Vin connection to quiet the input current spikes seen by the supply sourcing Vin.

Input and Output Bulk Capacitors: Input caps must provide the maximum ripple current of the switched input current. This can be initially estimated as one–half of the output current. Output caps control the output ripple voltage. This voltage is simply the inductor's ripple current, multiplied by the ESR of the capacitors. Favorite tricks for ESR reduction are paralleling several caps and, if budget allows, lower ESR tantalums are available from TDK and AVX.

Semiconductors: The switching FET selection is primarily based upon maximum voltage and current ratings. Also to be considered is the R_{DSon}. This determines the power burned in the FET and must be removed. Too little copper on the PC board to wick out this heat is a common cause of failure. In higher power convertors, heat sinks may be considered to keep the footprint down. The Schottky diode must also be selected by maximum current rating and voltage levels present. In this design, the continuous max is 7 A with peaks of 10 A. Average current is approximately (Vout/Vin) · Imax, so typically (3.3 V/5 V) · 7A = 2.3 A, so a 20 V, 5 A Schottky is a good choice.

Formulae

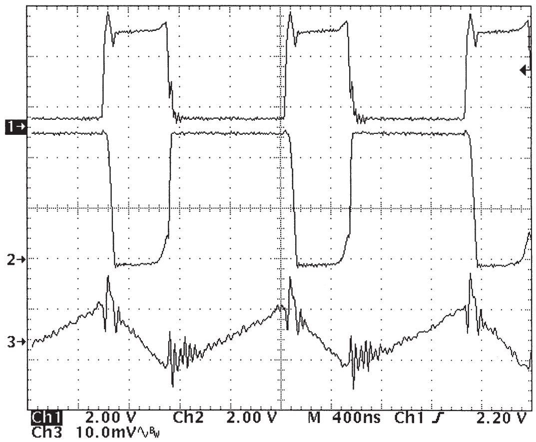
A few useful formulae for Buck architecture:

Duty Cycle: DTC = (Vout + Vdiode)/(Vin + Vdiode) = (3.3 + 0.5)/(5.0 + 0.5) = 69% (nominal)

Diode Current: Idiode = (1 – DTC) · $Iout_{max}$ = (1 – 0.69) · 7 A = 2.17 A (average max)

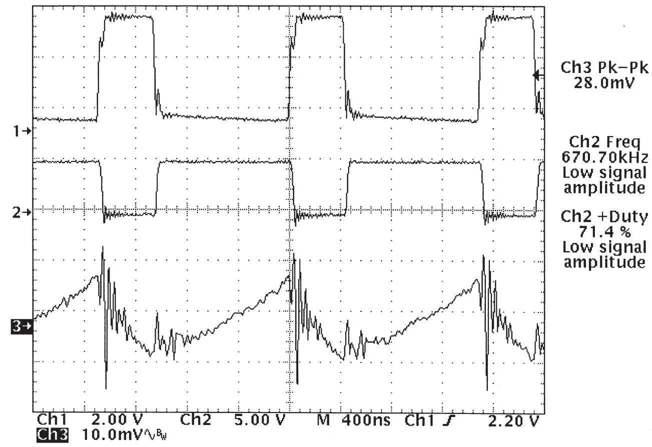
Power Loss: $P_{FET} = I^2 \cdot R_{DSon} \cdot DTC = 49 \cdot 0.025 \cdot 0.69$ = 845 mW

TYPICAL OSCILLOSCOPE WAVEFORMS



Trace 1 = FET Gate
Trace 2 = Inductor Switching Node
Trace 3 = Output Ripple Voltage

Figure 4. CS51031 Demonstration Board Voltage Waveforms During Normal Operation (Discontinuous Mode), Load Current = 100 mA

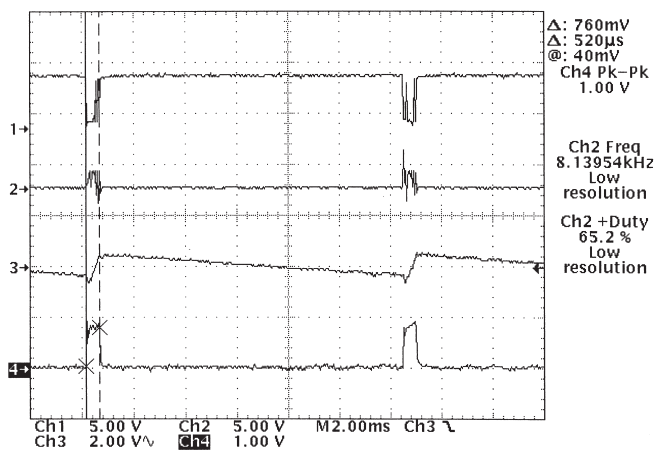


Trace 1 = FET Gate
Trace 2 = Inductor Switching Node
Trace 3 = Output Ripple Voltage

Figure 5. CS51031 Demonstration Board Voltage Waveforms During Normal Operation, Load Current = 2.5 A

Trace 1 = FET Gate
Trace 2 = Inductor Switching Node
Trace 3 = Output Ripple Voltage

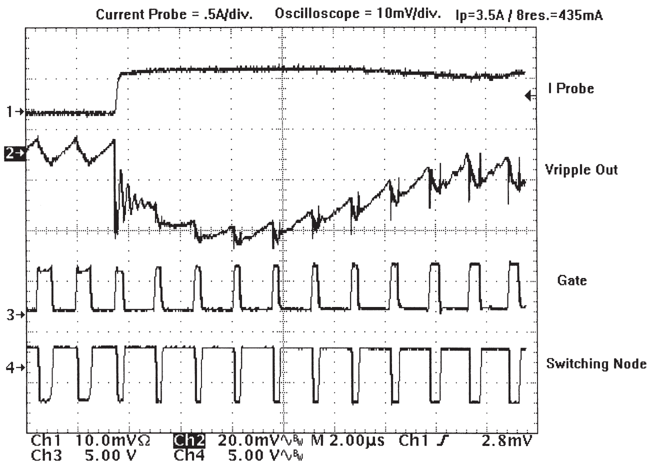
Figure 6. CS51031 Demonstration Board Voltages During Normal Operation, Load Current = 5.0 A



Trace 1 = FET Gate
Trace 2 = Inductor Switching Node
Trace 3 = Soft Start Pin (Pin 3)
Trace 4 = V_{OUT}

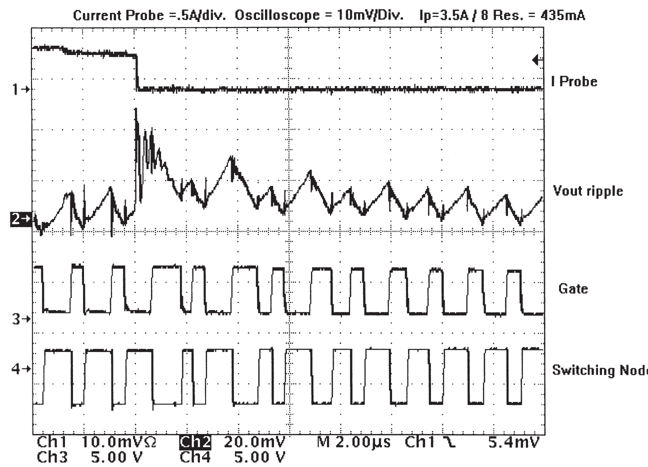
Figure 7. CS51031 Demonstration Board Voltage Waveforms During Hiccup Mode Short–Circuit Operation

TYPICAL OSCILLOSCOPE WAVEFORMS



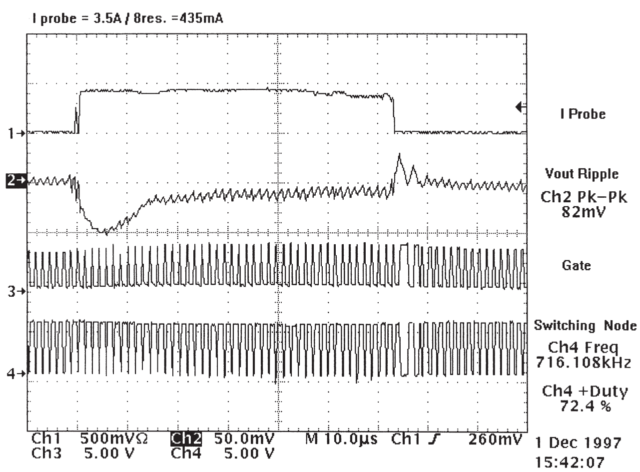
Trace 1 = Load Current 0.5 A/div.
Trace 2 = V_{OUT} Ripple
Trace 3 = FET Gate
Trace 4 = Inductor Switching Node

Figure 8. CS51031 Demonstration Board Voltage Waveforms During a 100 mA to 3.5 A Load Transient



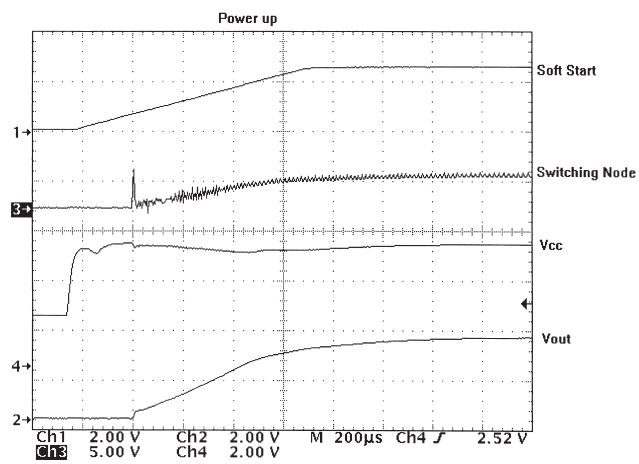
Trace 1 = Load Current 0.5 A/div.
Trace 2 = V_{OUT} Ripple
Trace 3 = FET Gate
Trace 4 = Inductor Switching Node

Figure 9. CS51031 Demonstration Board Voltage Waveforms During a 3.5 A Load to 100 mA



Trace 1 = Load Current = 500 mV
Trace 2 = V_{OUT} Ripple
Trace 3 = FET Gate
Trace 4 = Inductor Switching Node

Figure 10. CS51031 Demonstration Board Voltage Waveforms During a 3.5 A Load Transient



Trace 1 = Soft Start
Trace 2 = V_{OUT}
Trace 3 = Switching Node
Trace 4 = V_{IN}

Figure 11. CS51031 Demonstration Board Voltage Waveforms During Power Up

ELTEST (AUTOMATED POWER SUPPLY TEST SYSTEM) DATA

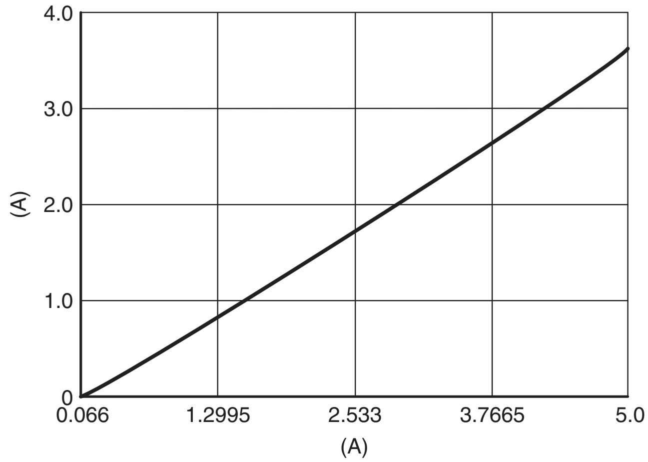


Figure 12. Input Current vs. Load, Vin = 5.0 V

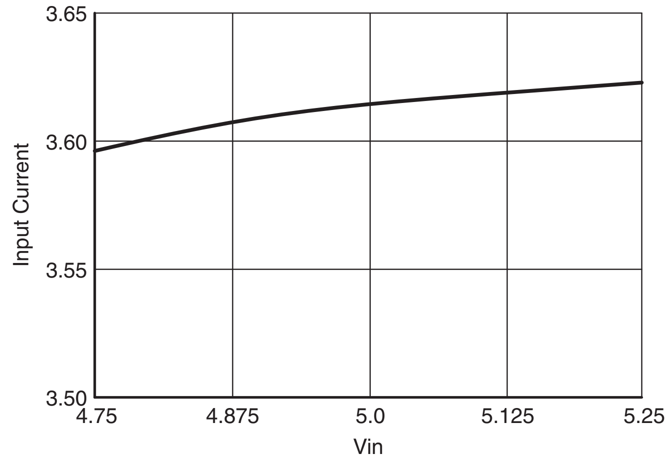


Figure 13. Input Current vs. Vin, Iout = 5.0 A

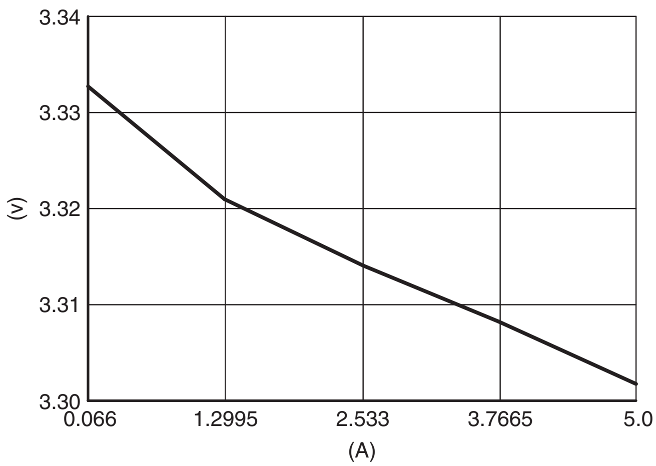


Figure 14. Load Regulation 0 < Iout > 5.0 A, Vin = 5.0 V

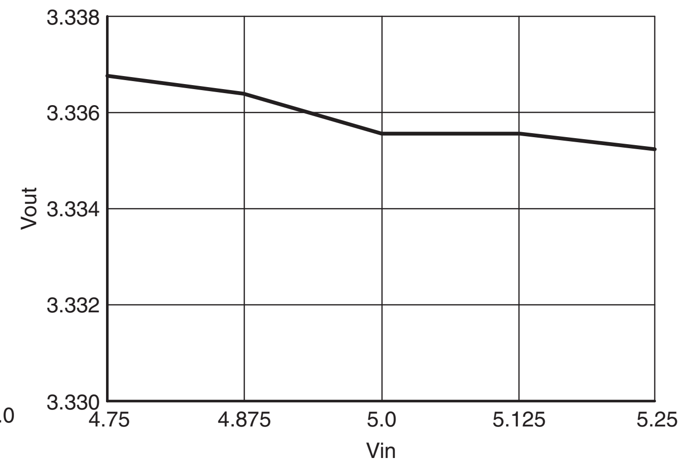


Figure 15. Line Regulation, Iout = 5.0 A

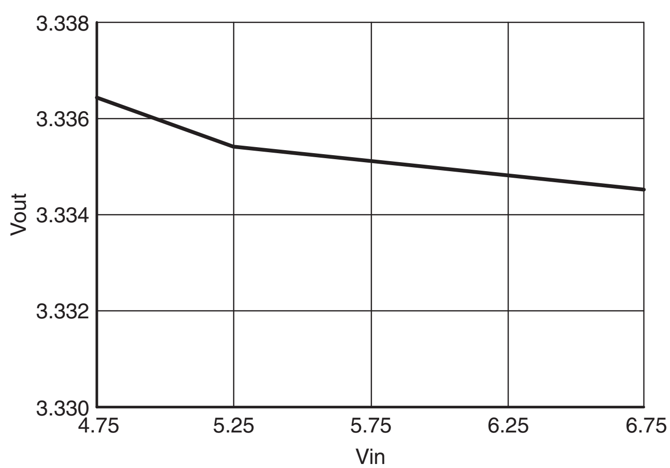


Figure 16. Line Overvoltage Test 4.75 V < +5.0 Vin < 6.75 V

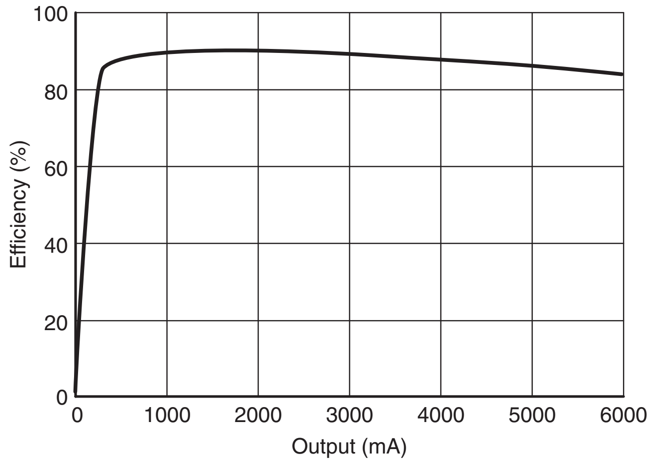


Figure 17. Percent Efficiency

BILL OF MATERIALS

Ref. Des	Qty	Description	Manufacturer	Manufacturer P/N	Telephone
C2–C4, C6, C9	5	100 μF/10 V Tantalum	KOA	TMC1AE–107MLRH	814–362–8883
C1	1	1.0 μF Cap. 1206	Novacap	1206Y105Z160N	805–295–5928
C5, C6	2	0.01 μF Cap. 0805	Novacap	0805B104M250N	805–295–5928
C7	1	100 pF Cap. 0805	Novacap	0805N101M500N	805–295–5928
R1	1	2.0 k, 1% Res. 0805	KOA	RK73H1JT2001F	814–362–8883
R2	1	3.32 k, 1% Res. 0805	KOA	RK73H1JT3321F	814–362–8883
L1	1	5.0 μH/5.0 A Smt Ind.	XFMRS	XF0056S4KM	317–834–1066
Q1	1	P–FET SO–8, 0.02 Ω	IR	IRF7416	310–322–2331
D1	1	Smt Schottky	Central	CMSH3–20	516–435–1824
U1	1	PFET Cont.	ON Semiconductor	CS51031	800–272–3601
J1–J4	4	Turret Terminals	Millmax	2501–1–00–44–00–00–07–0	–
PCB	1	Substrate	–	–	–

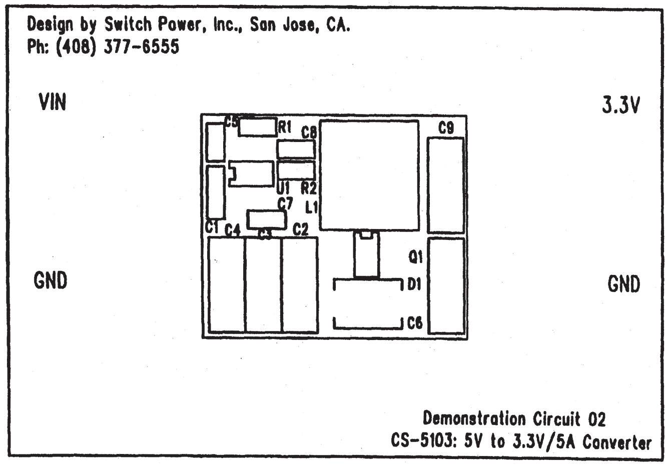


Figure 18. PC Board Layout

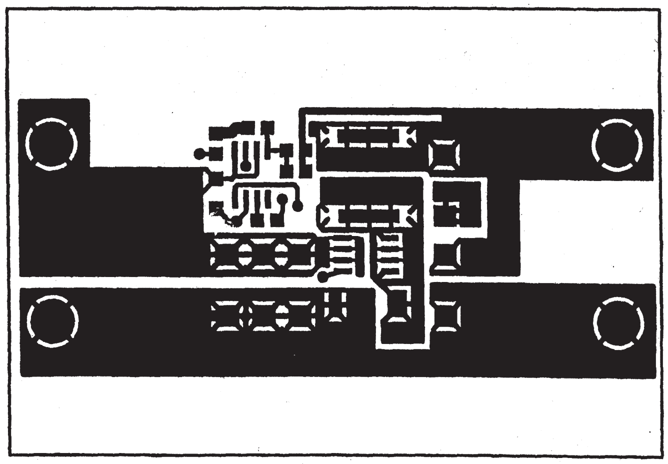


Figure 19. PC Board Component Side Copper

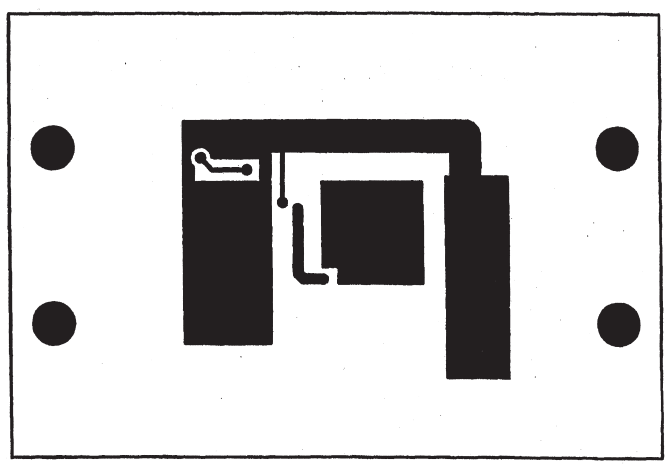


Figure 20. PC Board Solder Side Copper

Notes

Notes

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
Phone: 81–3–5740–2700
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local
Sales Representative.