DN05129/D

Design Note – DN05129/D

onsemi

Universal AC Input, 4 Watt Non-isolated Power Supply

Device	Application	Input Voltage	Output Power	Topology	I/O Isolation	
NCP10672BD060G	White Goods, E-meter, etc.	90 to 265 Vac	7.5 W @ 230 Vac 6.5 W @ 110 Vac	Buck	No	
			Output S			
	Output Vo	tage				
	Output Ri	pple	<90 mV @			
	Max Curr	ent	0			
	Min Curr	ent				
Efficiency			See E			
	Input Prote	ction				
Operating Temp. Range			0 to			
Cooling Method			Cor			
	No-load Power Co	onsumption	See No			

Circuit Description

This design note describes a simple 4 W, universal AC input, non-isolated buck converter. The key parameters of the power supply are dimensions and fast transient respond with given output filter. It is recommended to modify the power supply to fit individual needs, like standby consumption, output voltage ripple etc.

The power supply is a simple non-isolated buck topology utilizing **onsemi's** new NCP10672 monolithic switcher with integrated 12Ω MOSFET in a SOIC7 package (IC1). This Design Note provides the complete circuit schematic and BOM.

The AC voltage is rectified (D4, D5, D6, D8) and connected to bulk capacitor C4. The rising voltage allows DSS to charge Vcc capacitor C8. Once the voltage on C8 crosses UVLO level, the NCP10672 starts switching. When the internal MOSFET is on, the current flows from C4 to Drain pin, from GND pin through L2 into C3, then via negative line back to C4. When the MOSFET is turned off, the current flows from L2 to C3, then via D3 back to the coil. During demagnetization period, C1 is charged to output voltage level (through D2). The C1 value affects no load

consumption, transient response etc. The reason is, the capacitor can only be charged via D2, but discharging is done by FB resistor divider. Moreover, the charging is done only during demagnetization period of L2. If lower value of C1 is used, in skip mode, the C1 is discharged faster, so IC1 switches frequently to check the output value. On the other hand, choosing a bigger C1 value results in a longer switching period. As a result, the higher value of C1 decreases no load consumption and improves load regulation (see Figure 6 and Figure 7). The lower value of C1 decreases transient response time (see Figure 13 and Figure 14). The C1 value selection depends on designer's priorities. A resistor divider composed of R5, R6 and R3 reduces voltage for FB pin (3.3 V). The OVP protection and supplying the IC is done by R4 and D7 from the output voltage. Compensation network composes of R2, C2 and C7. The output diode D1 is a dummy load to clamp high output voltage in no load or low load conditions.

The output power can be boosted up to 7.5 W @ 230 V if C4 and C3 capacitances are increased. If such power is drawn from the demo without any update, the output ripple will rise.

- **Key Features** Universal AC input range (90 265 Vac). Small dimensions.

- Low no load consumption (it requires a device change)
 Over-voltage and over temperature protection.
 Frequency Jittering for Better EMI Signature (EMI not tested).



PCB layout



Demo-board Photo



Тор



Bottom

Principle description

For simplicity in schematic, current loops are colored:

Inductor current (loop A), FB current (loop B), IC supply current (loop C).

Step 1: The MOSFET (in IC1) is turned on:



Figure 1 MOSFET is turned on

Let's assume that the inductor L2 is fully demagnetized before MOSFET turn on, the converter has been running for a while, it is in steady state conditions and the output voltage is at target level.

The power MOSFET in IC1 is turned on, the current (loop A) starts to flow through the inductor and load, so an amount of energy charges C3 and part of the energy flows to the

load. The on time and peak current is assessed by the FB loop. The information of output voltage had been stored in C1 in previous cycle. The voltage from C1 is divided by R5, R6 and R3 and it is connected to FB pin. During MOSFET conductive phase, the output voltage is not connected to FB pin, so the on time is given by voltage stored on C1 (during previous cycle), not by the actual output voltage. The C1 capacitor is slowly discharged by FB divider (FB loop (B)). It is important to select C8 value (supply capacitor for IC1) in such a way that the C1 is not discharged by IC1 consumption. Otherwise, the stability will be affected by Vcc capacitor C8. Voltage between C4 minus terminal and IC1 GND pin is almost equal to C4 (input) voltage. The fact that the IC1 GND pin is at a high voltage prevents measuring any IC1's pin voltages with respect to IC GND pin using standard oscilloscope probe, which is usually connected to main grid PE terminal. Only differential probes or battery powered oscilloscope (off the main grid) provide relevant results.



Step 2: The MOSFET (in IC1) is turned off:

Figure 2 MOSFET is turned off

When the MOSFET is turned off, the inductor L2 will keep current flowing the same way, so the voltage on L2 is reversed and the inductor becomes the source of energy. There are several current loops, through which the current can/will flow. Which current loop will be closed first depends on several factors. If the output is at a light load or no load, the output voltage will be higher than desired by FB divider, so the current (loop A) will not start to flow to the output. We also want C8 to be discharged slower than C1, so the current (loop C) will not supply either IC1 or C8. In these light/no load conditions the current (loop B) will flow to C1 and FB divider first. Please notice the C1 is still not charged to the output voltage level (presented on C3), D3 is not conductive yet, because current (loop A) does not flow to the load. The next step depends on amount of energy stored in L2. If the energy is high enough to cover FB loop (B) and supply (loop C)

capacitor demand, then the current (loop A) will start to flow through D3, and C1 capacitor is properly charged to output voltage level (C3). The voltage on C1 will be used in next cycle as the value for on time and current peak settings. In case the energy in L2 is not high enough to push a current (loop A) through D3, then the voltage on C1 will not match the output one (C3). In such case, regulation voltage on C1 will be at target level, but output voltage will be higher than desired. It is important to have enough energy in L2 to open D3 diode (allow the current (loop A) flow through D3). It is recommended not to use too small FB divider resistors as the consumed energy by divider will be missing for closing current loop (A) through D3. In case this situation occurs, Zener diode D1 can save the situation, because it clamps the voltage below critical level. During this period IC GND pin voltage is by Vf of D3 diode drop higher, than the negative terminal of C4. If the drop on D3 is higher than Vf of D3 (see DS), then it can show that there is not enough energy in L2 to open current loop (A) and C3 voltage does not correspond to the one set by FB divider.

07 H <u>₀</u>2 IC1 VCC C1 FΒ COMP L1 05 TP3 DRAIN GND ₽ TP1 R2 D1 СЗ ₽ 🛣 оз C1 63 C7 厷 <u>⊢</u> | R2 R6 TD2 ВŤ C2 С

Step 3: No energy transfer to the output:

Figure 3 No energy transfer to the output

At the end of Step 2, all energy from L2 is consumed. The IC is supplied (loop C) from C8, capacitor C1 is discharged (loop B) by FB divider. The IC has no information about the real output voltage, so if a short or a step load causes voltage drop on the output, the converter will not react immediately. First, the C1 must be discharged (loop B) below FB reference level, which is done by FB divider and FB pin consumption (See DS). Then the IC clicks, which causes charging C1 capacitor to output voltage level (if the output voltage is higher than the one on C1). If the output voltage is too low, the energy transfer from input to output will start (the IC will start switching). If the output voltage is higher than desired, next switch will placed when C1 is discharged (loop B) below FB pin level. The description here shows, that the IC must switch to "check" output voltage even if the

output voltage is higher than desired. Every switching transfers an amount energy to the output, which causes output voltage increase at no/light load conditions. Too keep the output voltage at a safe level, Zener diode D1 is recommended, or the output load must be always high enough to not let the output voltage become too high. During this period, IC1 GND pin voltage is equal to the output voltage (measured with respect to negative terminal of C4).



Step 4: IC1 supply for low output voltage or skip mode:

Figure 4 IC supply from DSS

The converter will enter into "self-supply" mode when DSS is activated, which is during skip mode (long off time), or if the IC1 powering is not done from the output voltage (C3). For example if the output voltage is lower than Vcc(min) voltage of the IC1 minus voltage drop on D7 and R4. If supplying from the output voltage is not possible or not used, devices D7 and R4 are not needed, they can be omitted. The DSS is composed of 8 mA supply, which charges Vcc capacitor from HV line. See IC1 DS for details. If the Vcc voltage is lower than Vcc(min) level, the DSS is activated. The charging current (loop C) 8 mA flows from Drain pin via Vcc capacitor C8 through the load back to C4. The average current is equal to IC1 consumption. The charging (loop C) current is energy transferred to the output, which is not controlled by FB loop (B). Even if the IC1 is not switching at all (i.e. TSD is activated) there is a current (loop C) which flows to the output and increases the output voltage (under no load conditions). This is another reason for using a Zener diode D1 to protect output voltage from becoming too high.

Design procedure

1. On time vs off time ratio:

$$\frac{t_{on}}{t_{off}} = \frac{V_{out} + V_{fD3}}{V_{in} - V_{out}}$$
 eq. 1

The result is a ratio between on time and off time, at which the converter will run in CRM mode. It means the internal MOSFET will be turned on at the moment the inductor current reaches zero. It depends on user needs if CCM or CRM mode is required.

2. Inductor value calculation:

$$L2 = \frac{V_{out}}{f_{sw} \cdot \Delta I_{L2(max)}} \cdot \frac{t_{off}}{t_{on} + t_{off}}$$
eq. 2

The calculated inductor value will probably not be available, because they are manufactured only in specific values. The peak current for selected inductor is:

$$I_{L2(pk)} = I_{OUT} + \frac{V_{out}}{2 \cdot f_{sw} \cdot L2} \cdot \frac{t_{off}}{t_{on} + t_{off}}$$
eq. 3

The inductor is exposed to rectified input voltage. Use the inductor with appropriate voltage range.

3. Output capacitor C3 value:

$$C3 \ge \frac{\Delta I_{L2}}{8 \cdot f_{sw} \cdot (\Delta V_{OUT} - \Delta I_{L2} \cdot ESR_{C3})}$$
eq. 4

where:

 ΔI_{L2} - maximum inductor current ripple

f_{SW} - switching frequency

 ΔV_{OUT} - allowable output voltage drop during steady state conditions

It is recommended to use higher capacitor value than calculated, to cover energy demand during transients. It takes time to increase power delivery from the input to the output (due to limited FB loop speed). Higher capacitor value can supply the output energy demand before the power supply increases the power delivery. The overshoots will be lower as well for the same reason.

Output capacitor C3 RMS current:

$$I_{C3(RMS)} = I_{OUT} \cdot \frac{t_{off}}{\sqrt{12} \cdot \tau_{L2} \cdot (t_{on} + t_{off})} \qquad \text{eq. 5}$$
$$\tau_{L2} = \frac{L2}{R_{LOAD} \cdot t_{SW}} \qquad \text{eq. 6}$$

4. FB resistor divider sets up the output voltage. Value of resistor R3 is determined with respect to power loss on the entire resistor divider. The R5||R6 resistor is calculated using these formulas:

$$I_{R3} = \frac{V_{OUT} - V_{FWD(D2)} + V_{FWD(D3)} - V_{REF}}{R3}$$
 eq. 7

R5||R6 =
$$\frac{V_{REF}}{I_{R3} + I_{FB}}$$
 eq. 8

- 5. Bootstrap capacitor C1 value assessment requires to consider several aspects:
 - If the IC1 is self-supplied from the output voltage, capacitor C1 must be discharged via FB divider faster than C8 by IC consumption. This inequation must be fulfilled:

$$\frac{C8}{I_{CC@Vcc}} > \frac{C1 \cdot (R3 + R5||R6)}{V_{C1}}$$
 eq. 9

- From small signal model point of view, the C8 capacitor is connected in parallel to C1, so it will influence the FB loop control.
- The buck converter in this arrangement has no direct FB signal from the output voltage. The C1 capacitor is charged to the output voltage during inductor's demagnetization period. The output voltage is not monitored after the demagnetization nor during the on time.
- If too small C1 value is used, the output voltage will rise up in no load conditions. Every turn on period delivers an energy to the output, which increases the voltage. A dummy load (like Zener diode) effectively clamps the voltage at a safe level.
- If too big C1 value is used, the output voltage will not rise so high, no load consumption is lower (fewer switching periods are needed to keep C1 at a required level), load regulation is better. On the other hand, any step load (from low to high) causes much deeper voltage drop, because the C1 is charged only from the output, not discharged to the output.

- For the Comp pin device calculation please see: <u>https://www.onsemi.com/pub/Collateral/LOOP%20STABILIZATION%20FOR%2010</u> <u>6X.PDF</u>
- 7. Bulk capacitor calculation for full wave bridge rectifier:

$$C4 = \frac{\frac{P_{IN}}{f_{AC}} \cdot \left(\frac{1}{2} + \frac{\arcsin \cdot \left(\frac{V_{IN(min)}}{V_{IN(pk)}}\right)}{\pi}\right)}{V_{IN(pk)}^{2} - V_{IN(min)}^{2}}$$
eq. 10

Bulk capacitor calculation for single diode rectifier (half wave):

$$\frac{P_{IN}}{f_{AC}} \cdot \left(\frac{3}{2} + \frac{\arcsin \cdot \left(\frac{V_{IN(min)}}{V_{IN(pk)}}\right)}{\pi}\right)$$
eq. 11
$$C4 = \frac{V_{IN(pk)}^{2} - V_{IN(min)}^{2}}{V_{IN(pk)}^{2} - V_{IN(min)}^{2}}$$

Where:

 $V_{IN(min)}$ – minimum voltage on C4

 $V_{IN(pk)}$ – maximum voltage on C4, usually it is $V_{IN(pk)} = V_{IN} \cdot \sqrt{2}$

PIN - input power, calculated as POUT divided by expected efficiency

f_{AC} – main grid frequency

Measured data



Figure 5 Efficiency for two different C1 value (27 nF and 220 nF).







Figure 7 Influence of C1 value on no load consumption.



10 Dec 2018 11:10:01 Figure 19 110 Vac, start to 420 mA load, C1 27 nF

Figure 18 110 Vac, start to 20 mA load, C1 27 nF

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71.0 V

Figure 22 230 Vac, start to 20 mA load, C1 27 nF

BOM

Onsemi

Bill of Materials for the NCP10672 Buck SOIC7 Demo Board 15 V

Designator	Quantity	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Lead Free				
C1	1	CAPACITOR	27 nF	10%	0603	Kemet	C0603C273K5RACTU	Yes	Yes				
C2	1	CAPACITOR	47 nF	10%	0603	Kemet	C0603C473K5RACTU	Yes	Yes				
C3	1	CAPACITOR	47 µF	20%	1210	Taiyo Yuden	TMK325ABJ476MM-P	Yes	Yes				
C4	1	ELECTROLYTIC CAPACITOR	2.2 μF 400 V	20%	THROUGH HOLE	Yageo Würth Elektronik	SE400M2R20B3S-0811 860021374008	Yes	Yes				
C7	1	CAPACITOR	5.6 nF	10%	0603	Kemet	C0603C562K5RACTU	Yes	Yes				
C8	1	CAPACITOR	2.2 µF	20%	0603	TDK	C1608JB1E225M080AB	Yes	Yes				
R1	1	RESISTOR	10 Ω	5%	0207	Yageo	KNP1WSJT-52-10R	Yes	Yes				
R2	1	RESISTOR	3.6 kΩ	1%	0603	Yageo	RT0603FRE073K6L	Yes	Yes				
R3	1	RESISTOR	33 kΩ	1%	0603	Yageo	RT0603FRE0733KL	Yes	Yes				
R4	1	RESISTOR	560 Ω	1%	0603	Yageo	RT0603FRE0756RL	Yes	Yes				
R5	1	RESISTOR	150 kΩ	1%	0603	Yageo	RT0603FRE07150KL	Yes	Yes				
R6	1	RESISTOR	10 kΩ	1%	0603	Yageo	RT0603FRE0710KL	Yes	Yes				
D1	1	ZENER DIODE	MMSZ16	5%	SOD123	onsemi	MM3Z6V2	No	Yes				
D2, D3	2	DIODE	ES1JFL	-	SOD123	onsemi	ES1JFL	No	Yes				
D4, D5, D5, D8	4	DIODE	S1JFL	-	SOD123	onsemi	S1JFL	No	Yes				
D7	1	DIODE	1N4148	-	SOD123	onsemi	1N4148WS	No	Yes				
IC1	1	SWITCHER	NCP10672	-	SOIC7	onsemi	NCP10672BD060R2G	No	Yes				
L1	1	INDUCTOR	1.0 mH	20%	SMD/SMT	Würth Elektronik	744777930	No	Yes				
L2	1	INDUCTOR	280 µH	20%	SMD/SMT	Würth Elektronik	7687709681	No	Yes				
BOARD STANDOFF	4	HEX STANDOFF M3 NYLON	8.0 mm	-	-	Harwin	R30-1610800	Yes	Yes				

References

onsemi datasheet for NCP1067x monolithic switcher.

onsemi Design Notes DN05012, DN05017, DN05018, DN05080.

onsemi Design Note:

https://www.onsemi.com/pub/Collateral/LOOP%20STABILIZATION%20FOR%20106X.PDF

Würth Electronic Website: https://www.we-online.com/web/en/wuerth_elektronik/start.php

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