# MUN2136, MMUN2136L, MUN5136, DTA115EE, DTA115EM3

# Digital Transistors (BRT) R1 = 100 kΩ, R2 = 100 kΩ

## PNP Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

### Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

**MAXIMUM RATINGS** ($T_A$ = 25°C)

| Rating | Symbol | Max | Unit |
|---|---|---|---|
| Collector−Base Voltage | $V_{CBO}$ | 50 | Vdc |
| Collector−Emitter Voltage | $V_{CEO}$ | 50 | Vdc |
| Collector Current − Continuous | $I_C$ | 100 | mAdc |
| Input Forward Voltage | $V_{IN(fwd)}$ | 40 | Vdc |
| Input Reverse Voltage | $V_{IN(rev)}$ | 10 | Vdc |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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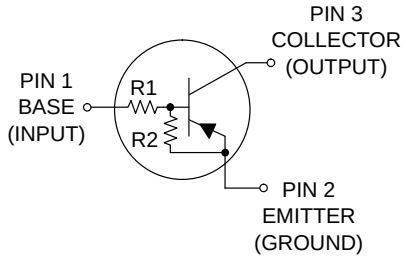
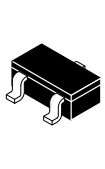
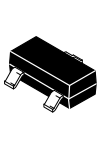
### PIN CONNECTIONS



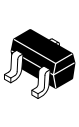

### MARKING DIAGRAMS



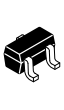

**SC−59**
**CASE 318D**
**STYLE 1**




**SOT−23**
**CASE 318**
**STYLE 6**




**SC−70/SOT−323**
**CASE 419**
**STYLE 3**




**SC−75**
**CASE 463**
**STYLE 1**


**SOT−723**
**CASE 631AA**
**STYLE 1**

XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending up- on manufacturing location.

### ORDERING INFORMATION

See detailed ordering, marking, and shipping information in the package dimensions section on page 2 of this data sheet.

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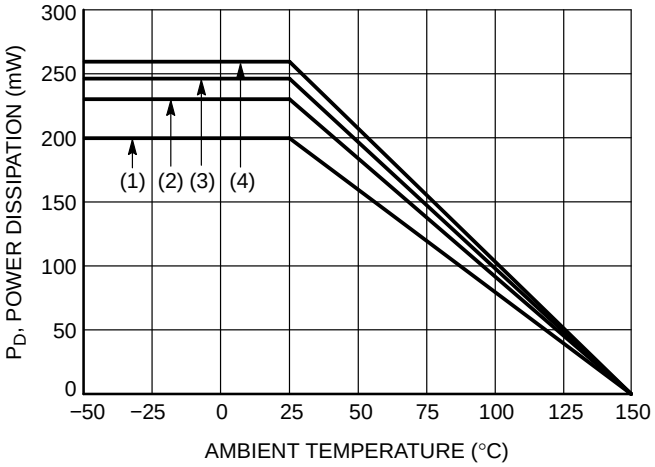
**Table 1. ORDERING INFORMATION**

| Device | Part Marking | Package | Shipping† |
|---|---|---|---|
| MUN2136T1G | 6N | SC−59 (Pb−Free) | 3000 / Tape & Reel |
| MMUN2136LT1G, NSVMMUN2136LT1G* | ACG | SOT−23 (Pb−Free) | 3000 / Tape & Reel |
| MUN5136T1G, NSVMUN5136T1G* | 6N | SC−70/SOT−323 (Pb−Free) | 3000 / Tape & Reel |
| DTA115EET1G, NSVDTA115EET1G* | 6N | SC−75 (Pb−Free) | 3000 / Tape & Reel |
| DTA115EM3T5G | 6N | SOT−723 (Pb−Free) | 8000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.




(1) SC−75 and SC−70/SOT323; Minimum Pad
(2) SC−59; Minimum Pad
(3) SOT−23; Minimum Pad
(4) SOT−723; Minimum Pad

**Figure 1. Derating Curve**

**Table 2. THERMAL CHARACTERISTICS**

| Characteristic | | Symbol | Max | Unit |
|---|---|---|---|---|
| **THERMAL CHARACTERISTICS (SC−59) (MUN2136)** | | | | |
| Total Device Dissipation | | $P_D$ | | |
| $T_A$ = 25°C | (Note 1) | | 230 | mW |
| | (Note 2) | | 338 | |
| Derate above 25°C | (Note 1) | | 1.8 | mW/°C |
| | (Note 2) | | 2.7 | |
| Thermal Resistance, Junction to Ambient | (Note 1) | $R_{\theta JA}$ | 540 | °C/W |
| | (Note 2) | | 370 | |
| Thermal Resistance, Junction to Lead | (Note 1) | $R_{\theta JL}$ | 264 | °C/W |
| | (Note 2) | | 287 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | −55 to +150 | °C |
| **THERMAL CHARACTERISTICS (SOT−23) (MMUN2136L)** | | | | |
| Total Device Dissipation | | $P_D$ | | |
| $T_A$ = 25°C | (Note 1) | | 246 | mW |
| | (Note 2) | | 400 | |
| Derate above 25°C | (Note 1) | | 2.0 | mW/°C |
| | (Note 2) | | 3.2 | |
| Thermal Resistance, Junction to Ambient | (Note 1) | $R_{\theta JA}$ | 508 | °C/W |
| | (Note 2) | | 311 | |
| Thermal Resistance, Junction to Lead | (Note 1) | $R_{\theta JL}$ | 174 | °C/W |
| | (Note 2) | | 208 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | −55 to +150 | °C |
| **THERMAL CHARACTERISTICS (SC−70/SOT−323) (MUN5136)** | | | | |
| Total Device Dissipation | | $P_D$ | | |
| $T_A$ = 25°C | (Note 1) | | 202 | mW |
| | (Note 2) | | 310 | |
| Derate above 25°C | (Note 1) | | 1.6 | mW/°C |
| | (Note 2) | | 2.5 | |
| Thermal Resistance, Junction to Ambient | (Note 1) | $R_{\theta JA}$ | 618 | °C/W |
| | (Note 2) | | 403 | |
| Thermal Resistance, Junction to Lead | (Note 1) | $R_{\theta JL}$ | 280 | °C/W |
| | (Note 2) | | 332 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | −55 to +150 | °C |
| **THERMAL CHARACTERISTICS (SC−75) (DTA115EE)** | | | | |
| Total Device Dissipation | | $P_D$ | | |
| $T_A$ = 25°C | (Note 1) | | 200 | mW |
| | (Note 2) | | 300 | |
| Derate above 25°C | (Note 1) | | 1.6 | mW/°C |
| | (Note 2) | | 2.4 | |
| Thermal Resistance, Junction to Ambient | (Note 1) | $R_{\theta JA}$ | 600 | °C/W |
| | (Note 2) | | 400 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | −55 to +150 | °C |
| **THERMAL CHARACTERISTICS (SOT−723) (DTA115EM3)** | | | | |
| Total Device Dissipation | | $P_D$ | | |
| $T_A$ = 25°C | (Note 1) | | 260 | mW |
| | (Note 2) | | 600 | |
| Derate above 25°C | (Note 1) | | 2.0 | mW/°C |
| | (Note 2) | | 4.8 | |
| Thermal Resistance, Junction to Ambient | (Note 1) | $R_{\theta JA}$ | 480 | °C/W |
| | (Note 2) | | 205 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | −55 to +150 | °C |

1. FR−4 @ Minimum Pad.
2. FR−4 @ 1.0 x 1.0 Inch Pad.

**Table 3. ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C, unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Collector−Base Cutoff Current ($V_{CB}$ = 50 V, $I_E$ = 0) | $I_{CBO}$ | – | – | 100 | nAdc |
| Collector−Emitter Cutoff Current ($V_{CE}$ = 50 V, $I_B$ = 0) | $I_{CEO}$ | – | – | 500 | nAdc |
| Emitter−Base Cutoff Current ($V_{EB}$ = 6.0 V, $I_C$ = 0) | $I_{EBO}$ | – | – | 0.05 | mAdc |
| Collector−Base Breakdown Voltage ($I_C$ = 10 μA, $I_E$ = 0) | $V_{(BR)CBO}$ | 50 | – | – | Vdc |
| Collector−Emitter Breakdown Voltage (Note 3) ($I_C$ = 2.0 mA, $I_B$ = 0) | $V_{(BR)CEO}$ | 50 | – | – | Vdc |
| **ON CHARACTERISTICS** | | | | | |
| DC Current Gain (Note 3) ($I_C$ = 5.0 mA, $V_{CE}$ = 10 V) | $h_{FE}$ | 80 | 150 | – | |
| Collector−Emitter Saturation Voltage (Note 3) ($I_C$ = 10 mA, $I_B$ = 0.3 mA) | $V_{CE(sat)}$ | – | – | 0.25 | Vdc |
| Input Voltage (off) ($V_{CE}$ = 5.0 V, $I_C$ = 100 μA) | $V_{i(off)}$ | – | 1.2 | 0.5 | Vdc |
| Input Voltage (on) ($V_{CE}$ = 0.3 V, $I_C$ = 1.0 mA) | $V_{i(on)}$ | 3.0 | 1.6 | – | Vdc |
| Output Voltage (on) ($V_{CC}$ = 5.0 V, $V_B$ = 5.5 V, $R_L$ = 1.0 kΩ) | $V_{OL}$ | – | – | 0.2 | Vdc |
| Output Voltage (off) ($V_{CC}$ = 5.0 V, $V_B$ = 0.5 V, $R_L$ = 1.0 kΩ) | $V_{OH}$ | 4.9 | – | – | Vdc |
| Input Resistor | R1 | 70 | 100 | 130 | kΩ |
| Resistor Ratio | $R_1/R_2$ | 0.8 | 1.0 | 1.2 | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle ≤ 2%.

## TYPICAL CHARACTERISTICS
## MUN2136, MMUN2136L, MUN5136, DTA115EE, DTA115EM3

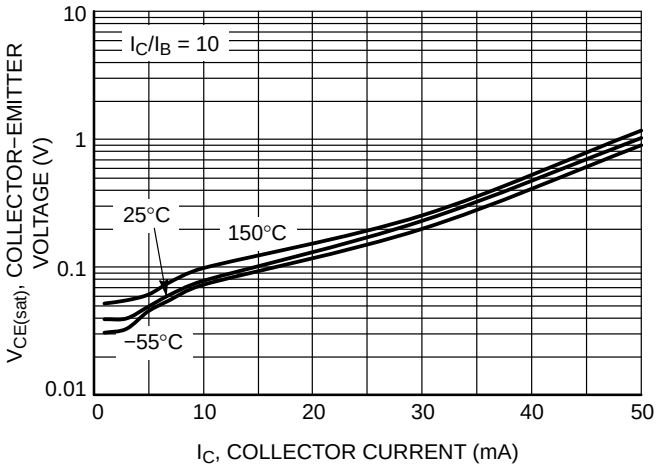



**Figure 2. $V_{CE(sat)}$ vs. $I_C$**

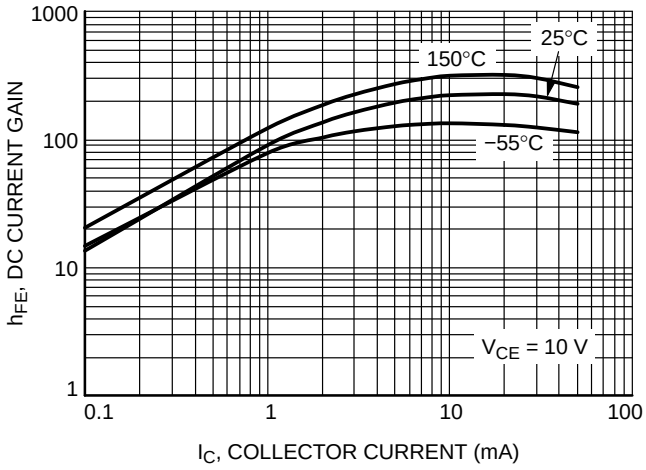



**Figure 3. DC Current Gain**

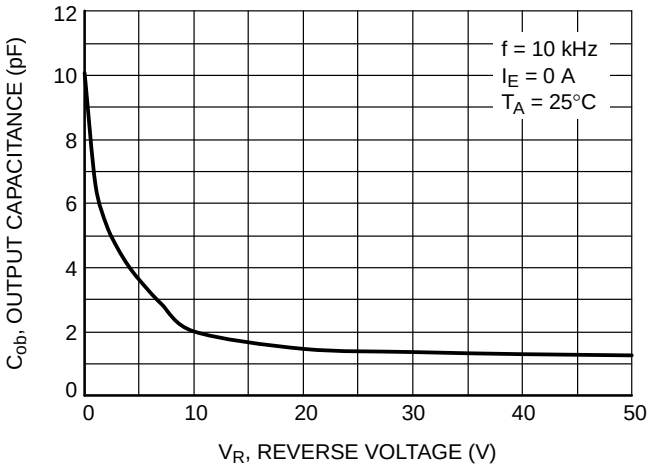



**Figure 4. Output Capacitance**

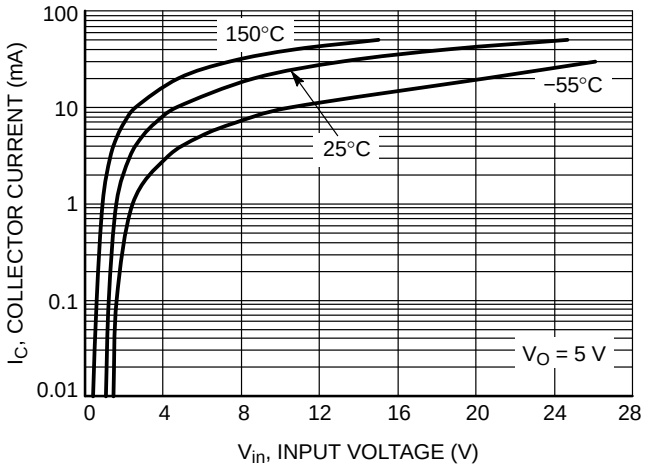



**Figure 5. Output Current vs. Input Voltage**

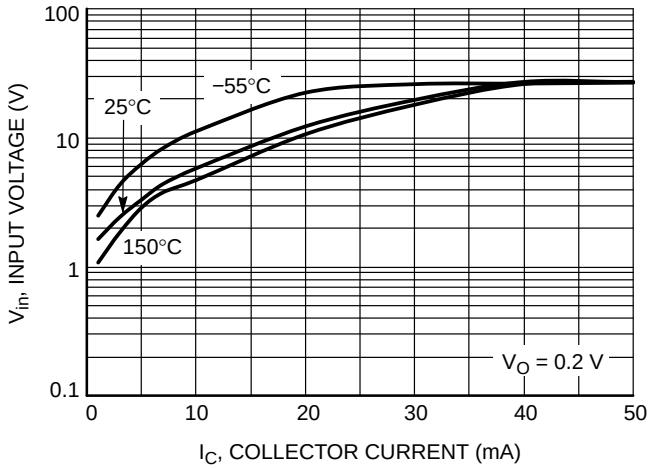
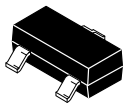



**Figure 6. Input Voltage vs. Output Current**

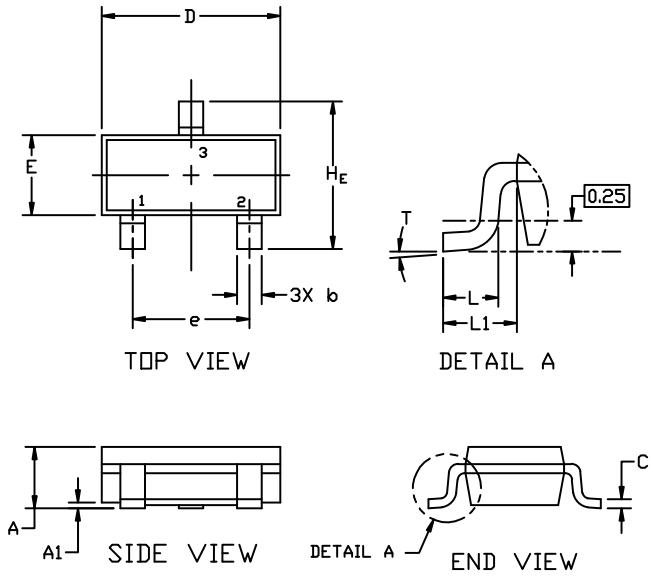
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS



SCALE 4:1

**SOT−23 (TO−236)**
CASE 318
ISSUE AT

DATE 01 MAR 2023

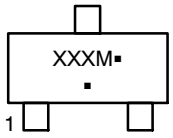



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

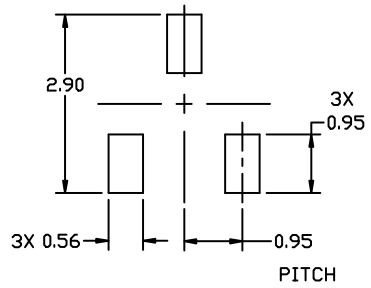
| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.89 | 1.00 | 1.11 | 0.035 | 0.039 | 0.044 |
| A1 | 0.01 | 0.06 | 0.10 | 0.000 | 0.002 | 0.004 |
| b | 0.37 | 0.44 | 0.50 | 0.015 | 0.017 | 0.020 |
| c | 0.08 | 0.14 | 0.20 | 0.003 | 0.006 | 0.008 |
| D | 2.80 | 2.90 | 3.04 | 0.110 | 0.114 | 0.120 |
| E | 1.20 | 1.30 | 1.40 | 0.047 | 0.051 | 0.055 |
| e | 1.78 | 1.90 | 2.04 | 0.070 | 0.075 | 0.080 |
| L | 0.30 | 0.43 | 0.55 | 0.012 | 0.017 | 0.022 |
| L1 | 0.35 | 0.54 | 0.69 | 0.014 | 0.021 | 0.027 |
| $H_E$ | 2.10 | 2.40 | 2.64 | 0.083 | 0.094 | 0.104 |
| T | 0° | --- | 10° | 0° | --- | 10° |

### GENERIC MARKING DIAGRAM*




XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.




RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42226B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. | |
| **DESCRIPTION:** | **SOT−23 (TO−236)** | | **PAGE 1 OF 2** |

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**SOT−23 (TO−236)**
CASE 318
ISSUE AT

DATE 01 MAR 2023

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE



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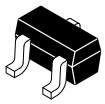
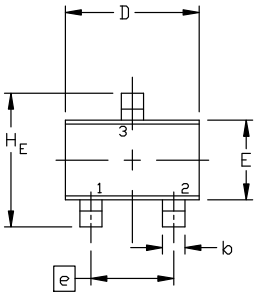
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**SC−70 (SOT−323)**
CASE 419
ISSUE R

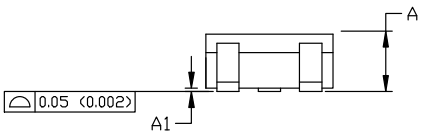
DATE 11 OCT 2022



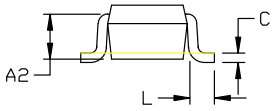
**SCALE 4:1**




TOP VIEW



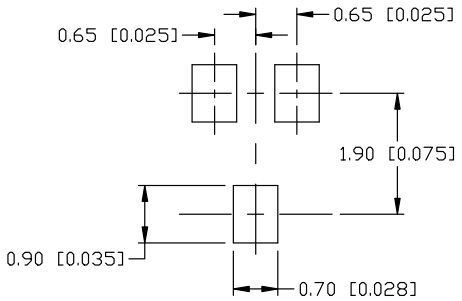

SIDE VIEW




END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH

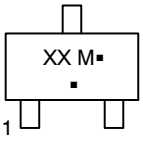
| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.80 | 0.90 | 1.00 | 0.032 | 0.035 | 0.040 |
| A1 | 0.00 | 0.05 | 0.10 | 0.000 | 0.002 | 0.004 |
| A2 | 0.70 REF | | | 0.028 BSC | | |
| b | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| c | 0.10 | 0.18 | 0.25 | 0.004 | 0.007 | 0.010 |
| D | 1.80 | 2.00 | 2.20 | 0.071 | 0.080 | 0.087 |
| E | 1.15 | 1.24 | 1.35 | 0.045 | 0.049 | 0.053 |
| e | 1.20 | 1.30 | 1.40 | 0.047 | 0.051 | 0.055 |
| e1 | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.20 | 0.38 | 0.56 | 0.008 | 0.015 | 0.022 |
| $H_E$ | 2.00 | 2.10 | 2.40 | 0.079 | 0.083 | 0.095 |




* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOLDERING FOOTPRINT

### GENERIC MARKING DIAGRAM




XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
CANCELLED

STYLE 2:
PIN 1. ANODE
2. N.C.
3. CATHODE

STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 6:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 7:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 8:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. ANODE−CATHODE

STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

| | | |
|---|---|---|
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| **DESCRIPTION:** | **SC−70 (SOT−323)** | **PAGE 1 OF 1** |

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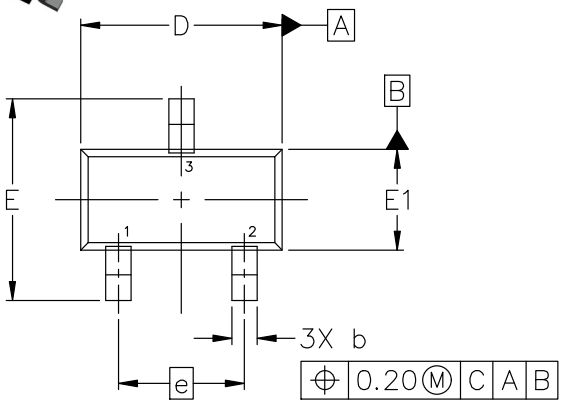
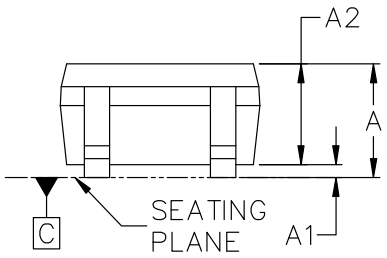
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**SC75−3 1.60x0.80x0.80, 1.00P**
CASE 463
ISSUE H

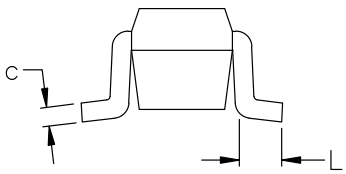
DATE 01 FEB 2024




TOP VIEW




SIDE VIEW



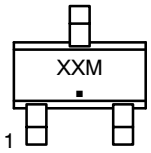

END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.

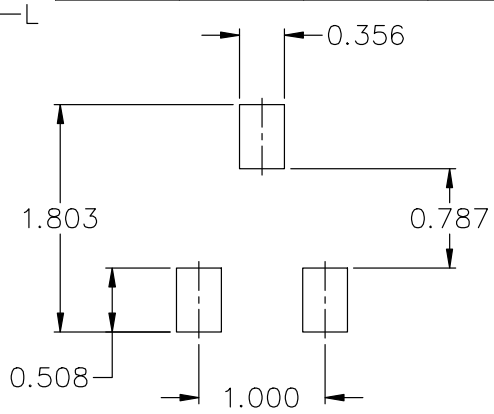
| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.70 | 0.80 | 0.90 |
| A1 | 0.00 | 0.05 | 0.10 |
| A2 | | 0.80 REF. | |
| b | 0.15 | 0.20 | 0.30 |
| c | 0.10 | 0.15 | 0.25 |
| D | 1.55 | 1.60 | 1.65 |
| E | 1.50 | 1.60 | 1.70 |
| E1 | 0.70 | 0.80 | 0.90 |
| e | | 1.00 BSC | |
| L | 0.10 | 0.15 | 0.20 |

**GENERIC**
**MARKING DIAGRAM***




XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.




RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN

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|---|---|---|
| DESCRIPTION: | SC75−3 1.60x0.80x0.80, 1.00P | PAGE 1 OF 1 |

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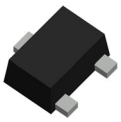
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

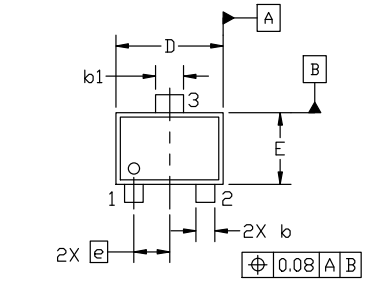


**SOT−723 1.20x0.80x0.50, 0.40P**
CASE 631AA
ISSUE E

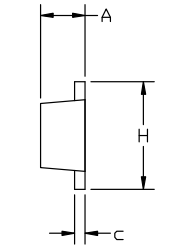
DATE 24 JAN 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

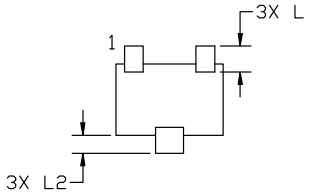
| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | 0.45 | 0.50 | 0.55 |
| b | 0.15 | 0.21 | 0.27 |
| b1 | 0.25 | 0.31 | 0.37 |
| c | 0.07 | 0.12 | 0.17 |
| D | 1.15 | 1.20 | 1.25 |
| E | 0.75 | 0.80 | 0.85 |
| e | 0.40 BSC | | |
| H | 1.15 | 1.20 | 1.25 |
| L | 0.29 REF | | |
| L2 | 0.15 | 0.20 | 0.25 |



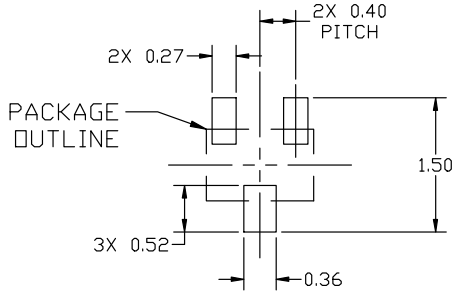
TOP VIEW



SIDE VIEW



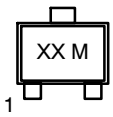
BOTTOM VIEW



RECOMMENDED MOUNTING
FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC
### MARKING DIAGRAM*

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M = Date Code

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3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

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2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN

| | | |
|---|---|---|
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| **DESCRIPTION:** | **SOT−723 1.20x0.80x0.50, 0.40P** | **PAGE 1 OF 1** |

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