



ON Semiconductor®

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## 7 Channel PMIC with 2 DC-DC Converters, 5 LDOs and a Triple Input 10 bits ADC Evaluation Kit Manual

### EVALUATION KIT MANUAL

The NCP6925EVK evaluation kit is a full assembled circuit board for evaluation and test of the NCP6925. This document provides documentation, test procedure and equipment set-up for the complete evaluation of the NCP6925. The NCP6925EVK comes with one NCP6925 evaluation board, 1 MCU board for I<sup>2</sup>C master and associated cables.

#### General Description

The NCP6925 integrated circuit is part of the ON Semiconductor mini power management IC family (PMIC). It is optimized to supply battery powered portable application sub-systems such as camera function, microprocessors. This device integrates 2 high efficiency 1 A step-down DC-DC converters, 5 low dropout (LDO) voltage regulators and a triple input 10 bits ADC in a WLCSP36 2.4 x 2.4 mm package.

#### Features

- 2 DC-DC Converters (3 MHz, 1  $\mu$ H / 10  $\mu$ F, 1 A)
  - ♦ Peak Efficiency 95%
  - ♦ Programmable Output Voltage from 0.6 V to 3.3 V by 12.5 mV Steps
- 5 Low Noise – Low Dropout Regulators (2.2  $\mu$ F, 300 mA)
  - ♦ Programmable Output Voltage from 0.8 V to 3.5 V by 25 mV Steps
- Triple Input 10 bits ADC
  - ♦ Dual Resistors Measurement Mode
  - ♦ General Purpose Mode
- Control
  - ♦ Fully Programmable Through a 400 kHz / 3.4 MHz I<sup>2</sup>C with Pins Selectable I<sup>2</sup>C Address and Interrupt Output
  - ♦ Power on Input and General Purpose I/O Pins that can be used as DC-DC Enable Pins
- Very Low Quiescent Current at No Load
- Small Footprint : 2.4 x 2.4 mm WLCSP 0.4 mm Pitch

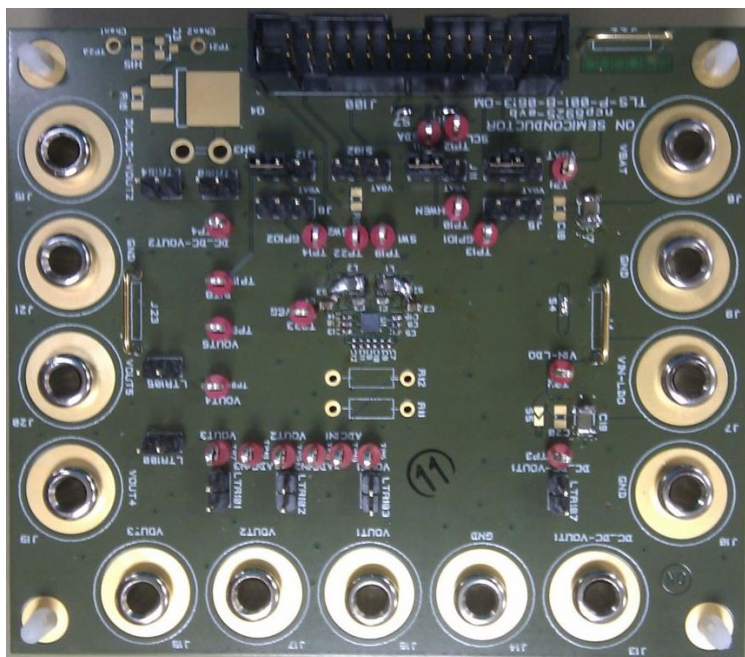


Figure 1. Evaluation Board Picture

# NCP6925EVK

**Table 1. BOARD COMPONENTS DESCRIPTION**

Qty	Reference	Value	PCB Footprint	MFR	Part Number
1	–	NCP6925 PMIC	–	ON Semiconductor	NCP6925
1	R13	SMD Resistor 10 K $\Omega$	0603	Panasonic	ERJ-3GEY0R00V
10	C5, C6, C7, C8, C9, C10, C11, C12, C13, C14	Ceramic Capacitor 2.2 $\mu$ F 6.3 V X5R	0402	TDK	C1005X5R0J225K050BC
2	C15, C16	Ceramic Capacitor 1 $\mu$ F 6.3 V X5R	0402	TDK	C1005X5R0J105K05BB
2	C1, C3	Ceramic Capacitor 4.7 $\mu$ F 6.3 V X5R	0603	TDK	C1608X5R0J475K080AB
2	C2, C4	Ceramic Capacitor 10 $\mu$ F 6.3 V X5R	0603	TDK	C1608X5R0J475K080AB
2	C17, C19	Ceramic Capacitor 100 $\mu$ F 6.3 V X5R	1210	TDK	C3225X5R0J107M250AC
2	L1, L2	Inductor	2016	TOKO	DFE2016R-H-2R2N
14	J3, J5, J8, J11, J12, S102, LTR100 $\rightarrow$ LTR107	Jumper Header Vertical Mount, 3 positions, 100mils	100 mils	Tyco Electronics / AMP	5-826629-0
13	J13 $\rightarrow$ J21 J6, J7, J9, J10	Banana Jack		Hirschmann Test and Measurement	930160000
1	J100	Connector header 26 pos		3M	N2526-6002-RB
23	TP1 ... TP23	Test Point		Keystone Electronics	5011
4	Q3, Q4, R15, R16,	Not Mounted			
3	J4, J22, J23	Jumper Connector	400 mils	Harwin	D3082-B01
3	S4, S6, S7	Shorted			
4	Spacer nylon	H1, H2, H3, H4		Richco Plastic co	R908-4

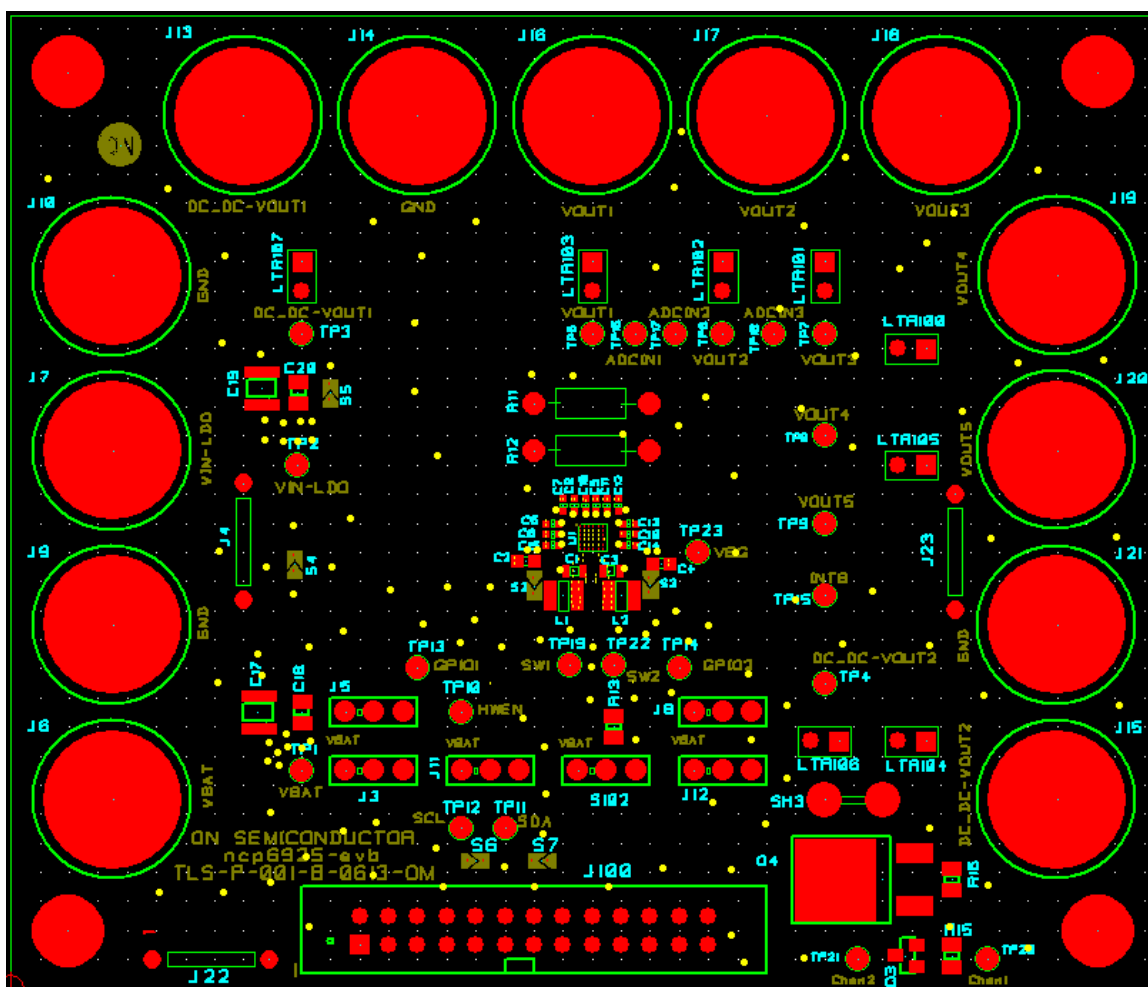
**Table 2. CONNECTOR DESCRIPTION**

Input Power		
Vbat (J6–J9)	–	<b>negative</b> input connected to <b>GND</b> pin (J9)
	AVIN and PVIN	Core and DCDCs power supply (J6)
VIN_LDO (J7–J10)	–	<b>negative</b> input connected to <b>GND</b> pin (J10)
	VIN_LDO	Dedicated LDOs power supply. S4 has to be unsoldered (J10)
Regulators Outputs		
J(13 $\rightarrow$ J21)	–	<b>negative</b> output connected to <b>GND</b> pin (J14 and J21)
	J13	DCDC1 output
	J15	DCDC2 output
	J16	LDO1 output
	J17	LDO2 output
	J18	LDO3 output
	J19	LDO4 output
	J20	LDO5 output

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**Table 2. CONNECTOR DESCRIPTION**

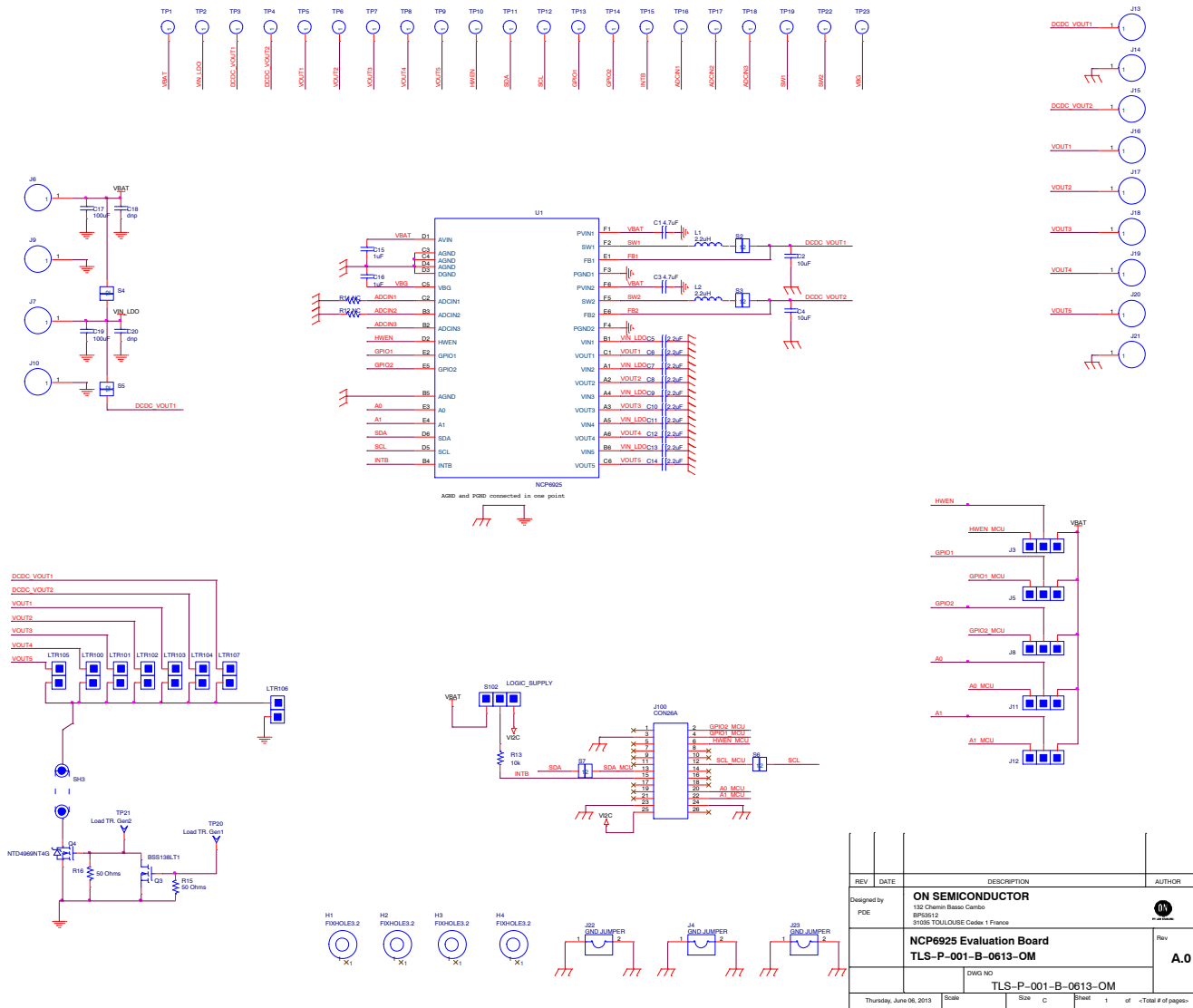
Chip Control		
MCU	SDA	I <sup>2</sup> C data, connect to <b>SDA</b> pin or the 26 pins ribbon cable
	SCL	I <sup>2</sup> C data, connect to <b>SCL</b> pin or the 26 pins ribbon cable
	HWEN	Master enable pin connected to the 26 pins ribbon cable thru J3
	A0	I <sup>2</sup> C address selectable pin connected to the 26 pins ribbon cable thru J11
	A1	I <sup>2</sup> C address selectable pin connected to the 26 pins ribbon cable thru J12
	GPIO1	GPIO pin connected to the 26 pins ribbon cable thru J5
	GPIO2	GPIO pin connected to the 26 pins ribbon cable thru J8



**Figure 2. Assembly Layer**

# NCP6925EVK

## SCHEMATIC



# NCP6925EVK

## SOFTWARE INSTALLATION

Double click on NCP6925\_setup.exe file. Follow the instructions set-up.

It is recommended to copy the NCP6925\_setup.exe to a local directory: If eval kit is already installed, a simple double click on NCP6925.exe will launch the GUI.

**Important notice: In order to properly install drivers and software, please launch NCP6925\_setup.exe file before connects the MCU board.**

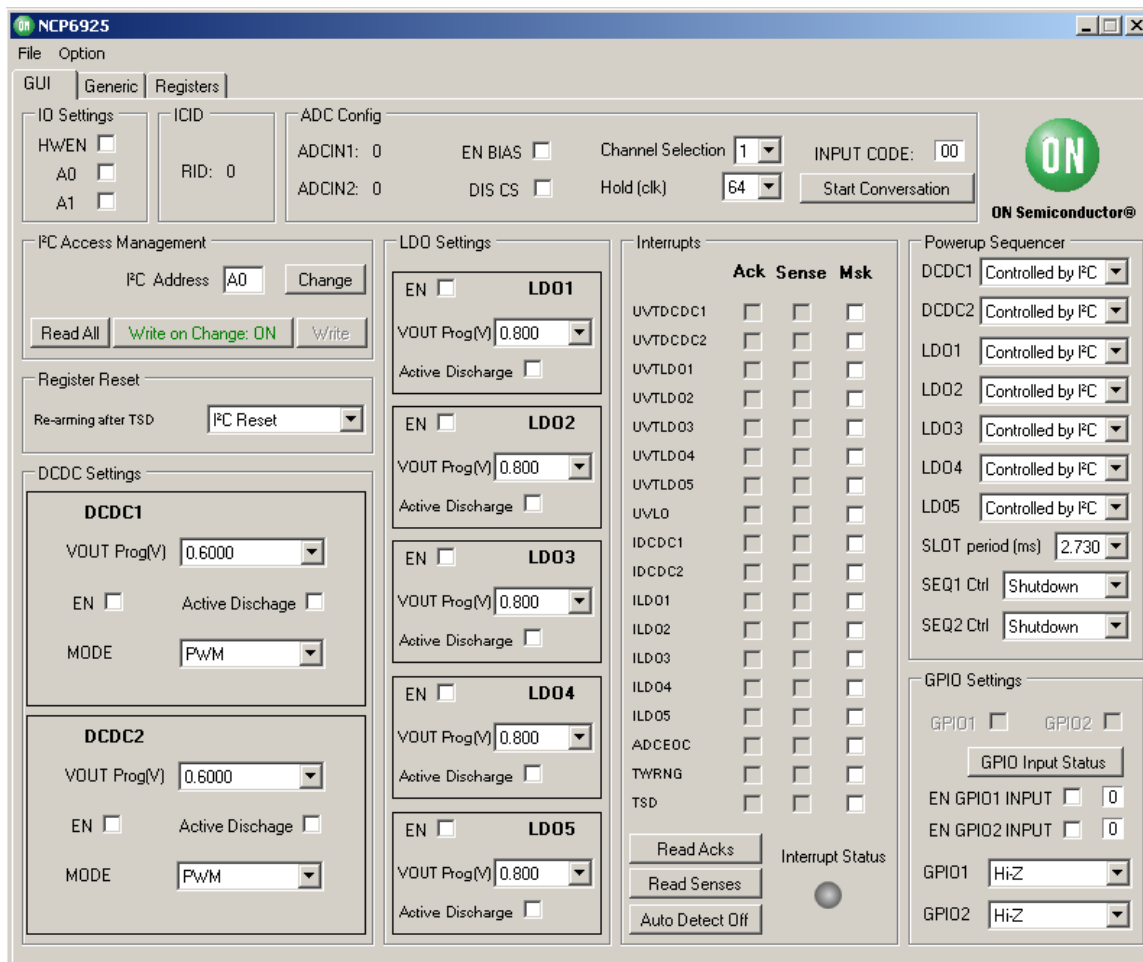


Figure 4.

## QUICK CONFIGURATION

### Power Supply

NCP6925 requires at least 1 external power supply :  
Vbat (J6) : supply between 2.5 V to 5.5 V.

### Jumpers Configuration

The HWEN, A0 and A1 jumpers are configured by default to work with the ONSEMI I<sup>2</sup>C interface board. GPIO1 and GPIO2 jumpers are not configured.

S4 shunt is soldered to use only one power supply for the DCDCs, LDOs and AVIN.

### Load

#### DCDCx Converters

An electronic load or passive load can be connected between J13 and J14 for DCDC1, between J15 and J21 for DCDC2.

#### LDOx Regulators

An electronic load or passive load can be connected between J16 and J14 or J21 for LDO1, between J17 and J14 or J21 for LDO2, J18 and J14 or J21 for LDO3, J19 and J14 or J21 for LDO4, J20 and J14 or J21 for LDO5.

#### ADC

TP13, TP14, TP18 can be used as general purpose input for the ADC.

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## PCB LAYOUT

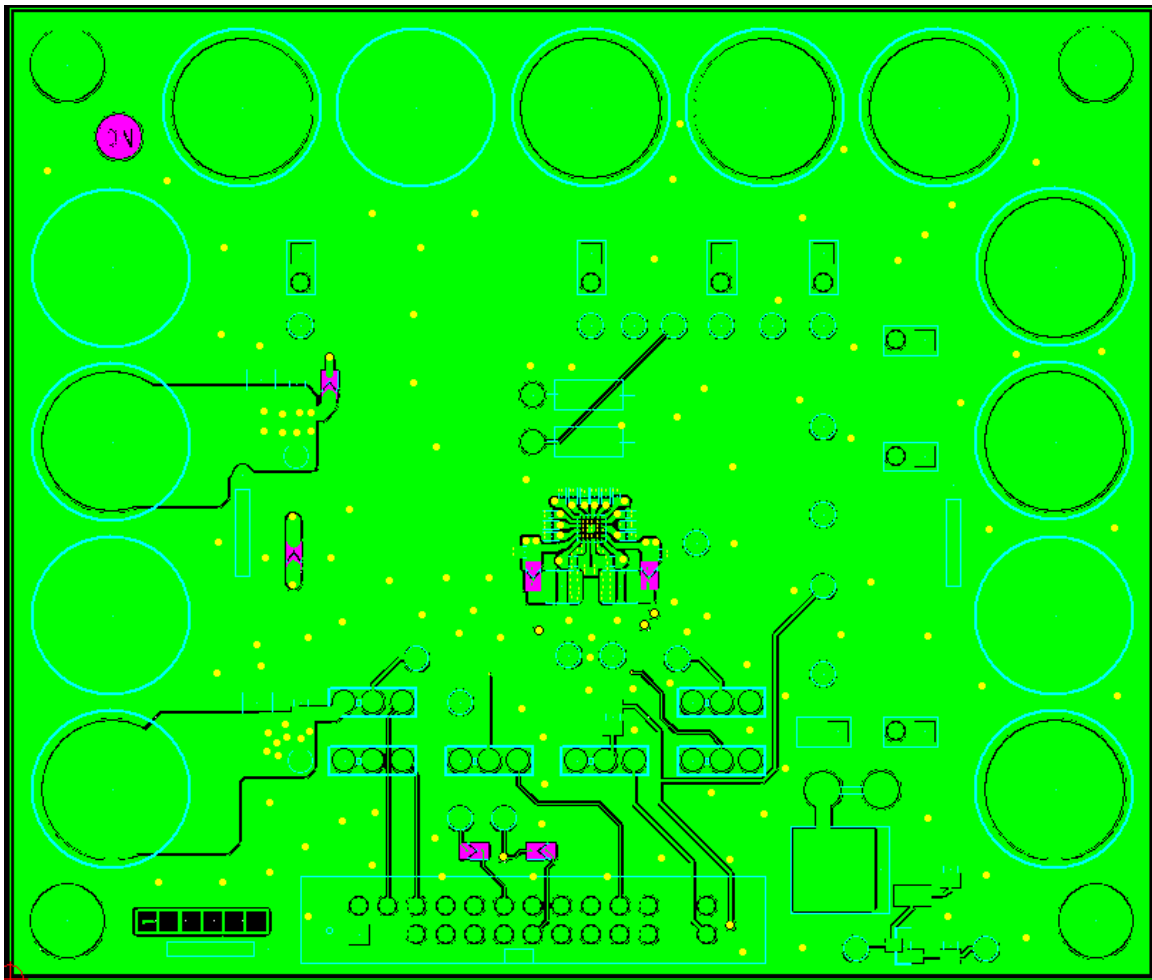


Figure 5. Top Layer

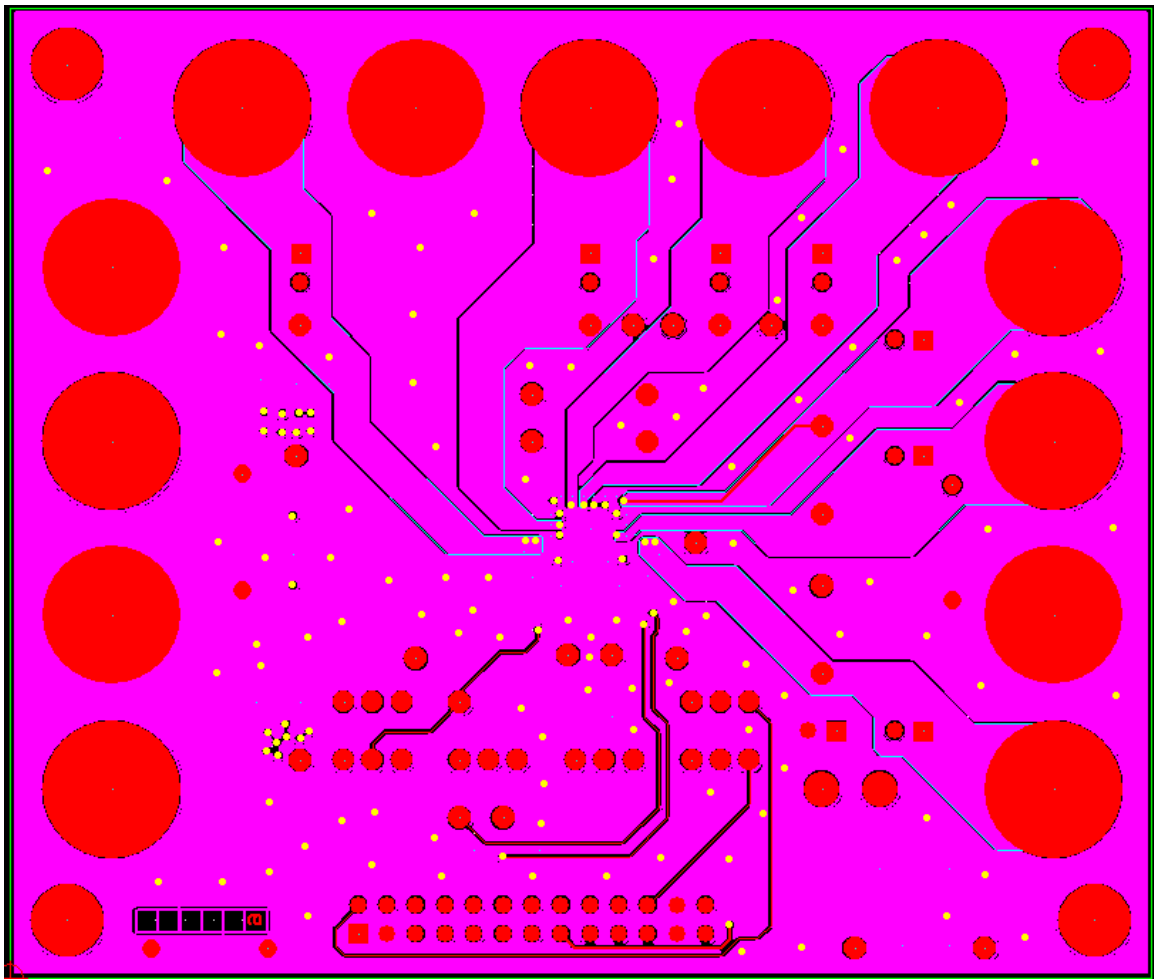


Figure 6. Bottom Layer

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