NCV7429V1GEVB

NCV7429 System Basis Chip Evaluation Board User's Manual

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

INTRODUCTION

This document describes the NCV7429 evaluation board for the ON Semiconductor NCV7429 System basis chip with a LIN transceiver, 5 V LDO, LS and HS switches. The functionality and major parameters can be evaluated using the NCV7429 evaluation board.

The NCV7429 is a monolithic LIN System−Basis−Chip with enhanced feature set useful in Automotive Body Control systems. Besides the LIN bus interface the IC features a 5 V voltage regulator, high−side and low−side switches to control LEDs and relays, and supervision functionality like a window watchdog. This allows a highly integrated solution by replacing external discrete components while maintaining the system flexibility. As a consequence, the board space and ECU weight can be minimized.

Figure 1. NCV7429V1GEVB Evaluation Board

EVALUATION BOARD FEATURES

- One−row pin header, providing the circuit signals, enables easy insertion of the evaluation board into a more complex application setup
- Oscilloscope test−points on all important signals
- Reverse protection and decoupling on the main (battery) supply
- Split supply paths for VS and VS_OUT device supply pins
- Decoupling on VR1 low−drop regulator output
- Additional pull−up resistors on the open−drain digital output NRES
- Filtering circuit on the switch−monitoring WU input
- On−board Local Wakeup switch
- Indication LEDs on NRES and FSO signals
- Master / Slave LIN−bus termination
- Good thermal connection of the circuit's exposed pad to the bottom ground plane
- Basic standalone functionality using Software Development Mode

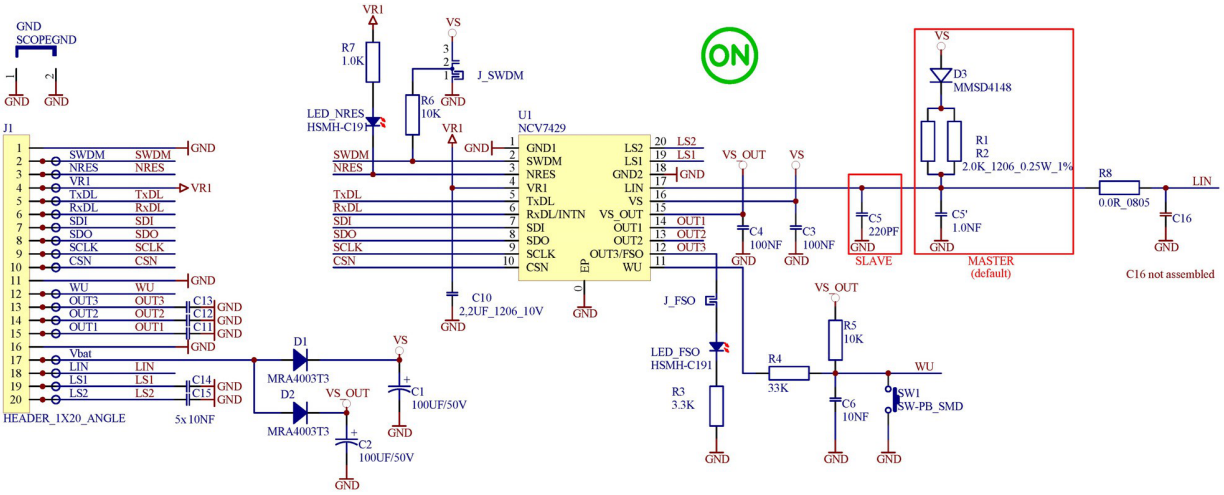

Figure 2. NCV7429 Evaluation Board Schematic

Table 1. ABSOLUTE MAXIMUM RATINGS

Rating	Pins	Min	Max	Unit
Supply voltage	Vbat	−40	40	V
VR1 regulator output voltage	VR1	−0.3	5.5	V
VR1 regulator output current	VR1	0	internally limited	mA
Digital inputs/outputs voltage	NRES, CSN, SCLK, SDI, SDO, TxDL, RxDL/INTN	−0.3	VR1+0.3	V
SWDM pin input voltage	SWDM	−0.3	40	
LIN bus line voltage	LIN	−40	40	V
Wake−up input voltage	WU	−0.3	Vbat	V
HS outputs voltage	OUT1−3	−0.3	Vbat	V
HS outputs current (from pin)	OUT1−3	0	internally limited	mA
LS outputs voltage (limited internally during flyback)	LS1/2	−0.3	40	V
LS outputs current	LS1/2	−120	Internally limited	mA
NCV7429 junction temperature		−40	+170	°C
Board temperature		−40	+125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. RECOMMENDED BOARD OPERATING CONDITIONS

Rating	Pins	Min	Max	Unit
Supply voltage	Vbat	0	28	V
VR1 regulator output voltage	VR1	4.9	5.1	V
VR1 regulator output current	VR1	0	150	mA
Digital inputs/outputs voltage	NRES, CSN, SCLK, SDI, SDO, TxDL, RxDL/INTN	0	VR1	V
SWDM pin input voltage	SWDM	−0.3	28	
LIN bus line voltage	LIN	0	Vbat	V
Wake−up input voltage	WU	0	Vbat	V
HS outputs voltage	OUT1−3	0	Vbat	V
HS outputs current (from pin)	OUT1−3	0	140	mA
LS outputs voltage (limited internally during flyback)	LS1/2	0	Vbat	V
LS outputs current	LS1/2	0	200	mA
NCV7429 junction temperature		−40	+150	°C
Board temperature		−40	+105	°C

OPERATIONAL GUIDELINES

NCV7429 is a complex SCB device, which needs external MCU, connected through J1 connector, to control all functions and settings. However NCV7429 may work in so called Software Development Mode (SWDM), where watchdog services are not needed. To configure NCV7429 into this mode, SWDM pin has to be tight to a voltage source of at least 10 V during start−up or while SWDM pin sampling is requested via SPI. Connection to VS is not recommended as the voltage ramp−up may be limited, which could lead to incorrect SWDM state sampling. Two on−board LEDs indicate faulty states of the board, as described in Table 4.

Table 3. SOLDERING STRAPS FUNCTIONS

Jumper	Position	Function
J_SWDM	”−” or not connected (GND)	Normal operation mode with external MCU connected (Watchdog service needed) OR SWDM supplied from an external power supply.
	”+” (VS)	Software Development Mode (Watchdog does not need to be served) In case of slow ramp−up of the Vbat voltage, SWDM may be incorrectly sampled Therefore an external voltage source on SWDM pin is recommended.
J_FSO		LED connection to OUT3/FSO

Table 4. LED FUNCTIONS

Jumper	Function
LED_NRES	Indicates activation of RSTN pin due to the following reasons: • Sleep/Fail−safe mode (LED_NRES off due to missing VR1 supply) • Reset mode (2 ms on)
LED_FSO	OUT3/FSO pin active due to failure condition: • Fatal VR1 failure • Watchdog failure (ignored if SWDM is High) • Thermal Shutdown

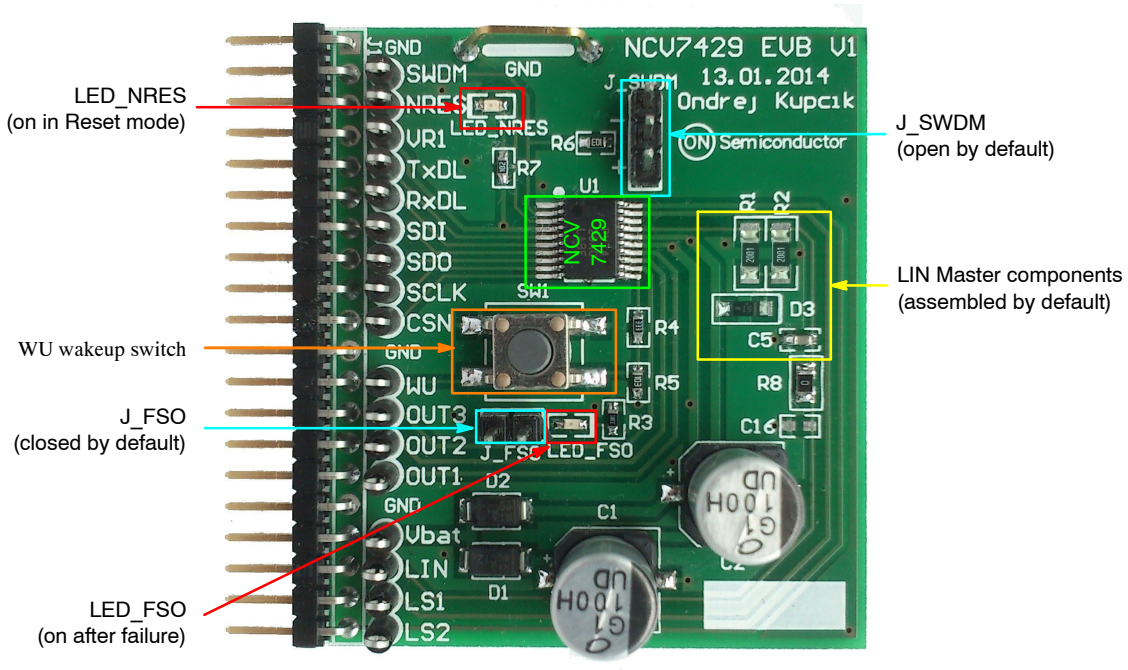

Figure 3. NCV7429 Evaluation Board Description

External Board Connections

For basic evaluations without watchdog services, the board may operate in the Software Development Mode (Figure 4). If the Vbat supply source does not provide fast startup (C1 and C2 capacitors have to be charged), the Software Development mode may not be entered properly. In this case, external power supply (> 10 V) for SWDM input is preferred.

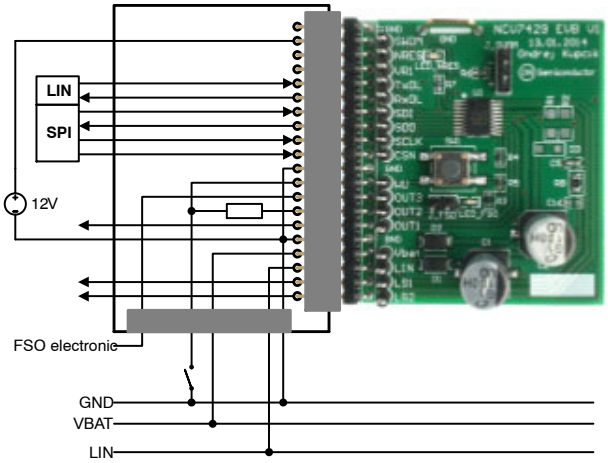

Figure 4. Example of Simplified NCV7429 Evaluation Setup (Software Development mode used)

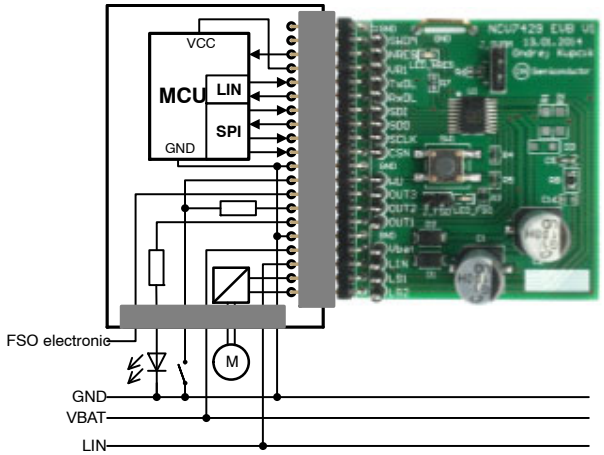

Figure 5. Example of NCV7429 Full Evaluation Setup

FUNCTIONAL DESCRIPTION

Vbat Supply Input

VS and VS_OUT pins of NCV7429 are typically connected to the car battery through reverse−protection diodes and can be exposed to all relevant automotive disturbances (ISO7637 pulses, system ESD ...). VS supplies mainly the control logic and integrated LIN transceiver, while VS_OUT supplies LS1/2 low−side drivers, OUT1−3 high−side drivers and WU wakeup circuitry. The evaluation boards provides split VS and VS_OUT into individual supply paths, which helps covering battery line drop−outs, when the outputs functionality can be affected by the under−voltage, but the MCU has to be still running.

VR1 Low−drop Regulator

An integrated low−drop regulator provides a 5 V supply VR1 to external loads, typically microcontroller.

VR1 voltage level is monitored by an under−voltage detector with multiple thresholds:

- Comparison with SPI−selectable threshold *VR1_RESx*. By default, the highest threshold (typ. 4.5 V) applies for the state machine control and the activation of the NRES signal (LED_NRES on).
- VR1 is compared with a fixed threshold *Vfail_VR1* (typ. 2 V). If VR1 stays below *Vfail_VR1* level for longer than *Tshort_VR1* (typ. 40 ms) in the Init phase, a VR1 short−circuit is detected, SPI flag VR1_FAIL is set and Fail−safe mode entered (OUT3/FSO on, if enabled). In other modes with VR1 active, any under−voltage longer than Tfail_VR1 is flagged into VR1_FAIL, but the Fail−safe mode is not entered.

LIN Transceiver

The NCV7429 on−chip LIN transceiver is an interface between a physical LIN bus and the LIN protocol controller. It is compatible to LIN2.x and J2602 specifications. The LIN is supplied solely from the VS pin and its state linked to the device operating states controlled via SPI. The LIN transceiver is enabled in the Software Development mode.

High−Side Drivers

High−side drivers OUT1−OUT3 are designed to supply mainly LED‘s or switches (for cyclic monitoring).

In the Normal mode, they can be set to one of the following states via the corresponding SPI bits:

- Driver is off in all modes (default)
- Driver is on in all modes, except Fail−safe mode
- Driver is activated periodically in all modes, except Fail−safe mode. Periodical activation can be used, for example, for LED flashing or cyclic contact monitoring
- Driver is controlled by the on−chip PWM controller in all modes, except Fail−safe mode

All OUTx outputs are protected by the following features:

- Over−current protection and current limitation
- Under−load detection
- Thermal protection
- VS_OUT under−/over−voltage protection

Ceramic capacitors (C11−13) on the outputs are recommended in case the drivers supply external loads. They improve EMC and ESD performance of the drivers.

Low−Side Drivers

NCV7429 offers two low−side drivers LS1 and LS2 primarily intended to drive relays.

For the relay demagnetization, LS1/2 drivers feature active flyback clamps towards ground (no diode to VS_OUT) allowing to keep the load off even under a load−dump condition on VS_OUT. Alternatively, LS1/2 can drive LED‘s or other loads.

Ceramic capacitors (C14/15) on the outputs are recommended in case the drivers supply external loads. They improve EMC and ESD performance of the drivers.

LS1/2 can be configured in one of the following states:

- Off in all modes (default)
- On in the Normal mode; off in all other modes
- Controlled by individual PWM in the Normal mode; off in all other modes. If a relay is connected to the output, this setting should not be used.

LS1/2 outputs are protected by the following features:

- Over−current protection and current limitation
- Thermal protection
- VS_OUT under−/over−voltage protection

Operating Status

NCV7429 provides four basic static operating modes and additional transition states − see NCV7429 datasheet available at www.onsemi.com.

For initial evaluation, a Software Development Mode can be entered. This mode equals to a Normal mode (VR1 and LIN enabled by default) while the only difference is that the watchdog does not need to be served. The Software Development mode is entered, if SWDM pin is high (typ. Above 8.5 V) after a power−up (in Init phase) or SWDM pin sampling is requested via SPI.

PCB DRAWINGS

Assembly Drawings

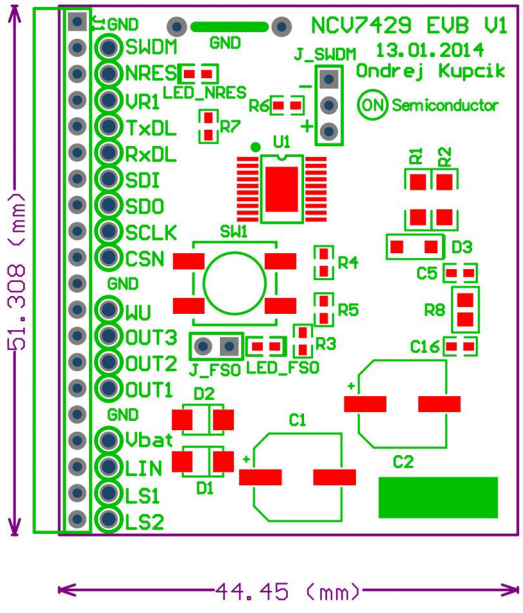

Figure 6. NCV7429 EVB PCB Top Assembly Drawing

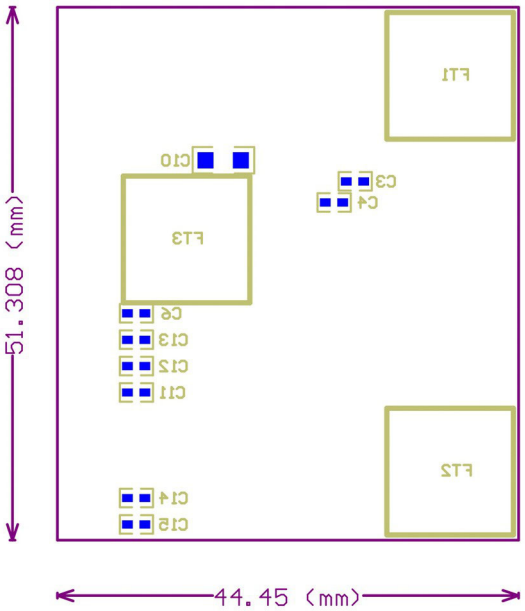

Figure 7. NCV7429 EVB PCB Bottom Assembly Drawing

Composite Drawings

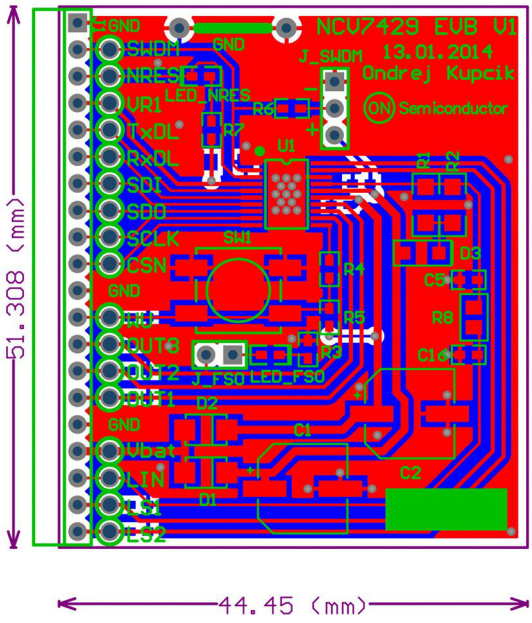

Figure 8. NCV7429 EVB PCB Top Composite Drawing

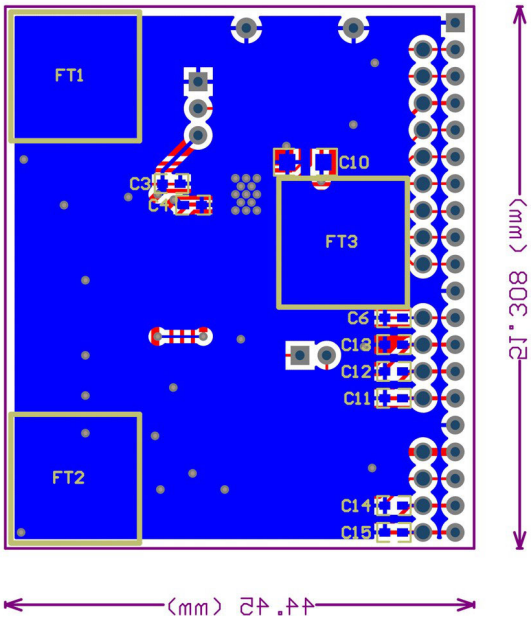

Figure 9. NCV7429 EVB PCB Bottom Composite Drawing (Bottom view)

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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