EVBUM2625

50 W LED Driver with Ultra-Wide Output Voltage Range at Universal Line

ON Semiconductor®

www.onsemi.com

EVAL BOARD USER'S MANUAL

Evaluation Board Overview

This user guide supports the evaluation kit for the FL7733. It should be used in conjunction with the FL7733 datasheet as well as ON Semiconductor's application notes and technical support team. Please visit ON Semiconductor website at www.onsemi.com.

INTRODUCTION

This document describes a solution for an universal AC input voltage LED driver using the FL7733 Primary−Side Regulation (PSR) single−stage controller. The input voltage range is 90 V_{RMS} ~ 277 V_{RMS} and there is one DC output with a constant current of 1.0 A at 50 V. This document contains a general description of the FL7733, the power supply solution specification, schematic, bill of materials, and typical operating characteristics.

General Description of FL7733

The FL7733 is an active Power Factor Correction (PFC) controller for use in single−stage flyback topology or buck−boost topology. Primary−side regulation and single−stage topology minimize cost by reducing external components such as the input bulk capacitor and secondary side feedback circuitry. To improve power factor and Total Harmonic Distortion (THD), constant on−time control is utilized with an internal error amplifier and a low bandwidth compensator. Precise constant−current control provides accurate output current, independent of input voltage and output voltage. Operating frequency is proportionally changed by the output voltage to guarantee Discontinuous Current Mode (DCM) operation, resulting in high efficiency and simple designs. The FL7733 also provides open−LED, short−LED, and over−temperature protection functions.

Controller Features

High Performance

- Cost−Effective Solution: Doesn't Require Input Bulk Capacitor and Secondary−Side Feedback Circuitry
- Power Factor Correction
- THD <10% Over Universal Line Range
- CC Tolerance:
  < ±1% by Universal Line Voltage Variation
  < ±1% by 50% ~ 100% Load Voltage Variation
  < ±1% by ±20% Magnetizing Inductance Variation
- High−Voltage Startup with V_{DD} Regulation
- Adaptive Feedback Loop Control for Startup without Overshoot

High Reliability

- LED Short / Open Protection
- Output Diode Short Protection
- Sensing Resistor Short / Open Protection
- V_{DD} Over−Voltage Protection (OVP)
- V_{DD} Under−Voltage Lockout (UVLO)
- Over−Temperature Protection (OTP)
- All Protections by Auto Restart
- Cycle−by−Cycle Current Limit
- Application Voltage Range: 80 V_{AC} ~ 308 V_{AC}

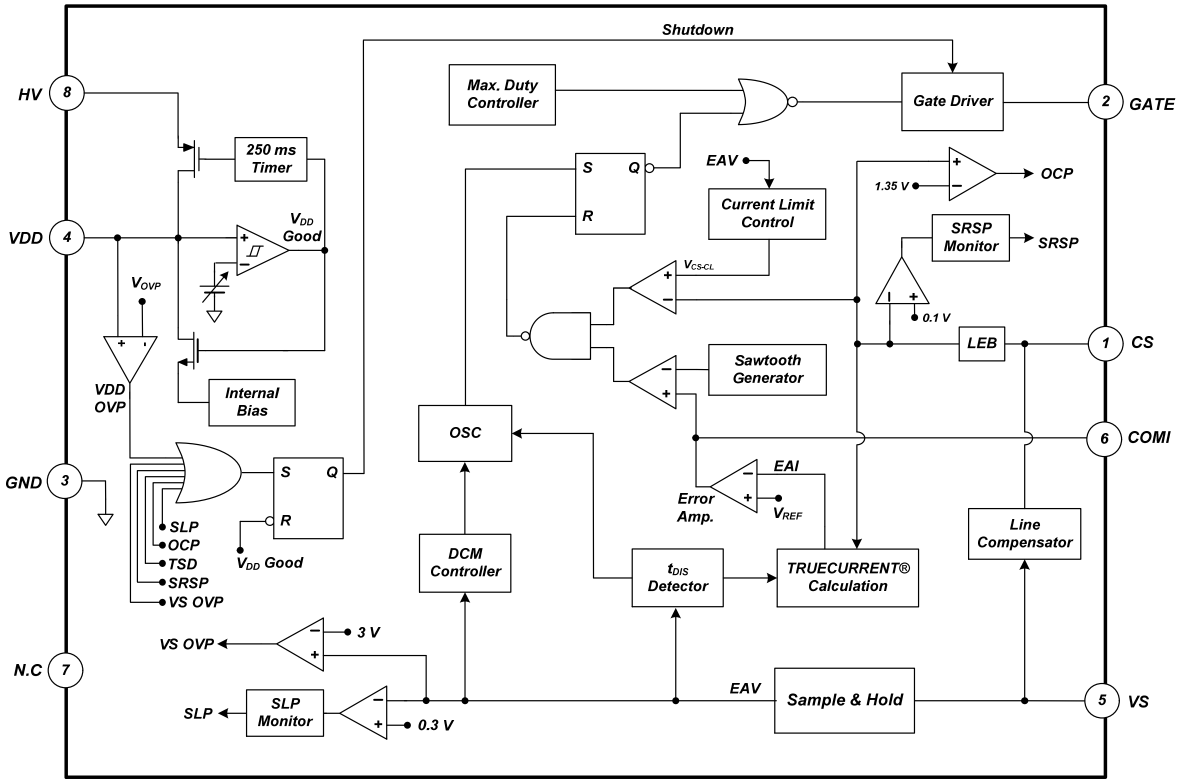

Figure 1. Block Diagram of MT9S6NNV01−LVDS Adapter Board

Evaluation Board Specifications

Table 1. SPECIFICATIONS FOR LED LIGHTING LOAD

Description		Symbol	Value	Comments
Input	**Voltage**	$V_{IN.MIN}$	90 V_{AC}	Minimum AC Input Voltage
		$V_{IN.MAX}$	277 V_{AC}	Maximum AC Input Voltage
		$V_{IN.NOMINAL}$	120 V / 230 V	Nominal AC Input Voltage
	Frequency	f_{IN}	60 Hz / 50 Hz	Line Frequency
Output	**Voltage**	$V_{OUT.MIN}$	7 V	Minimum Output Voltage
		$V_{OUT.MAX}$	55 V	Maximum Output Voltage
		$V_{OUT.NOMINAL}$	50 V	Nominal Output Voltage
	Current	$I_{OUT.NOMINAL}$	1.0 A	Nominal Output Current
		CC Deviation	< ±0.85%	Line Input Voltage Change: 90~277 V_{AC}
			< ±1.75%	Output Voltage Change: 7~55 V
	Description	Symbol	Value	Comments
Efficiency		Eff_{90VAC}	87.56%	Efficiency at 90 V_{AC} Input Voltage
		Eff_{120VAC}	88.96%	Efficiency at 120 V_{AC} Input Voltage
		Eff_{140VAC}	89.49%	Efficiency at 140 V_{AC} Input Voltage
		Eff_{180VAC}	90.13%	Efficiency at 180 V_{AC} Input Voltage
		Eff_{230VAC}	90.31%	Efficiency at 230 V_{AC} Input Voltage
		Eff_{277VAC}	90.26%	Efficiency at 277 V_{AC} Input Voltage
PF / THD		PF /THD_{90VAC}	0.997 / 3.36%	PF/THD at 90 V_{AC} Input Voltage
		PF / THD_{120VAC}	0.992 / 3.55%	PF/THD at 120 V_{AC} Input Voltage
		PF / THD_{140VAC}	0.987 / 3.60%	PF/THD at 140 V_{AC} Input Voltage
		PF / THD_{180VAC}	0.975 / 4.44%	PF/THD at 180 V_{AC} Input Voltage
		PF / THD_{230VAC}	0.944 / 5.36%	PF/THD at 230 V_{AC} Input Voltage
		PF / THD_{277VAC}	0.902 / 6.88%	PF/THD at 277 V_{AC} Input Voltage
Temperature	**FL7733**	T_{FL7733}	57.9°C	Open−Frame Condition (T_A = 25°C) FL7733 Temperature
	Primary MOSFET	T_{MOSFET}	66.1°C	Primary MOSFET Temperature
	Secondary Diode	T_{DIODE}	65.2°C	Secondary Diode Temperature
	Bridge Diode	$T_{BRG−DIODE}$	60.1°C	Bridge Diode Temperature

1. All data of the evaluation board measured with the board was enclosed in a case and external temperature around T_A = 25°C

EVALUATION BOARD PHOTOGRAPHS

Dimensions: 168 mm (L) x 35 mm (W) x 25 mm (H)

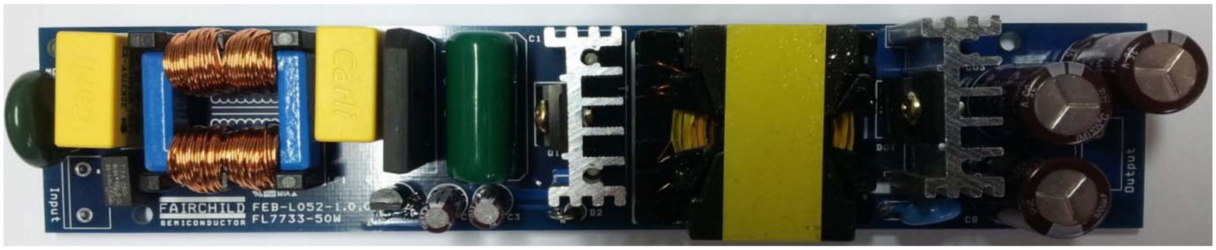

Figure 2. Top View

Figure 3. Bottom View

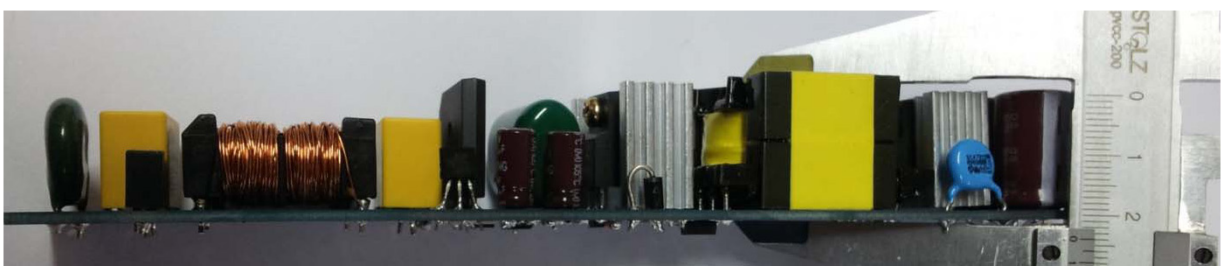

Figure 4. Side View

EVALUATION BOARD PRINTED CIRCUIT BOARD (PCB)

Unit: mm

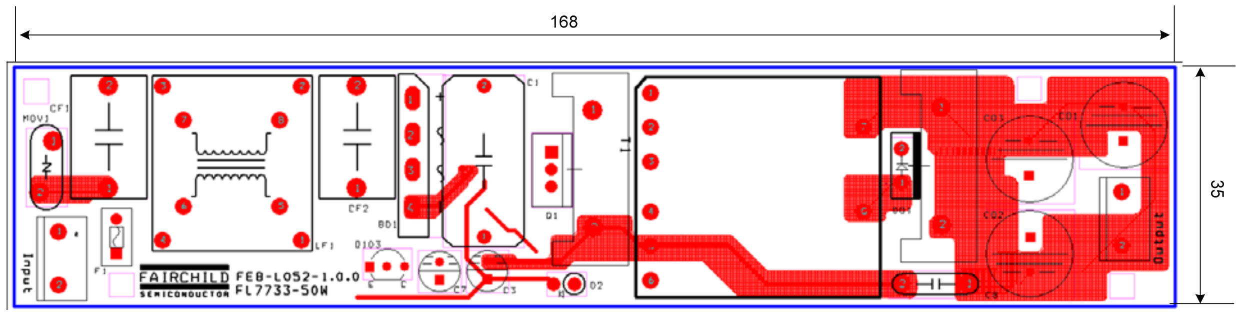

Figure 5. Top Pattern

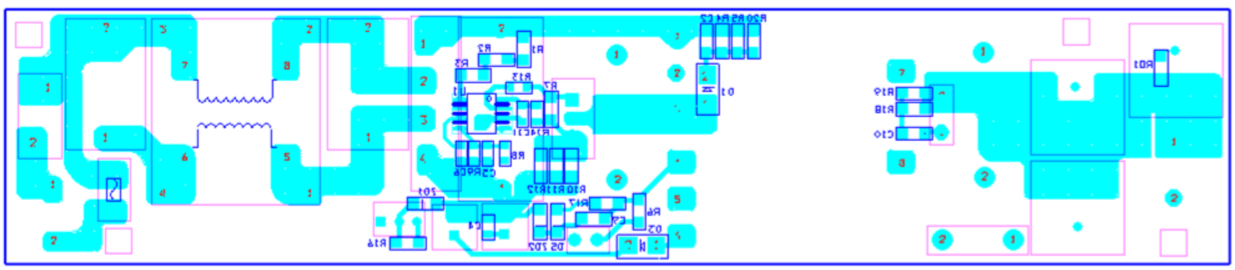

Figure 6. Bottom Pattern

EVALUATION BOARD SCHEMATIC

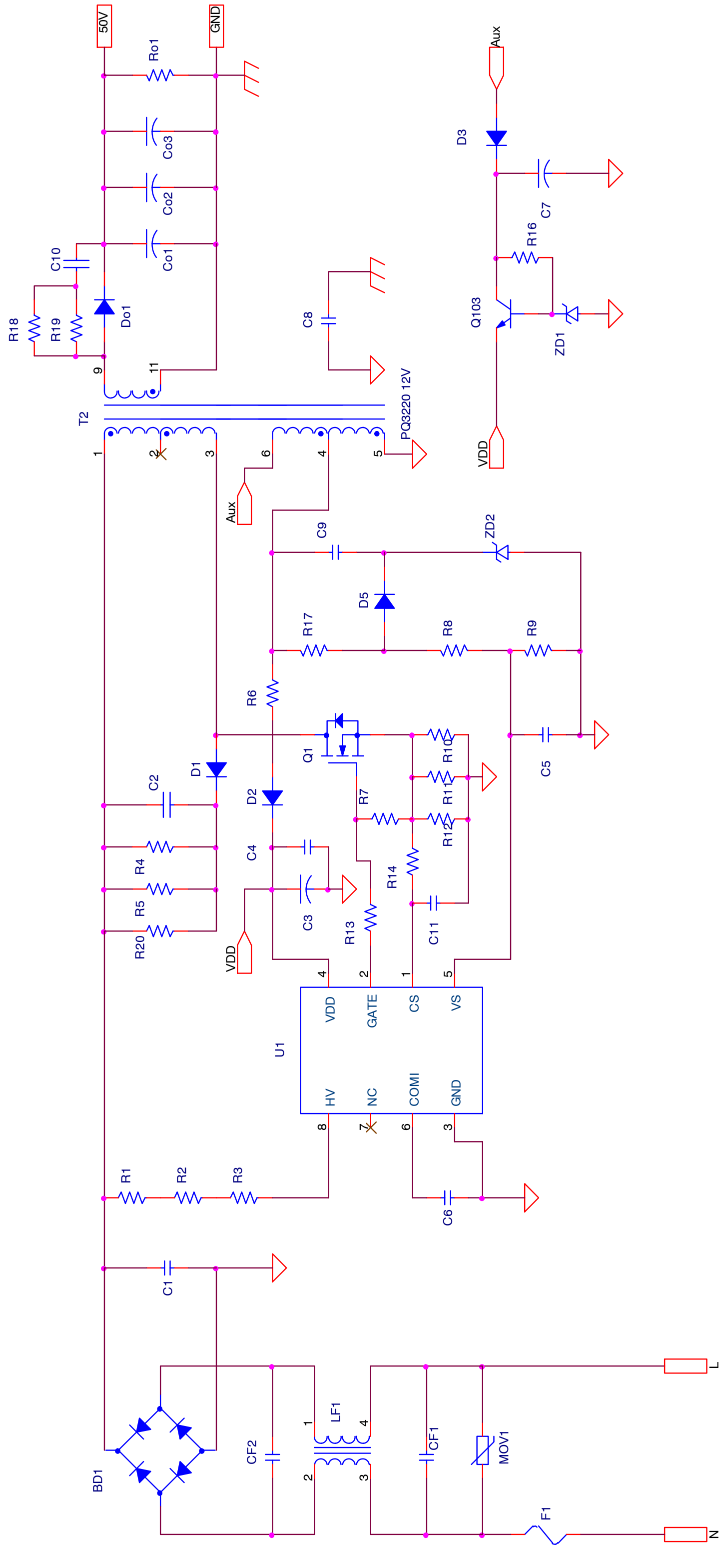

Figure 7. Schematic

Table 2. EVALUATION BOARD BILL OF MATERIALS

Item No.	Part Reference	Part Number	Qty.	Description	Manufacturer
1	BD1	G3SBA60	1	2.3 A / 600 v, Bridge Diode	Vishay
3	CF1	MPX AC275 V 474K	1	470 nF / 275 V_{AC}, X−Capacitor	Carli
3	CF2	MPX AC275 V 224K	1	220 nF / 275 V_{AC}, X−Capacitor	Carli
4	Co1, Co2, Co3	KMG 470 μF / 63 V	3	470 μF / 63 V, Electrolytic Capacitor	Samyoung
5	C1	MPE 630 V 334K	1	330 nF / 630 V, MPE film Capacitor	Sungho
6	C2	C1206C103KDRACTU	1	10 nF / 1 KV, SMD Capacitor 1206	Kemet
7	C3	KMG 10 μF / 35 V	1	10 μF / 35 V, Electrolytic Capacitor	Samyoung
8	C4	C0805C104K5RACTU	1	100 nF / 50 V, SMD Capacitor 2012	Kemet
9	C5	C0805C519C3GACTU	1	5.1 pF / 25 V, SMD Capacitor 2012	Kemet
10	C6	C0805C105J3RACTU	1	1 μF / 25 V, SMD Capacitor 2012	Kemet
11	C7	KMG 22 μF / 100 V	1	22 μF / 100 V, Electrolytic Capacitor	Samyoung
12	C8	SCFz2E472M10BW	1	4.7 nF / 250 V, Y−Capacitor	Samwha
13	C9	C1206C331KCRACTU	1	330 pF / 500 V, SMD Capacitor 1206	Kemet
14	C10	C1206C221KCRACTU	1	220 pF / 500 V, SMD Capacitor 1206	Kemet
15	C11	C0805C101K3GACTU	1	100 pF / 25 V, SMD Capacitor 0805	Kemet
16	Do1	FFPF08H60S	1	600 V / 8 A, Hyperfast Rectifier	ON Semiconductor
17	D1, D3	RS1M	2	1000 V / 1 A, Ultra−Fast Recovery Diode	ON Semiconductor
18	D2	1N4003	1	200 V / 1 A, General Purpose Rectifier	ON Semiconductor
19	D5	LL4148	1	100 V / 0.2 A, Small Signal Diode	ON Semiconductor
20	F1	250 V / 2 A	1	250 V / 2 A, Fuse	Bussmann
21	LF1	B82733F	1	40 mH Common Inductor	EPICO
22	MOV1	SVC471D−10A	1	Metal Oxide Varistor	Samwha
23	Q1	FCPF400N80Z	1	800 V / 400 mΩ, N−Channel MOSFET	ON Semiconductor
24	Q103	KSP42	1	High Voltage Transistor	ON Semiconductor
25	Ro1	RC1206JR−0727KL	1	27 kΩ, SMD Resistor 1206	Yageo
26	R1, R7	RC1206JR−0710KL	2	10 kΩ, SMD Resistor 1206	Yageo
27	R2, R3	RC1206JR−0715KL	2	15 kΩ, SMD Resistor 1206	Yageo
28	R4, R5, R20	RC1206JR−07100KL	3	100 kΩ, SMD Resistor 1206	Yageo
29	R6	RC1206JR−0710RL	1	10 Ω, SMD Resistor 1206	Yageo
30	R8	RC0805JR−07160KL	1	160 kΩ, SMD Resistor 0805	Yageo
31	R9	RC0805JR−0751KL	1	51 kΩ, SMD Resistor 0805	Yageo
32	R10	RC1206JR−070R2L	1	0.2 Ω, SMD Resistor 1206	Yageo
33	R11, R12	RC1206JR−073RL	2	3 Ω, SMD Resistor 1206	Yageo
34	R13	RC0805JR−0710RL	1	10 Ω, SMD Resistor 0805	Yageo
35	R14	RC0805JR−07510RL	1	510 Ω, SMD Resistor 0805	Yageo
36	R16	RC1206JR−0730KL	1	30 kΩ, SMD Resistor 1206	Yageo
37	R17	RC1206JR−071K2L	1	1.2 kΩ, SMD Resistor 1206	Yageo
38	R18, R19	RC1206JR−0730RL	2	30 Ω, SMD Resistor 1206	Yageo

39	T1	PQ3220	1	PQ Core, 12−Pin Transformer	TDK
40	U1	FL7733	1	Main PSR Controller	ON Semiconductor
41	ZD1	MM5Z15V	1	15 V Zener Diode	ON Semiconductor
42	ZD2	MM5Z10V	1	10 V Zener Diode	ON Semiconductor

TRANSFORMER DESIGN

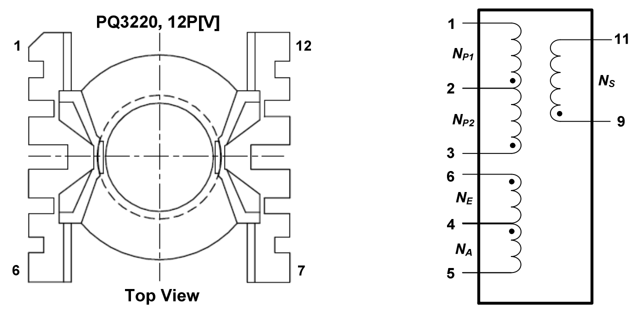

Figure 8. Transformer PQ3220's Bobbin Structure and Pin Configuration

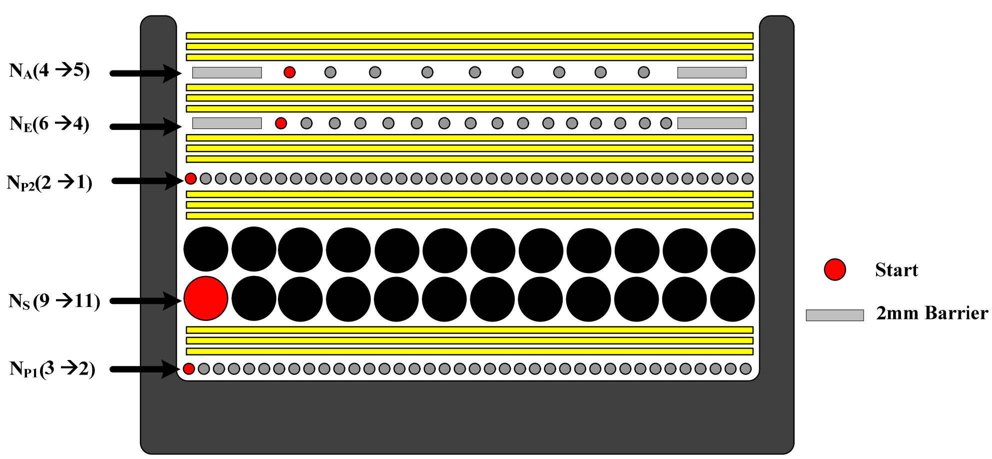

Figure 9. Transformer Winding Structure

Table 3. WINDING SPECIFICATIONS

No	Winding	Pin (S → F)	Wire	Turns	Winding Method
1	N_{P1}	3 → 2	0.45 ψ	17 Ts	Solenoid Winding
2	Insulation: Polyester Tape t = 0.025 mm, 3−Layer				
3	N_S	9 → 11	0.7 ψ (TIW)	19 Ts	Solenoid Winding
4	Insulation: Polyester Tape t = 0.025 mm, 3−Layer				
5	N_{P1}	2 → 1	0.45 ψ	11 Ts	Solenoid Winding
	Insulation: Polyester Tape t = 0.025 mm, 3−Layer				
6	N_E	6 → 4	0.25 ψ	16 Ts	Solenoid Winding
7	Insulation: Polyester Tape t = 0.025 mm, 3−Layer				
8	N_A	4 → 5	0.25 ψ	8 Ts	Solenoid Winding
9	Insulation: Polyester Tape t = 0.025 mm, 3−Layer				

Table 4. ELECTRICAL CHARACTERISTICS

	Pin	Specifications	Remark
Inductance	1–3	160 μH ± 10%	60 kHz, 1 V
Leakage	1–3	5 μH	60 kHz, 1 V, Short All Output Pins

EVALUATION BOARD PERFORMANCE

Table 5. TEST CONDITION & EQUIPMENT LIST

Ambient Temperature	T_A = 25°C
Test Equipment	AC Power Source: PCR500L by Kikusui Power Analyzer: PZ4000000 by Yokogawa Electronic Load: PLZ303WH by KIKUSUI Multi Meter: 2002 by KEITHLEY, 45 by FLUKE Oscilloscope: 104Xi by LeCroy Thermometer: Thermal CAM SC640 by FLIR SYSTEMS LED: EHP−AX08EL/GT01H−P03 (3 W) by Everlight

Startup

Figure 10 and Figure 11 show the overall startup performance at rated output load. The output load current starts flowing after about 0.2 s and 0.1 s for input voltage 90 V_{AC} and 277 V_{AC} condition upon AC input power switch turns on; CH1: V_{DD} (10 V / div), CH2: V_{IN} (100 V / div), CH3: V_{LED} (20 V / div), CH4: I_{LED} (500 A / div), Time Scale: (100 ms / div), Load: 2 parallel * 18 series−LEDs.

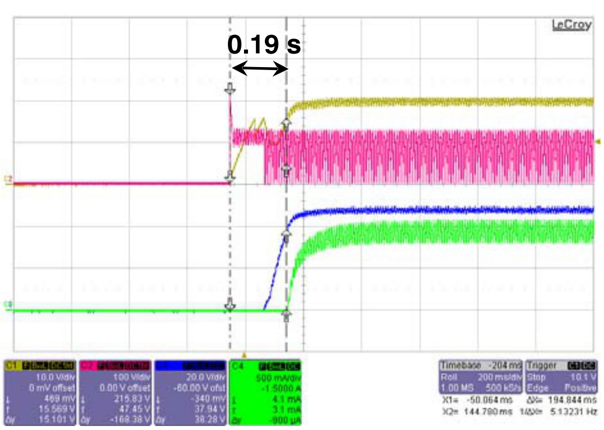

Figure 10. V_{IN} = 90 V_{AC} / 60 Hz

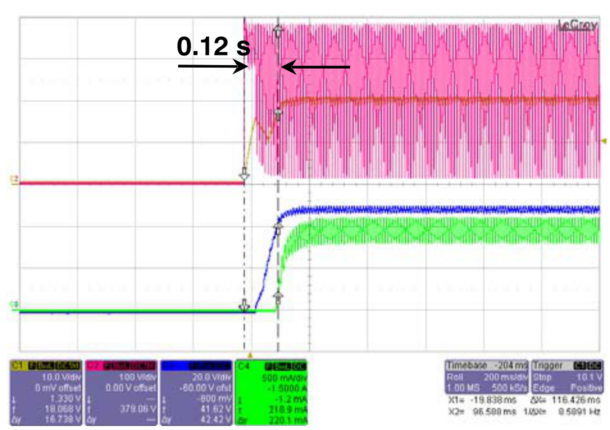

Figure 11. V_{IN} = 277 V_{AC} / 50 Hz

Operation Waveforms

Figure 12 to Figure 15 show AC input and output waveforms at rated output load. CH1: I_{IN} (1.00 A / div), CH2: V_{IN} (100 V / div), CH3: V_{LED} (20 V / div), CH4: I_{LED} (500 mA / div), Time Scale: (5 ms / div), Load: 2 parallel * 18 series−LEDs.

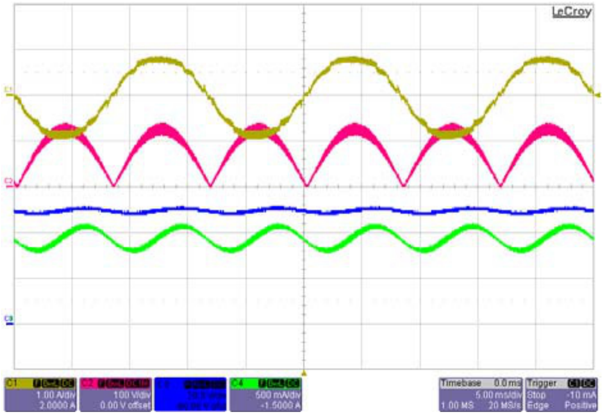

Figure 12. V_{IN} = 90 V_{AC} / 60 Hz

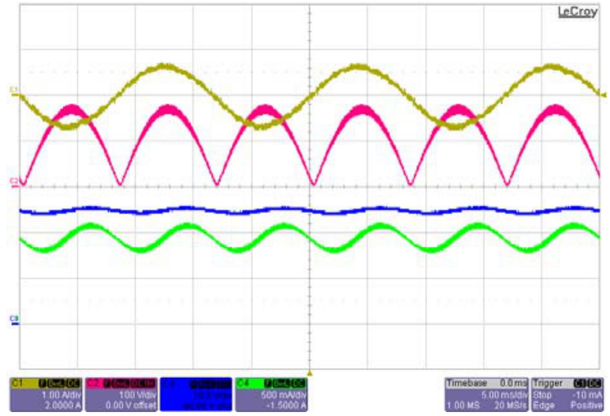

Figure 13. V_{IN} = 120 V_{AC} / 60 Hz

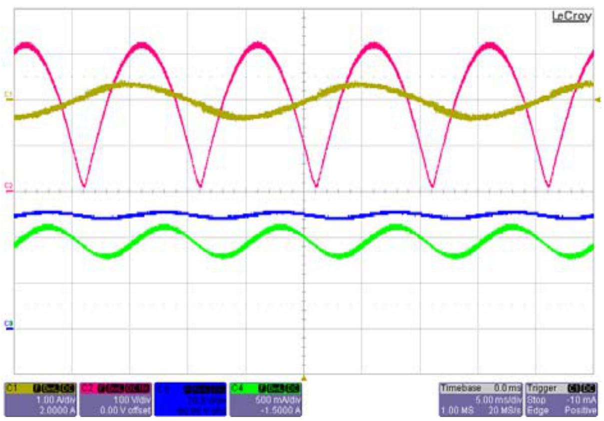

Figure 14. V_{IN} = 230 V_{AC} / 50 Hz

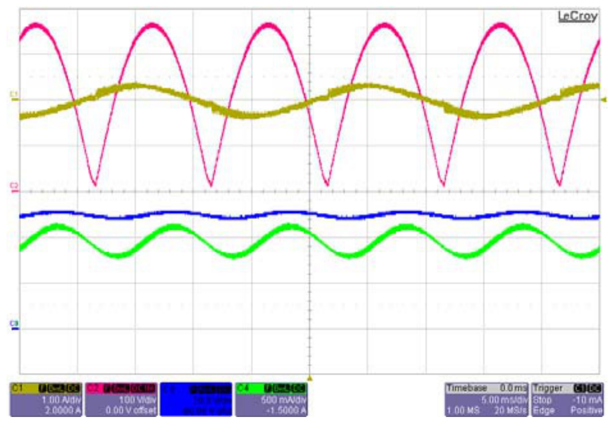

Figure 15. V_{IN} = 277 V_{AC} / 50 Hz

Figure 16 to Figure 19 show key waveforms of single−stage flyback converter operation for line voltage at rated output load. CH1: I_{DS} (2.00 A / div), CH2: V_{DS} (200 V / div), CH3: $V_{SEC-Diode}$ (200 V / div), CH4: $I_{SEC-Diode}$ (5.00 A / div), Load: 2 parallel * 18 series−LEDs.

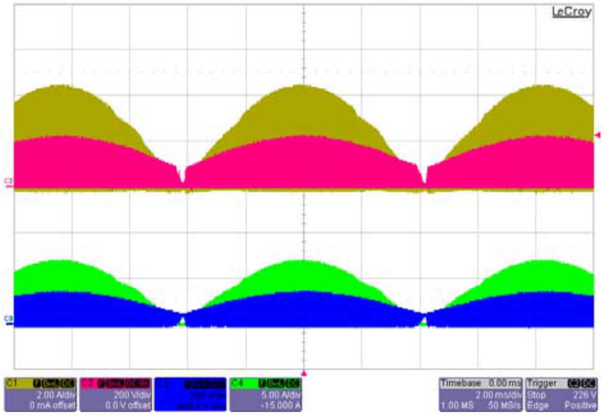

Figure 16. V_{IN} = 90 V_{AC} / 60 Hz, [2.0 ms/ div]

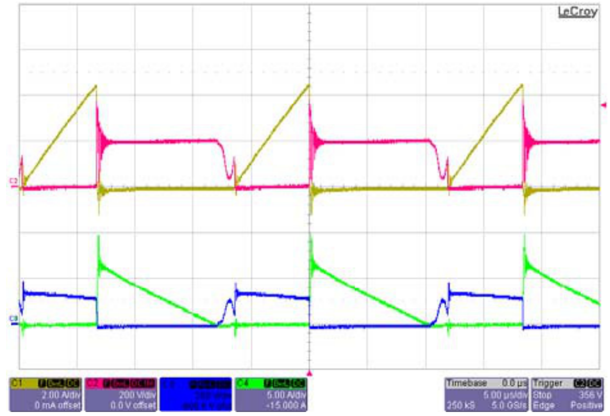

Figure 17. V_{IN} = 90 V_{AC} / 60 Hz, [5.0 μs/ div]

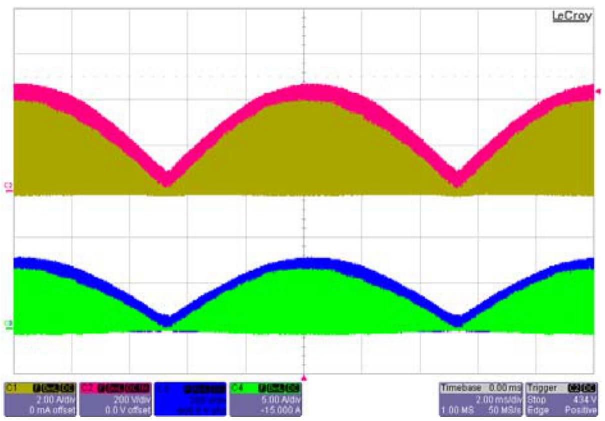

Figure 18. V_{IN} = 277 V_{AC} / 60 Hz, [2.0 ms/ div]

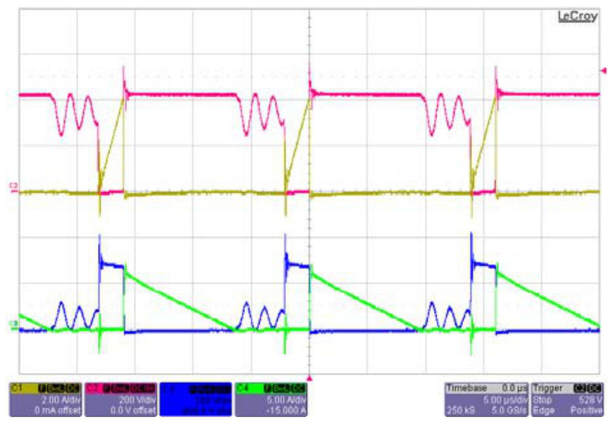

Figure 19. V_{IN} = 277 V_{AC} / 60 Hz, [5.0 μs/ div]

Constant−Current Regulation

The output current deviation for wide output voltage ranges from 7 V to 55 V is less than ±1.75 % at each line voltage. Line regulation at the output voltage (52 V) is also less than ±0.85%. The results were measured with E−load [CR Mode].

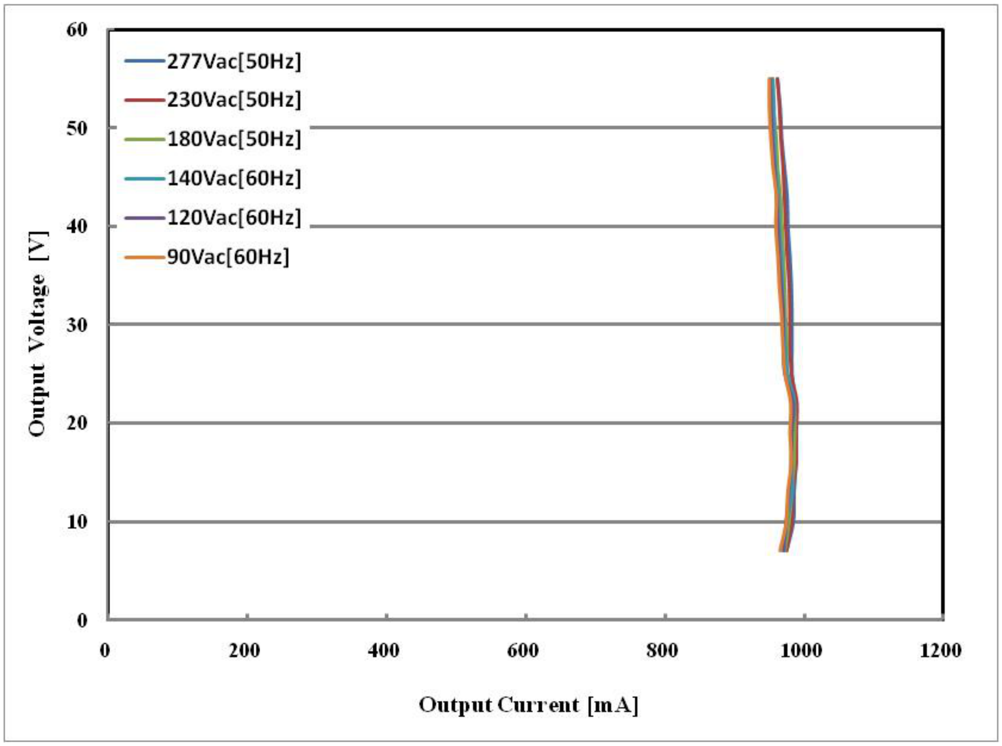

Figure 20. Constant−Current Regulation

Table 6. CONSTANT−CURRENT REGULATION BY OUTPUT VOLTAGE CHANGE (7 ~ 55)

Input Voltage	Min. Current [mA]	Max. Current [mA]	Tolerance
90 V_{AC} [60 Hz]	950	981	±1.61%
120 V_{AC} [60 Hz]	951	984	±1.71%
140 V_{AC} [60 Hz]	955	986	±1.60%
180 V_{AC} [50 Hz]	955	986	±1.60%
230 V_{AC} [50 Hz]	961	989	±1.44%
277 V_{AC} [50 Hz]	961	988	±1.39%

Table 7. CONSTANT−CURRENT REGULATION BY LINE VOLTAGE CHANGE (90 ~ 277 V_{AC})

Output Voltage	90 V_{AC} [60 Hz]	120 V_{AC} [60 Hz]	140 V_{AC} [60 Hz]	180 V_{AC} [50 Hz]	230 V_{AC} [50 Hz]	277 V_{AC} [50 Hz]	Tolerance
55 V	950 mA	951 mA	957 mA	955 mA	961 mA	961 mA	±0.58%
52 V	950 mA	952 mA	957 mA	956 mA	964 mA	965 mA	±0.78%
46 V	955 mA	957 mA	963 mA	962 mA	969 mA	971 mA	±0.83%

V_S Circuits for Wide Output

The first consideration for R1, R2, and R3 selection is to set V_S to 2.45 V to ensure high− frequency operation at the rated output power.

The second consideration is V_S blanking. The output voltage is detected by auxiliary winding and a resistive divider connected to the VS pin, as shown in Figure 21. However, in a single−stage flyback converter without a DC link capacitor, auxiliary winding voltage cannot be clamped to reflected output voltage at low line voltage due to the small Lm current, which induces V_S voltage−sensing error. Frequency decreases rapidly at the zero− crossing point of line voltage, which can cause LED light flicker. To maintain constant frequency over the whole sinusoidal line voltage, V_S blanking disables V_S sampling at less than a particular line voltage $V_{IN.bnk}$ by sensing the auxiliary winding.

The third consideration is V_S level, which should be operated between 0.6 V and 3 V to avoid triggering SLP and V_S OVP in wide output application. V_S level can be maintained using additional V_S circuits, as shown in Figure 21.

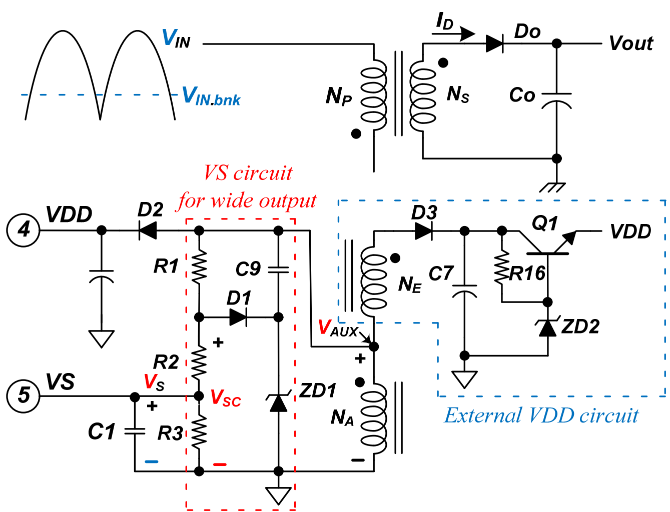

Figure 21. External Circuitry for System Operation in Wide Output Voltage Ranges

Considering the maximum switching frequency up to 50% of maximum output voltage, Zener diode and R1, R2, and R3 are obtained as:

$$V_{ZD1} < (V_{DD.OVP} \times 0.5) - V_{F.D1} \quad \text{(eq. 1)}$$

Where $V_{F.D1}$ is the forward voltage of D1 connected in series with Zener diode ZD1.

Considering Zener diode voltage regulation and its power rating, R1 can be selected to limit the Zener diode current I_{ZD1} to 10 mA maximum, such as:

$$R1 = \frac{(V_{DD.OVP} - V_{SC})}{10\ mA} = 1.2\ k\Omega \quad \text{(eq. 2)}$$

Where V_{SC} is voltage clamped by D1 and ZD1.

$$R2 = n_{AP} \times \frac{V_{IN.bnk}}{I_{VS.bnk}} - R1 \quad \text{(eq. 3)}$$

Where $V_{IN.bnk}$ and $I_{VS.bnk}$ line voltage level and V_S current for V_S blanking, respectively.

$$R3 \geq \frac{R2 \times 2.45}{V_{SC} - 2.45} \quad \text{(eq. 4)}$$

Additional consideration in V_S circuits for wide output voltage range is t_{DIS} delay, which is caused by the voltage difference when the V_{AUX} across auxiliary winding is clamped to V_{SC}, as shown in Figure 22. This delay lasts until V_{AUX} is at the same level as V_{SC} and may affect constant output current regulation. It can be removed by capacitor C9 connected between auxiliary winding and cathode terminal of Zener diode ZD1. The V_{AUX} is divided into capacitor voltage V_{C3} and V_{ZD1} after the MOSFET gate is turned off. Then V_{C3} maintains its voltage without discharging while V_{ZD2} slowly decreases to $V_{AUX} - V_{C3}$ as the output diode current I_D reaches zero. Therefore, V_S can follow V_{AUX}, as shown by the dotted line in Figure 22. C3 should be selected to the proper value depending on resonant frequency determined by the resonance between magnetizing inductance Lm and MOSFET's C_{OSS}. The 330 pF used in this application was selected by trial and error. Its value can be obtained as:

$$C9 = \frac{300\ kHz}{f_t} \cdot 330\ pF \quad \text{(eq. 5)}$$

Where f_r is the resonance frequency determined by the resonance between C_{oss} and L_m.

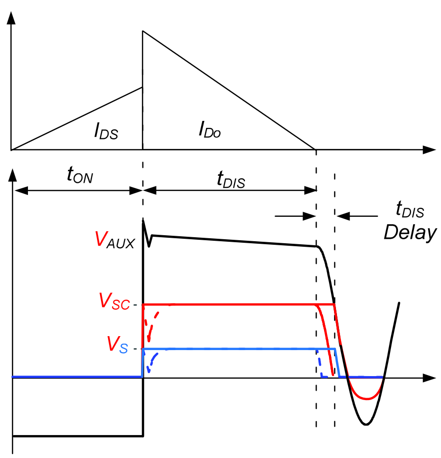

Figure 22. Waveforms in V_s Circuits

V_{DD} Circuit for Wide Output

FL7733's V_{DD} operation range is 8.75 ~ 23 V and UVLO is triggered and shuts down switching if output voltage is lower than $V_{OUT}-V_{UVLO}$ ($8.75 \times N_S / N_A$). Therefore, V_{DD} should be supplied properly without triggering UVLO across the wide output voltage range of 7 ~ 55 V. V_{DD} can be supplied by adding external winding N_E and V_{DD} circuits composed of voltage regulator, as shown in Figure 21. The N_E should be designed so V_{DD} can be supplied without triggering UVLO at minimum output voltage ($V_{min.OUT}$). Therefore, the external winding NE can be determined as follows:

$$N_E > \frac{(8.75 + V_{CE.Q1} + V_{F.D3})}{(V_{V.FDo} + V_{min.OUT})} \times N_S - N_A \quad \text{(eq. 6)}$$

where $V_{CE.Q1}$ is Q1's collector−emitter saturation voltage, $V_{F.D3}$ is D3's forward voltage, and $V_{F.Do}$ is forward voltage of the output diode at minimum output voltage.

Short− / Open−LED Protections

Figure 23 to Figure 26 show the operating waveforms when the LED short protection is triggered and recovered. Once the LED short occurs, SCP is triggered and V_{DD} starts "Hiccup" Mode with JFET regulation times [250 ms]. This lasts until the fault condition is removed. Systems can restart automatically when the output load returns to normal condition. CH1: V_{DD} (10 V / div), CH2: V_{IN} (100 V / div), CH3: V_{GATE} (10 V / div), I_{OUT} (500 mA / div), Time Scale: (1.00 s / div).

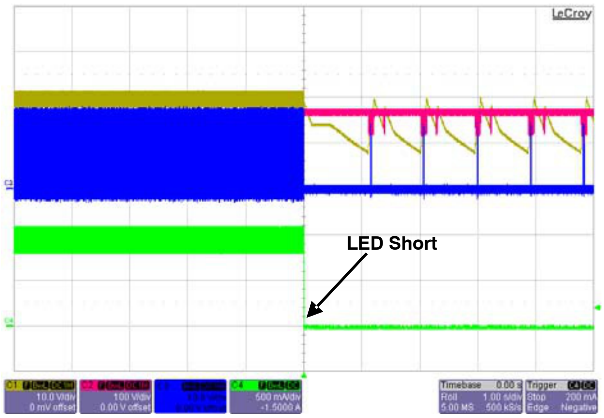

Figure 23. V_{IN} = 120 V_{AC} / 60 Hz, [LED Short]

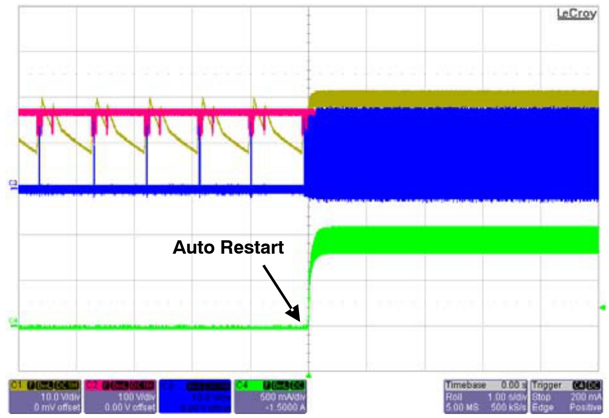

Figure 24. V_{IN} = 120 V_{AC} / 60 Hz, [LED Restore]

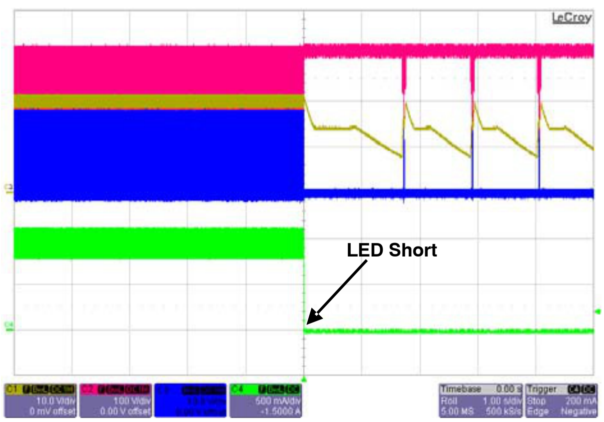

Figure 25. V_{IN} = 230 V_{AC} / 50 Hz, [LED Short]

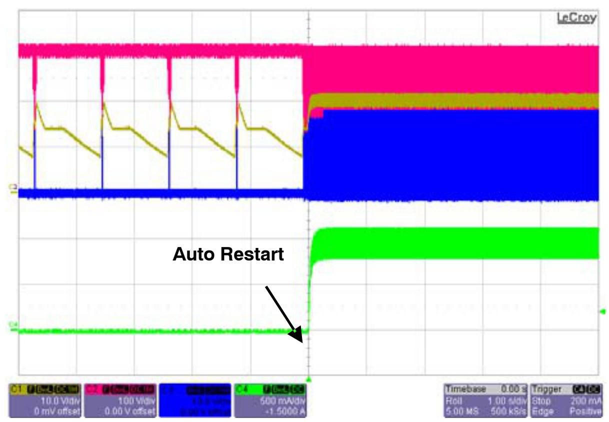

Figure 26. V_{IN} = 230 V_{AC} / 50 Hz, [LED Restore]

Figure 27 to Figure 30 show the operating waveforms when the LED open condition is triggered and recovered. Once the output goes open circuit, V_S OVP or V_{DD} OVP are triggered and V_{DD} starts Hiccup Mode with JFET regulation times [250 ms]. This lasts until the fault condition is eliminated. Systems can restart automatically when returned to normal condition. CH1: V_{DD} (10 V / div), CH2: V_{IN} (100 V / div), CH3: V_{GATE} (10 V / div), V_{OUT} (50 V / div), Time Scale: (1.00 s / div).

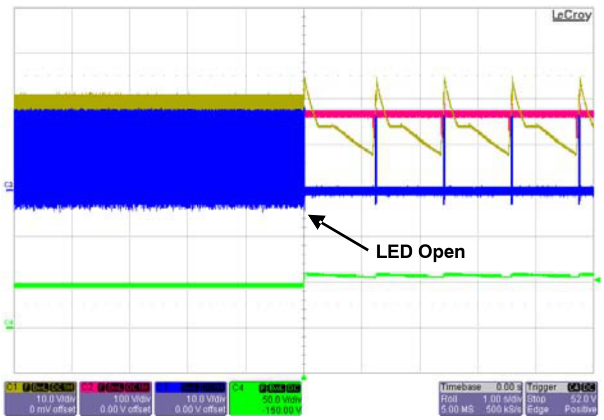

Figure 27. V_{IN} = 120 V_{AC} / 60 Hz, [LED Short]

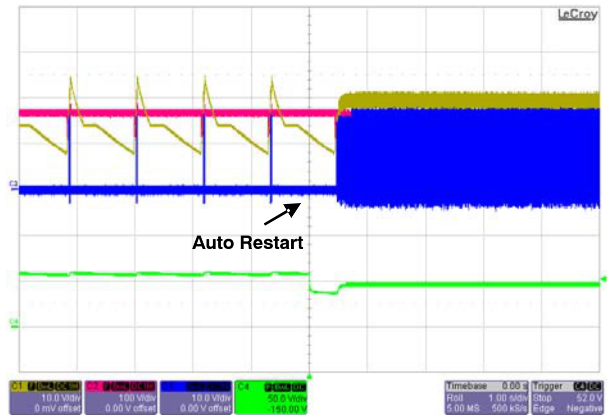

Figure 28. V_{IN} = 120 V_{AC} / 60 Hz, [LED Restore]

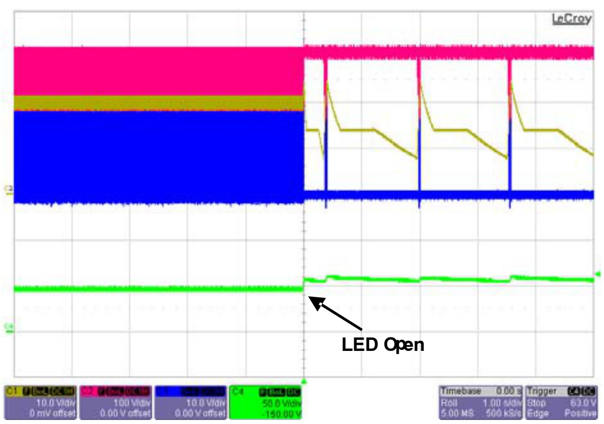

Figure 29. V_{IN} = 230 V_{AC} / 50 Hz, [LED Short]

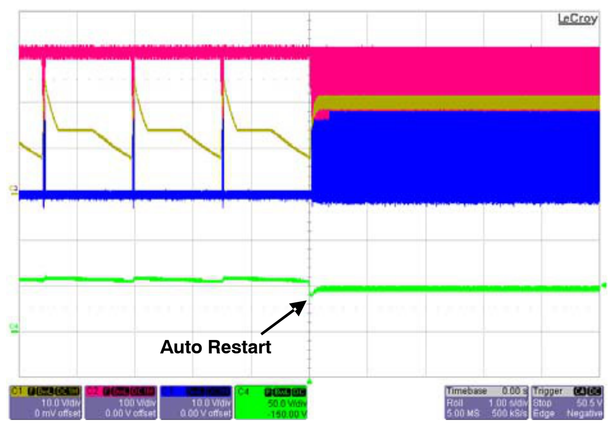

Figure 30. V_{IN} = 230 V_{AC} / 50 Hz, [LED Restore]

NOTE: When the LED is re−connected after open−LED condition, the output capacitor is quickly discharged through the LED load and the inrush current by the discharge could destroy the LED load.

Efficiency

System efficiency is 87.56% ~ 90.81% over input voltages 90 ~ 277 V_{AC}. The results were measured using actual rated LED loads 30 minutes after startup.

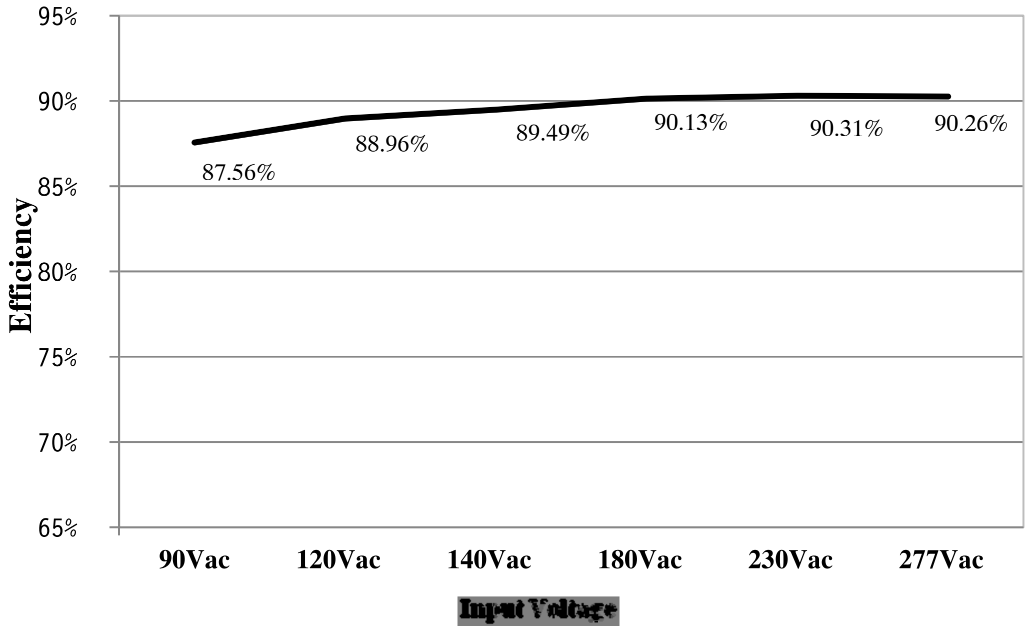

Figure 31. System Efficiency

Table 8. SYSTEM EFFICIENCY

Input Voltage	Input Power (W)	Output Current (A)	Output Voltage (V)	Output Power (W)	Efficiency (%)
90 V_{AC} [60 Hz]	53.68	0.952	49.40	47.00	87.56
120 V_{AC} [60 Hz]	53.18	0.955	49.52	47.31	88.96
140 V_{AC} [60 Hz]	53.05	0.958	49.57	47.47	89.49
180 V_{AC} [50 Hz]	54.43	0.963	50.95	49.06	90.13
230 V_{AC} [50 Hz]	54.66	0.969	50.94	49.36	90.31
277 V_{AC} [50 Hz]	54.78	0.974	50.78	49.44	90.26

Power Factor (PF) & Total Harmonic Distortion (THD)

The FL7733 evaluation board shows excellent THD performance: much less than 10%. The results were measured using actual rated LED loads 10 minutes after startup.

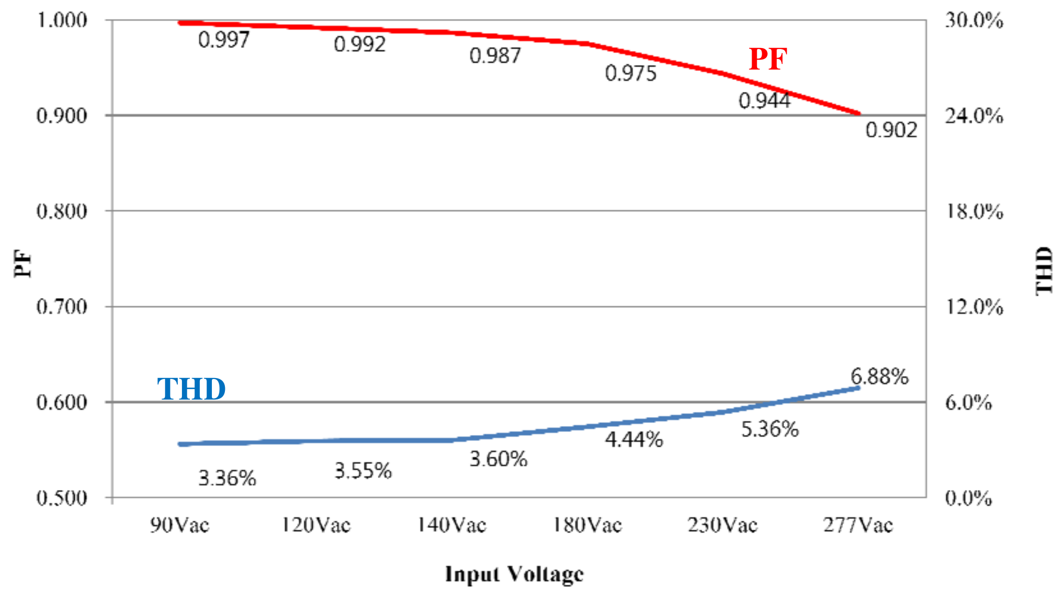

Figure 32. Power Factor & Total Harmonic Distortion

Table 9. POWER FACTOR & TOTAL HARMONIC DISTORTION

Input Voltage	Output Current (A)	Output Voltage (V)	Power Factor	THD (%)
90 V_{AC} [60 Hz]	0.952	49.40	0.997	3.36
120 V_{AC} [60 Hz]	0.955	49.52	0.992	3.55
140 V_{AC} [60 Hz]	0.958	49.57	0.987	3.60
180 V_{AC} [50 Hz]	0.963	50.95	0.975	4.44
230 V_{AC} [50 Hz]	0.969	50.94	0.944	5.36
277 V_{AC} [50 Hz]	0.974	50.78	0.902	6.88

Harmonics

Figure 33 to Figure 36 shows current harmonics measured using actual rated LED loads.

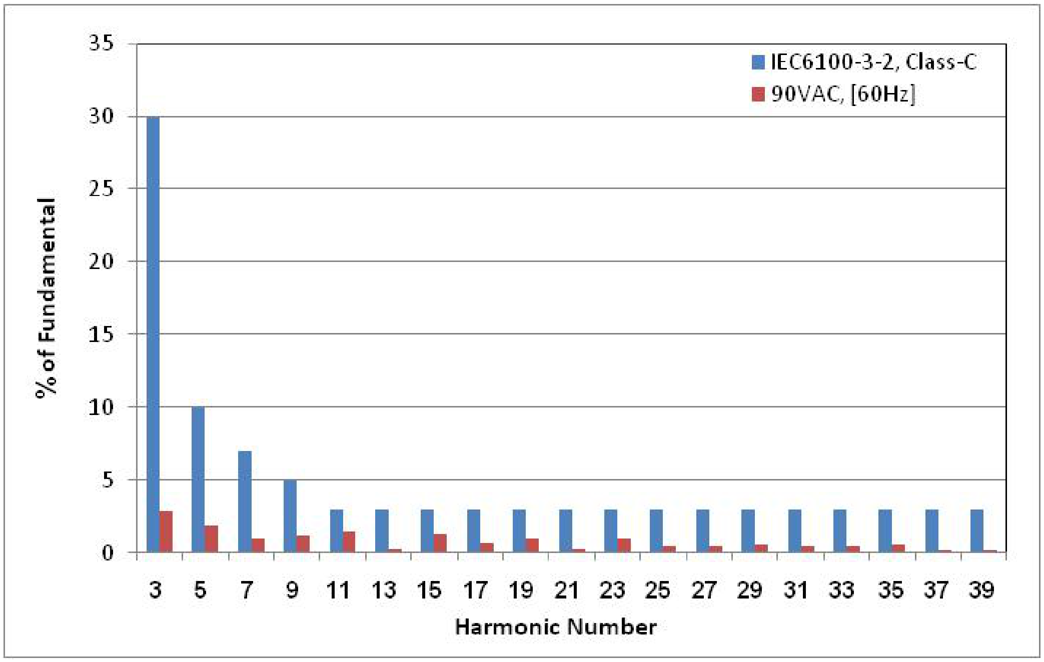

Figure 33. V_{IN} = 90 V_{AC} / 60 Hz

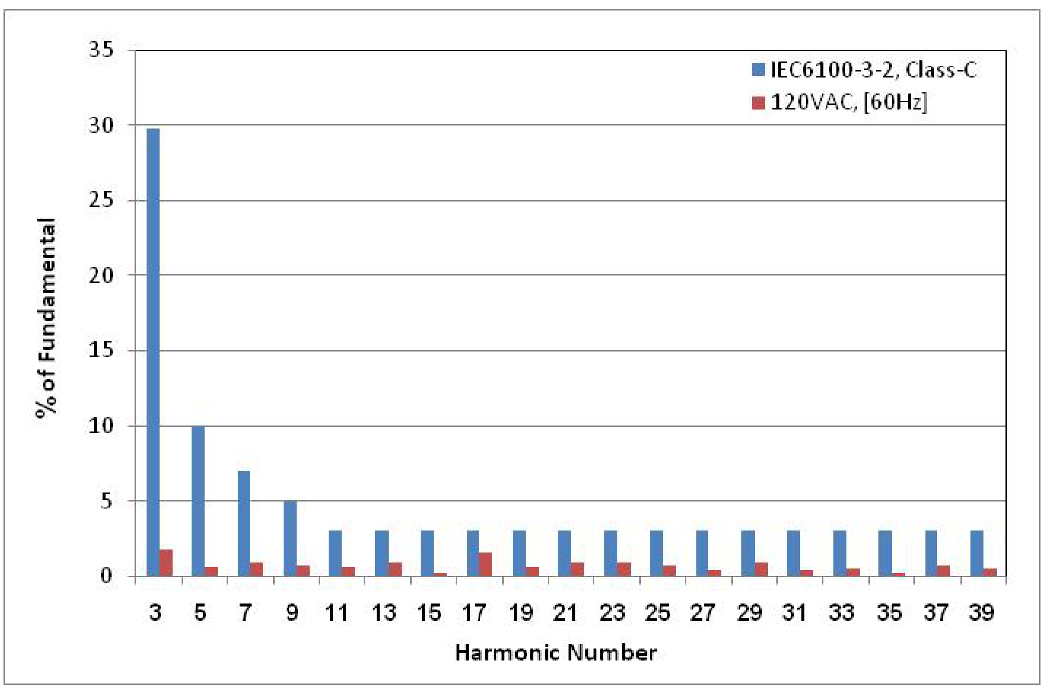

Figure 34. V_{IN} = 120 V_{AC} / 60 Hz

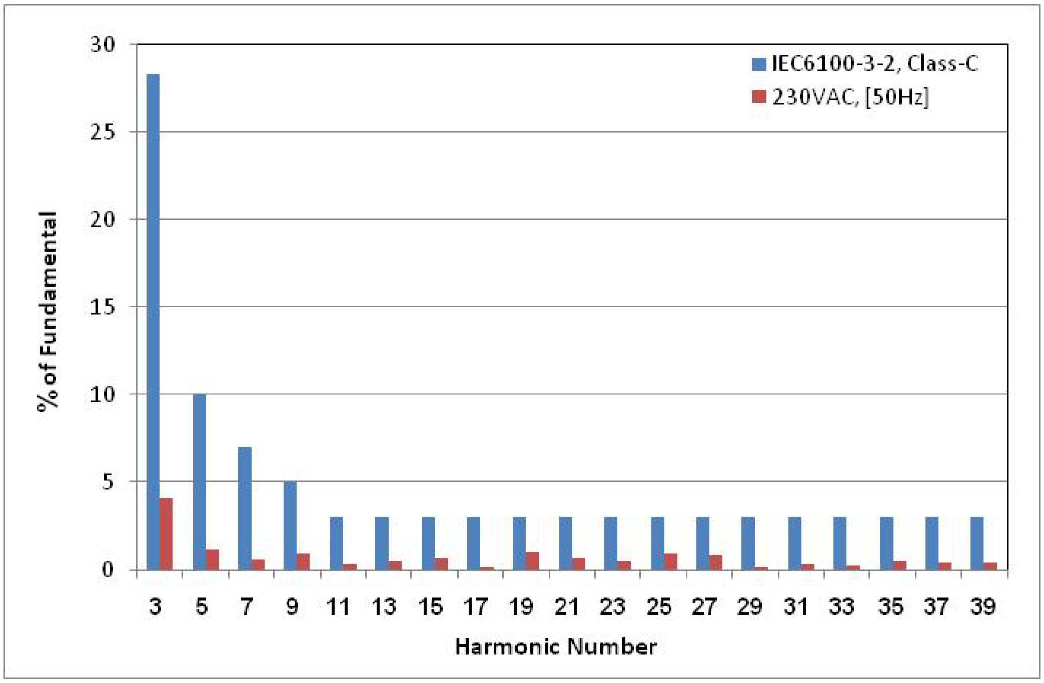

Figure 35. V_{IN} = 230 V_{AC} / 50 Hz

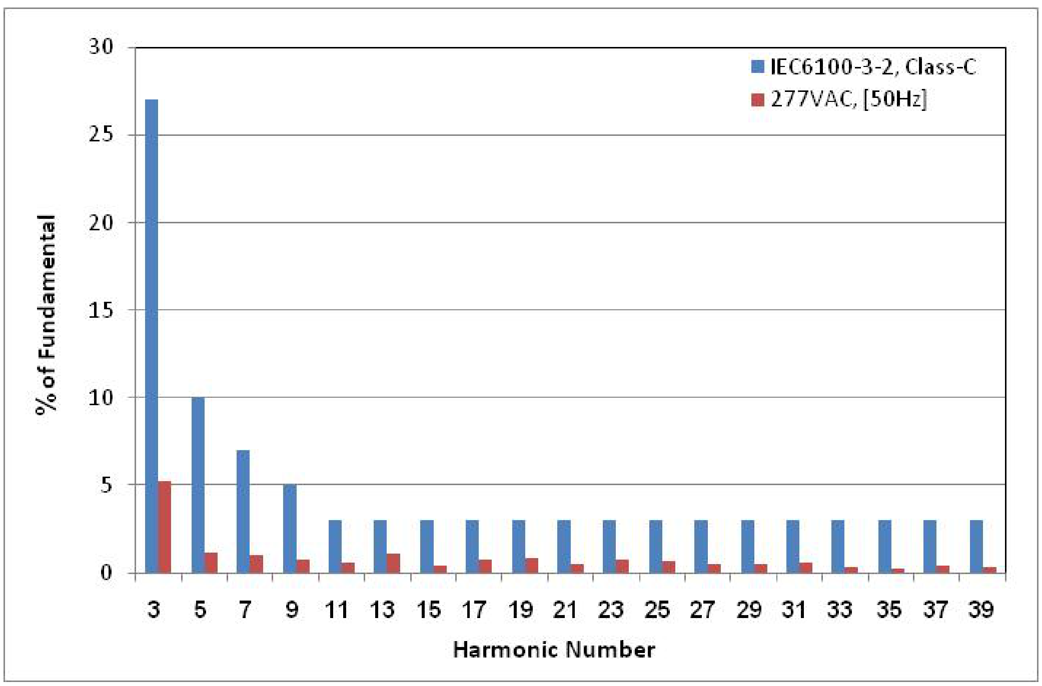

Figure 36. V_{IN} = 277 V_{AC} / 50 Hz

Operating Temperature

Temperatures on all components for this board are less than 68°C.

The result were measured using actual rated LED loads 60 minutes after startup.

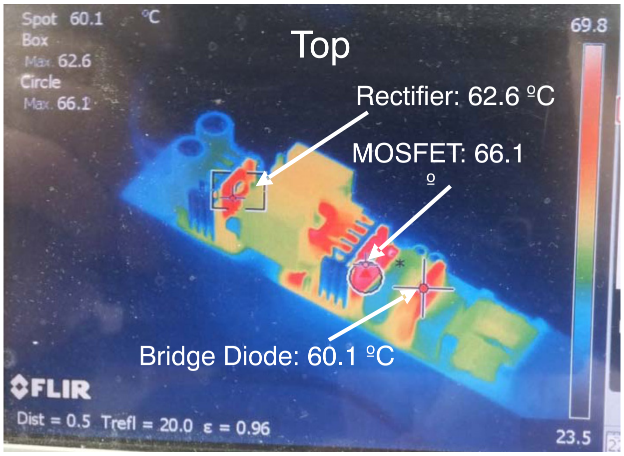

Figure 37. V_{IN} = 90 V_{AC} / 60 Hz

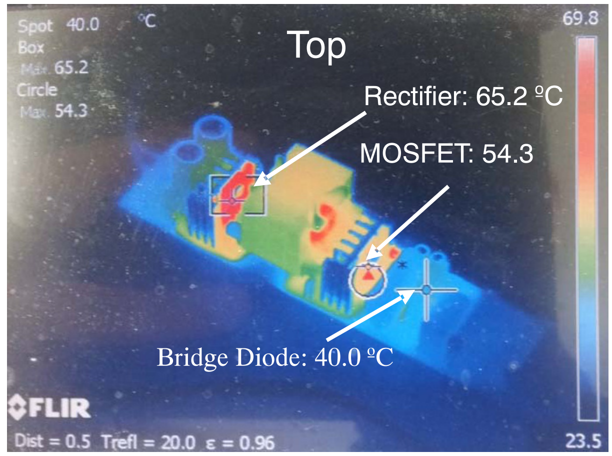

Figure 38. V_{IN} = 277 V_{AC} / 50 Hz

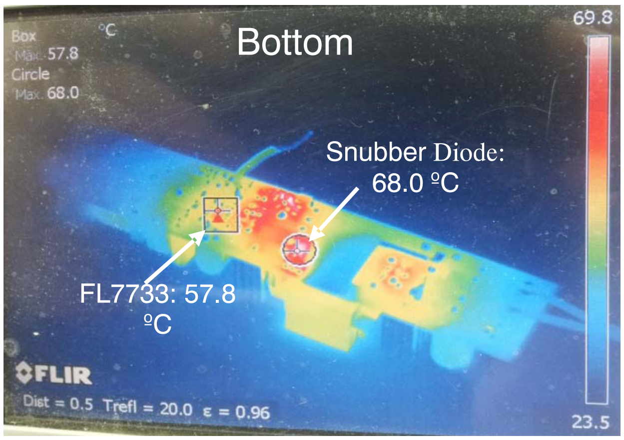

Figure 39. V_{IN} = 90 V_{AC} / 60 Hz

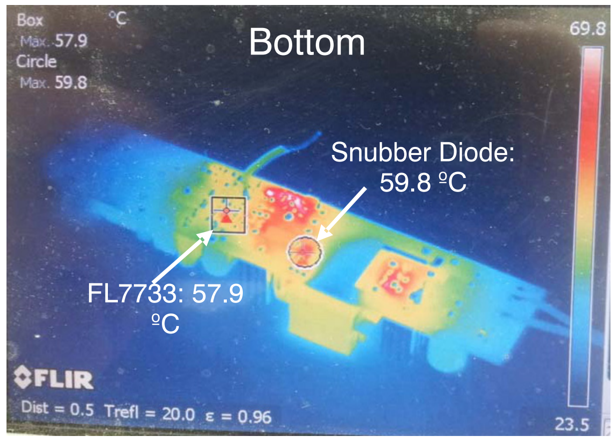

Figure 40. V_{IN} = 277 V_{AC} / 50 Hz

NOTE: The IC temperature can be improved by the PCB layout.

Electromagnetic Interference (EMI)

All measurements were conducted in observance of EN55022 criteria. The result were measured using actual rated LED loads 30 minutes after startup.

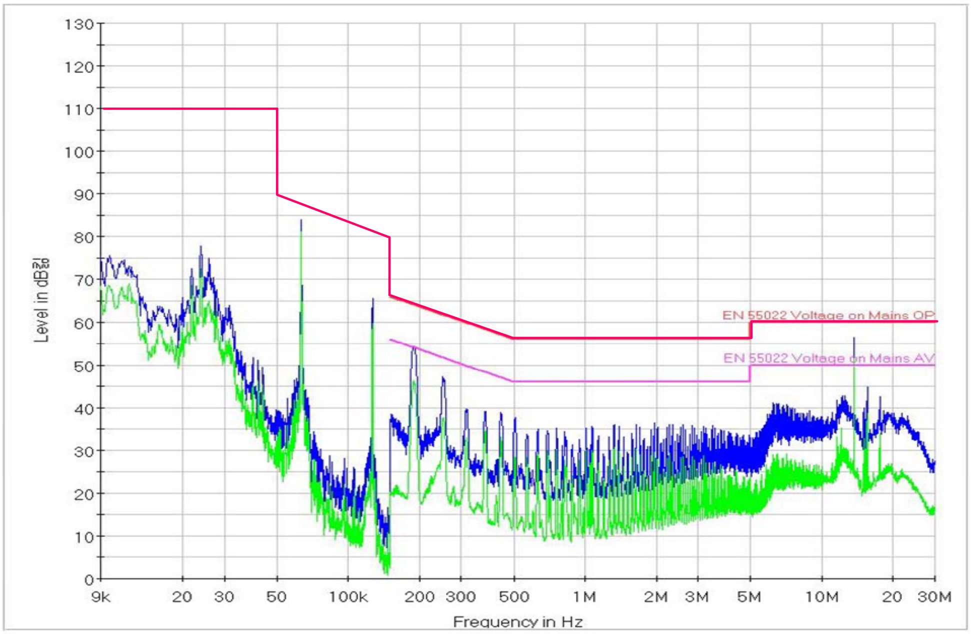

Figure 41. V_{IN} [110 V_{AC}, Neutral]

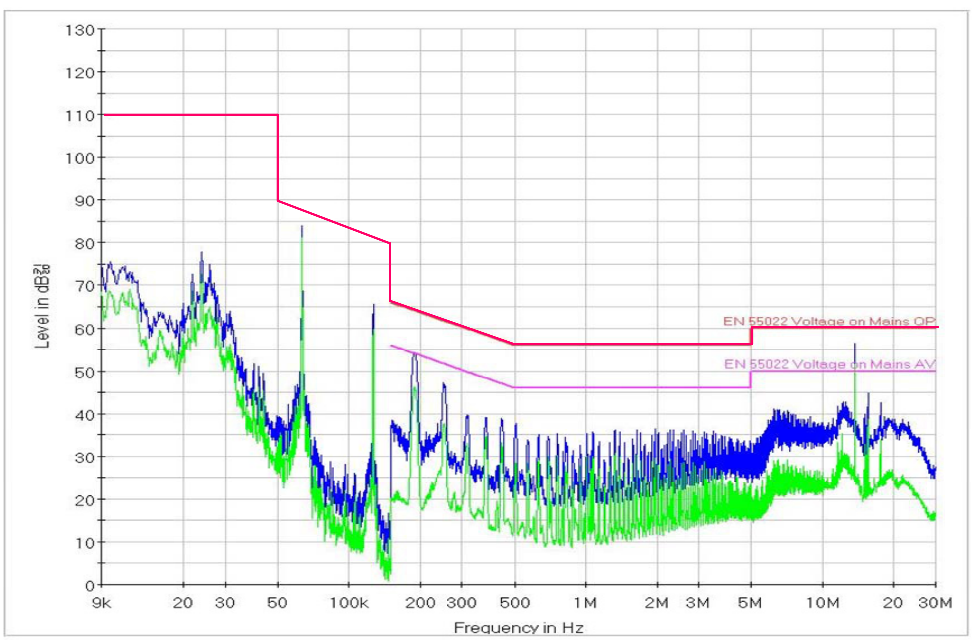

Figure 42. V_{IN} [220 V_{AC}, Live]

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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