NCP51810 HB GaN Driver Evaluation Board User's Manual

NCP51810 High−Speed, Half−Bridge, GaN Driver Evaluation Board for Existing or New PCB Designs

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EVAL BOARD USER'S MANUAL

NCP51810GAN1GEVB

INTRODUCTION

Purpose

The NCP51810 HB GaN Driver Evaluation Board (EVB) is intended to replace the driver and power MOSFETs used in existing half−bridge or full−bridge power supplies. This EVB highlights the performance, simplicity and minimal number of components required to efficiently and reliably drive two gallium nitride power switches used in a mid−voltage, totem pole configuration. Intended applications include off−line power converter topologies such as: phase−shifted full−bridge, active clamp flyback and forward, dual active−bridge, and voltage synchronous buck. This document describes mating techniques for the NCP51810 HB GaN Driver EVB.

NCP51810 GaN Driver Description

The NCP51810 high−speed, gate driver is designed to meet the stringent requirements of driving enhancement mode (E−mode), high electron mobility transistor (HEMT) and gate injection transistor (GIT) HEMT, gallium nitride (GaN) power switches in half−bridge power topologies. The NCP51810 offers short and matched propagation delays with advanced level shift technology providing −3.5 V to +100 V (typical) common mode voltage range for the high−side drive and −3.5 V to +3.5 V common mode voltage range for the low−side drive. In addition, the device provides stable and reliable operation when used in high dV/dt environments up to 200 V/ns. In order to fully protect the gates of the GaN power switches against excessive voltage, both NCP51810 drive stages employ separate, dedicated voltage regulators to accurately maintain the gate−source drive signal amplitude. The circuit offers active clamping of the driver's bias rails thus protecting against potential gate−source over−voltage under various operating conditions.

The NCP51810 offers important protection functions such as independent under−voltage lockout (UVLO), monitoring V_{DD} bias voltage, VDDH and VDDL driver bias and thermal shutdown based on die junction temperature of the device. As shown in Figure 2, the Schmitt trigger, EN, HIN and LIN inputs are internally pulled LOW to assure the driver is always in a default 'OFF' state during initial application of V_{DD} bias. Programmable dead−time control is available by the DT pin and can be configured to prevent or allow cross−conduction.

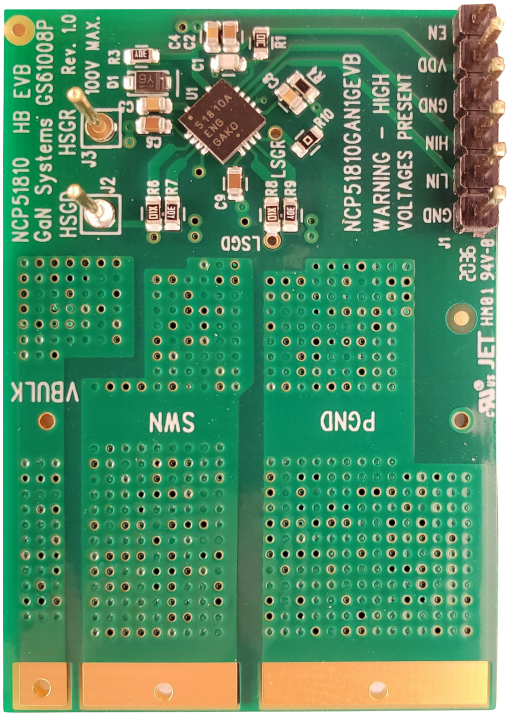

Figure 1. Evaluation Board Photo

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The NCP51810 can be considered as having two independent high−side and low−side "floating" drive stages. The high−side can float up to 100 V referenced to SW and the low−side can float up to 3.5 V referenced to PGND, making it well suited for applications where the driver has to float above a low−side current sense resistor as described in "Connection Method #2" section. Each drive stage includes dedicated input level shifting to ensure accurately matched propagation delays to within 5 ns. Each output includes separate source and sink allowing rise and fall times to be set independently with a single resistor, eliminating additional, discrete circuitry often required for high−speed turn−off.

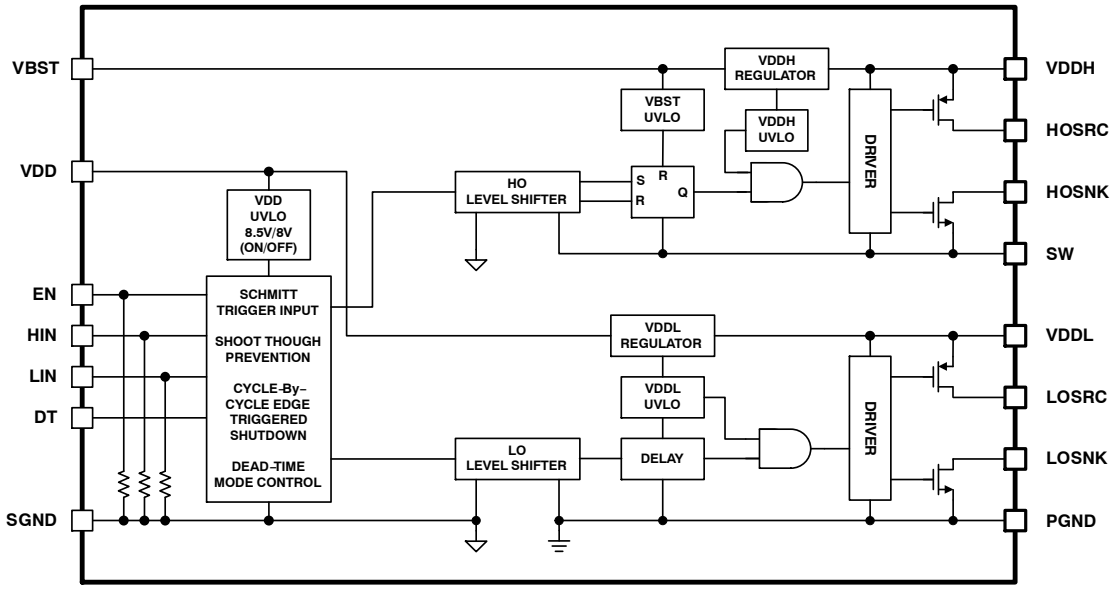


Figure 2. NCP51810, Functional Block Diagram

NCP51810 HB GaN Driver EVB Description

The NCP51810 HB GaN Driver EVB is designed using an 1880 mil x 1310 mil, four−layer printed circuit board (PCB) and includes the NCP51810 GaN driver, two E−mode GaN power switches connected in a high−side, low−side configuration and all necessary drive circuitry. The EVB does not include a PWM controller, and is generic from the point of view that it is not dedicated to any one topology, and can be used in any topology that requires the use of a high−side/low−side FET combination. The EVB can be connected into an existing power supply, and will replace the HS/LS driver and MOSFETs. The EVB has preset, but configurable dead−time control and driver enable/disable. The GaN power switches are rated up to 100 V, 90 A, making them well suited for half−bridge topologies operating from an output in the range of 100 V. However, due to $R_{DS(ON)}$ temperature dependence, the maximum, practical case temperature should not exceed ~90°C (90°C = 1.6 x $R_{DS(ON)}$, normalized at 25°C). The EVB has only 27 components and its small size allows it to be installed in tight areas. Even with the small size, several pins are available to probe the circuit. HS and LS gate drives, as well as SWN are accessible. Note: In half−bridge operation, the HS gate drive can only be probed with a high−voltage differential probe on the Hi−Side Gate Drive (HSGD) pin and the Hi−Side Gate Return (HSGR) pin. The LS gate drive has two plated holes for a tip−and−barrel probe measurement (LSGD). The plated hole closest to the NCP51810 is probe GND, as shown in Figure 3. A tip−and−barrel measurement is performed by removing the "hat" from a passive probe and using the probe "pin" for the measurement and a spring pin fit on the GND barrel of the probe for ground. Figure 4 shows the typical tip−and−barrel measurement method for LSGD using a LeCroy passive probe and GND spring.

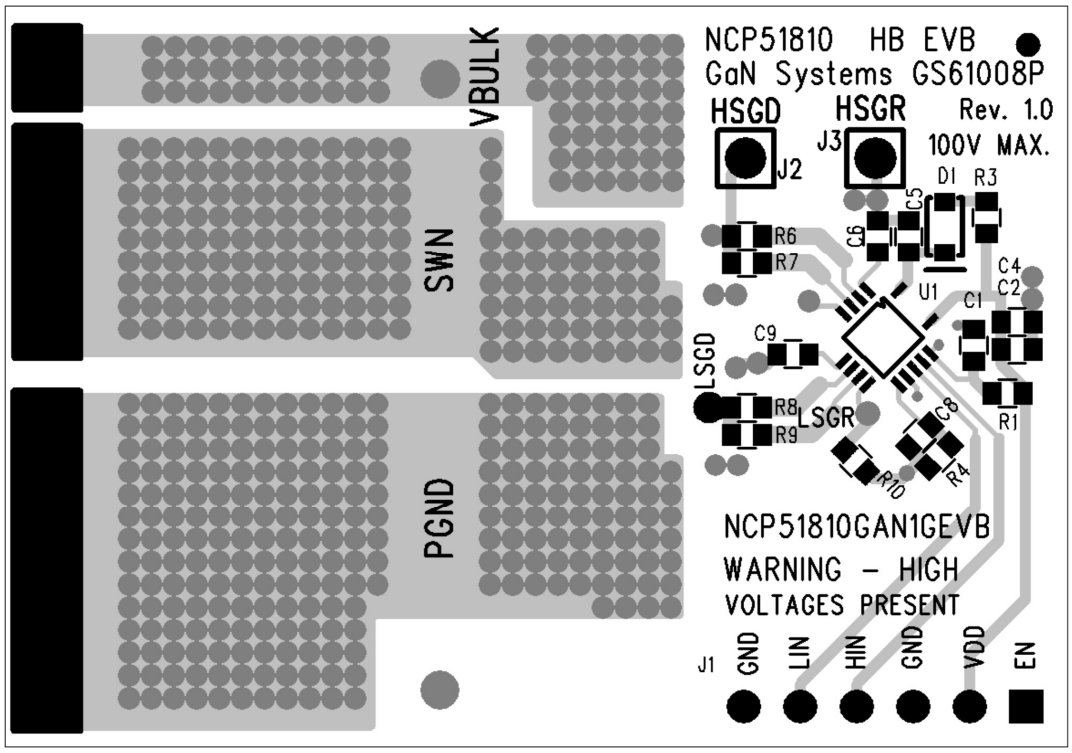


Figure 3. NCP51810 HB GaN Driver EVB

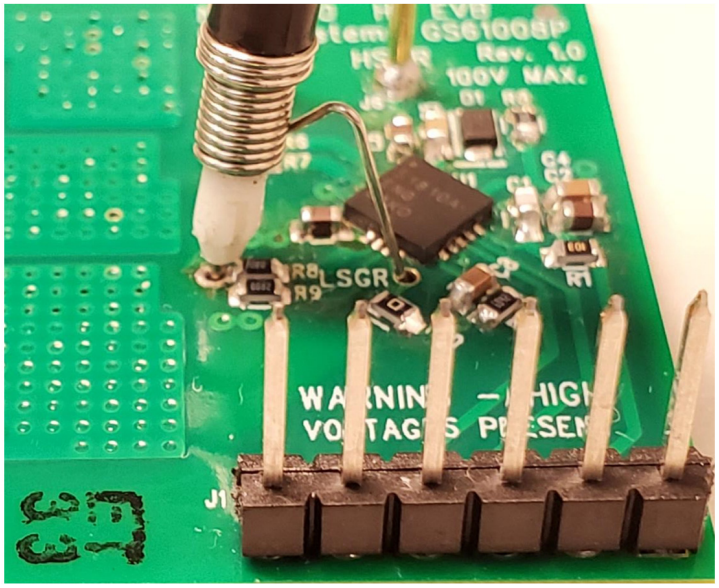


Figure 4. Tip−and−Barrel Measurement Method

NCP51810 EVB Schematic

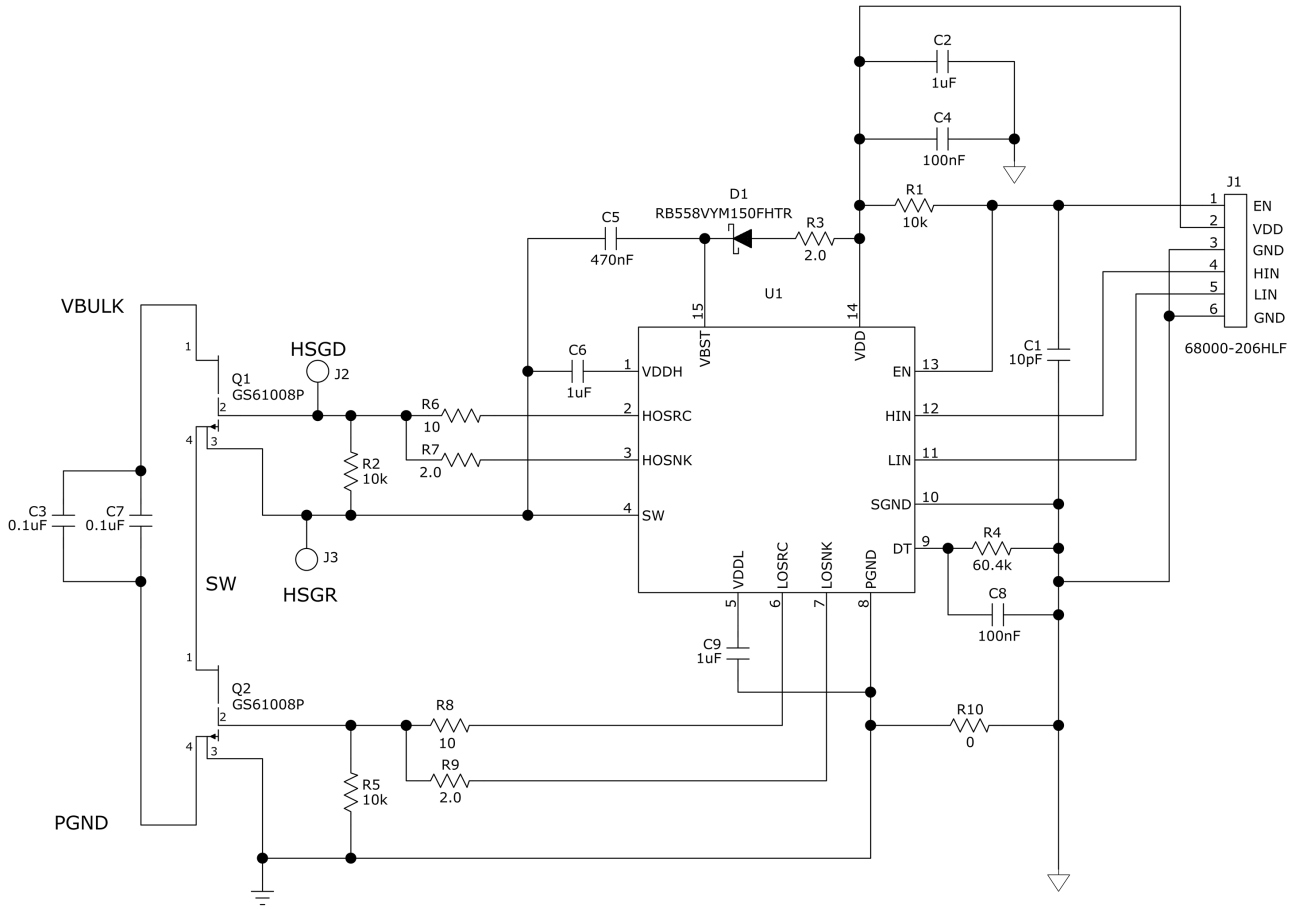


Figure 5. NCP51810 EVB Schematic

NCP51810 EVB Bill of Materials (BOM)

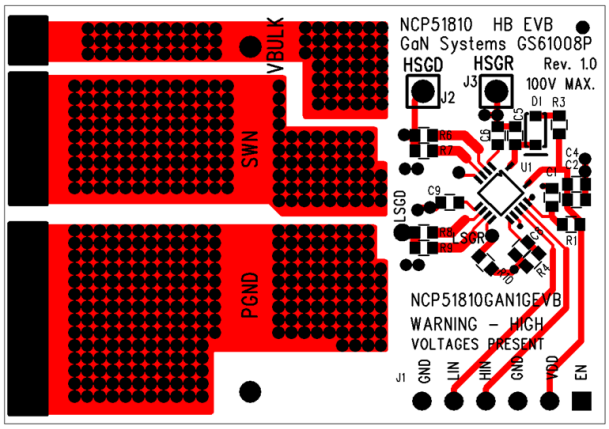
Table 1. NCP51810 EVB BILL OF MATERIALS

Item	Qty	Reference	Value	Part Number	Description	Manufacturer	Pkg Type
1	1	C1	10 pF	CC0603JRNPO9BN100	CAP, SMD, CERAMIC, 50 V, NPO	Yageo	603
2	1	C5	470 nF	CC0603KRX7R8BB474	CAP, SMD, CERAMIC, 25 V, X7R	Yageo	603
3	3	C2 C6 C9	1 μF	CL10B105KA8NNNC	CAP, SMD, CERAMIC, 25 V, X7R	Samsung	603
4	2	C3 C7	0.1 μF	C1206J104K2RAC7800	CAP, SMD, CERAMIC, 200 V, X7R	Kemet	1206
5	2	C4 C8	100 nF	CC0603KRX7R8BB104	CAP, SMD, CERAMIC, 25 V, X7R	Yageo	603
6	1	D1		RB558VYM150FHTR	Diode_Shottky, 150 V, 500 mA, 6.35 ns RR	Rohm	SOD−323
7	1	J1		68000−206HLF	Header, SIP6 100mil pitch, Post − 95 mil, Mate − 230 mil	Amphenol	Thru−Hole
8	2	J2−3		1352−1	Testpin, Gold, 40 mil, 28 mil solder length	Keystone	Thru−Hole
9	2	Q1−2		GS61008P	GaNFET, 100 V, E−mode, 90 A, 7 mΩ, Kelvin Source	GaN Systems	7.55 x 4.59 mm
10	1	R4 (Note 1)	60.4 kΩ	RMCF0603FT60K4	RES, SMD, 1/10 W	Stackpole	603
11	1	R10 (Note 2)	0 Ω	RC0603JR−070RL	RES, SMD, 1/10 W	Yageo	603
12	3	R1−2 R5	10 kΩ	RC0603FR−0710KL	RES, SMD, 1/10 W	Yageo	603
13	3	R3 R7 R9	2 Ω	CPF0603F2R0C1	RES, SMD, 1/10 W	TE Connectivity	603
14	2	R6 R8	10 Ω	RC0603FR−0710RL	RES, SMD, 1/10 W	Yageo	603
15	1	U1		NCP51810	High Speed Half Bridge GaN Driver, 200 V	ON Semiconductor	MLP 4x4−15

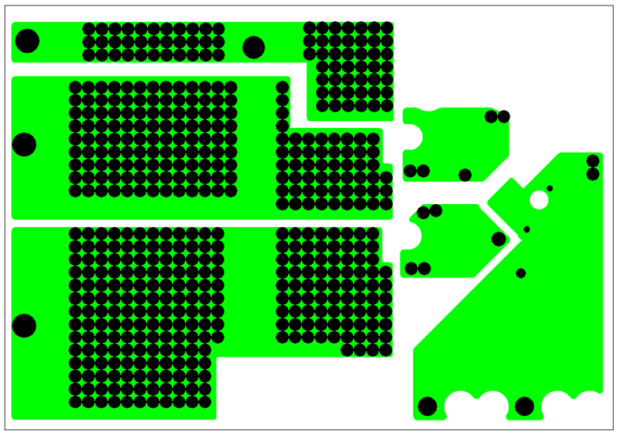
1. R4 used to set dead−time (DT).
2. R10 used to connect SGND to LS gate return.

NCP51810 Layers

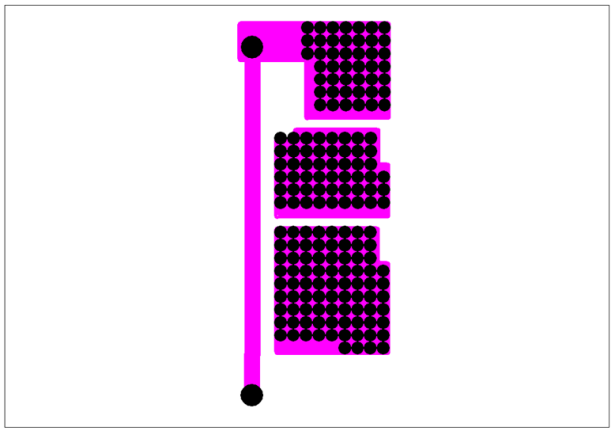
- **Top Layer:** The large copper high current carrying etches used to connect the HS/LS GaN power switches also act as heat spreaders. A heatsink (if utilized) will be attached to this layer.
- **Layer 2 (Internal):** This layer has a shielding plane for the driver and driver components as well as additional high current carrying etches for the HS/LS GaN power switches.
- **Layer 3 (Internal):** Layer 3 has additional high current carrying etches for the HS/LS GaN power switches.
- **Bottom Layer:** The high current carrying etches for the HS/LS GaN power switches on the bottom layer also act as heat spreaders.



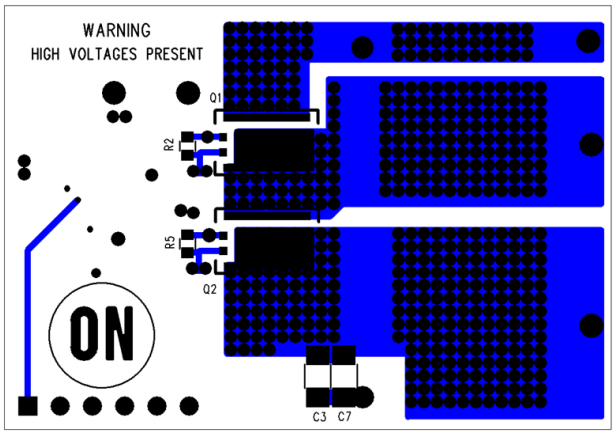
Top Layer



Layer 2, Internal



Layer 3, Internal



Bottom Layer

Figure 6. PCB Assembly and Layers

NCP51810 EVB I/C Connections

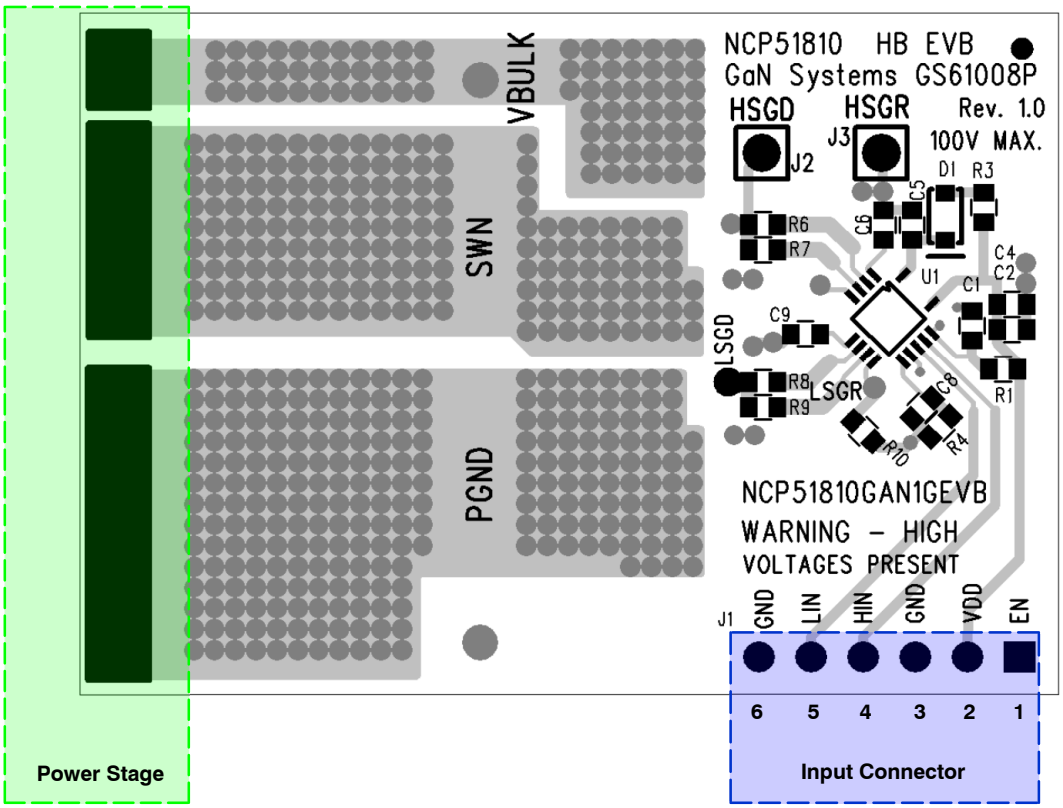


Figure 7. EVB I/O Connections

Table 2. I/O CONNECTOR DESCRIPTION

Pin Name	Pin Type	Description	Value
EN (Note 3)	J1−1	Logic input for enabling/disabling the driver	2.5 V < EN < V_{DD} + 0.3 V
VDD	J1−2	Bias voltage for high current driver	8 V < V_{DD} < 20 V
GND	J1−3,6	Signal ground on the driver	0 V
HIN	J1−4	Logic input for high−side gate driver	0 V < HIN < V_{DD} + 0.3 V
LIN	J1−5	Logic input for low−side gate driver	0 V < LIN < V_{DD} + 0.3 V
VBULK	PAD	VIN connection	100 V max
SWN	PAD	Switch Node connection	100 V max
PGND	PAD	Power Ground connection	0 V

3. EN pin tied to driver V_{DD} through 10 kΩ resistor (R1) on EVB.

NCP51810 EVB CONNECTION METHODS

There are two different methods for connecting the EVB to an existing power board.

Power topologies not using a current sense resistor connected in series with the LS GaN power switch source (a current sense transformer or other method of sensing current used) will use Connection Method #1, shown in "Connection Method #1" section.

Power topologies using a current sense resistor (R_{CS}) connected in series with the LS GaN source, will use Connection Method #2, shown in "Connection Method #2" section.

Preparing Power Board for EVB Connection

1. Remove HS and LS MOSFETs and HS and LS gate drive resistors from the power board as illustrated in Figure 8.
2. Remove any gate turn off circuitry. This is any circuit used to help drive the gate to 0 V during turn off.
3. Before connecting the EVB, ensure that VDD, HIN, LIN, and VBULK are within the parameters listed in Table 2.

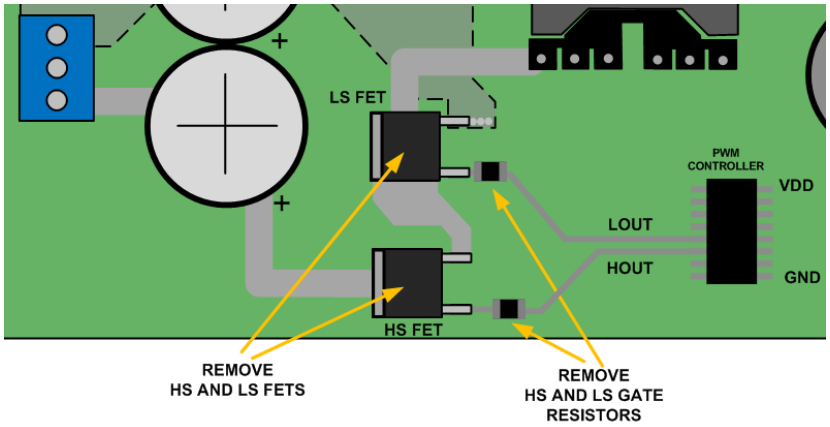


Figure 8. Power Board Preparation

Connection Method #1 – No GaN LS Current Sense Resistor on Power Board

Connect the EVB as shown in Figure 9. AWG #22 wire is suggested for LIN, HIN and VDD. AWG #18 or larger wire is suggested for VBULK, SWN and PGND. Keeping both the Input connections and the VBLK, SWN and PGND connections as short as possible is preferred.

Connection Method #2 – LS GaN Current Sense Resistor (R_{CS}) Present on Power Board

Low−power applications, such as an active−clamp flyback or forward converter often use a current sensing resistor, R_{CS}, located in the low−side GaN power switch-source leg. In such applications, the EVB PGND and SGND pins must be isolated on the EVB (normally connected by R10) because R_{CS} would essentially be shorted through this resistor if not removed. The NCP51810 low−side drive circuit is able to withstand −3.5 V to +3.5 V of common mode voltage. Since most current sense voltage signals are less than 1 V, the low−side drive stage can easily "float" above the voltage, V_{RCS}, generated by the current sense resistor.

Connection Method #2: Remove R10 on the EVB to isolate LS gate drive return from GND as shown in Figure 10 and Figure 13. Failure to remove R10 will short out R_{CS}. Connect the EVB as shown in Figure 10. AWG #22 wire is suggested for LIN, HIN and VDD. AWG #18 or larger wire is suggested for VBULK, SWN and PGND. Keeping both the input and power connections as short as possible is preferred.

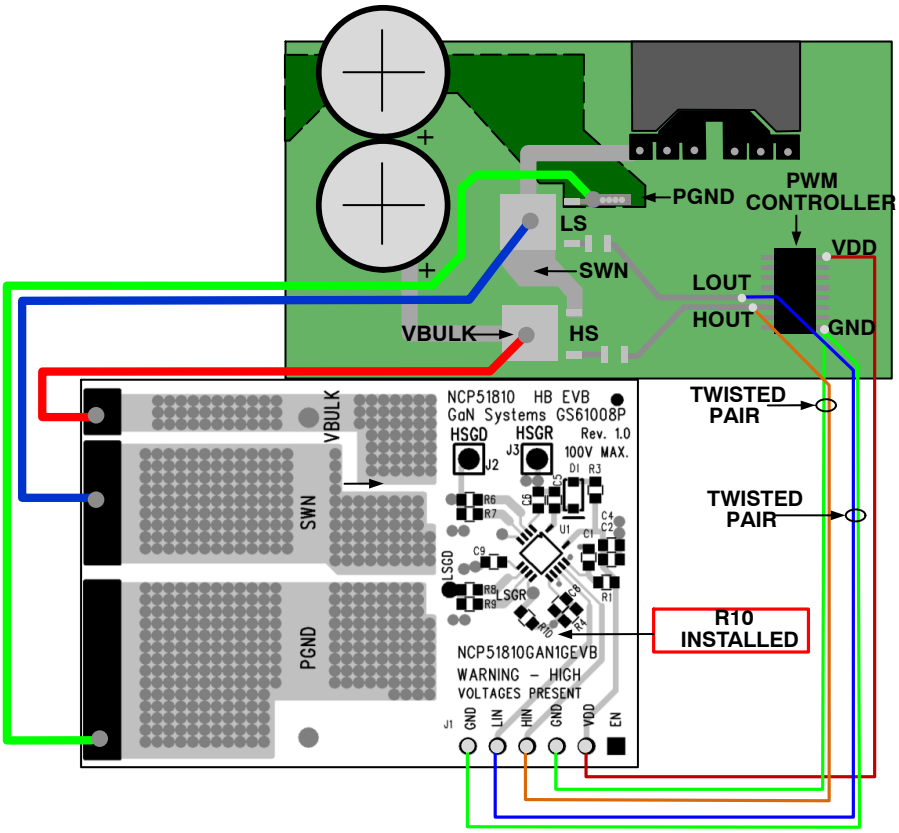


Figure 9. Connection Method #1 – No LS Current Sense Resistor

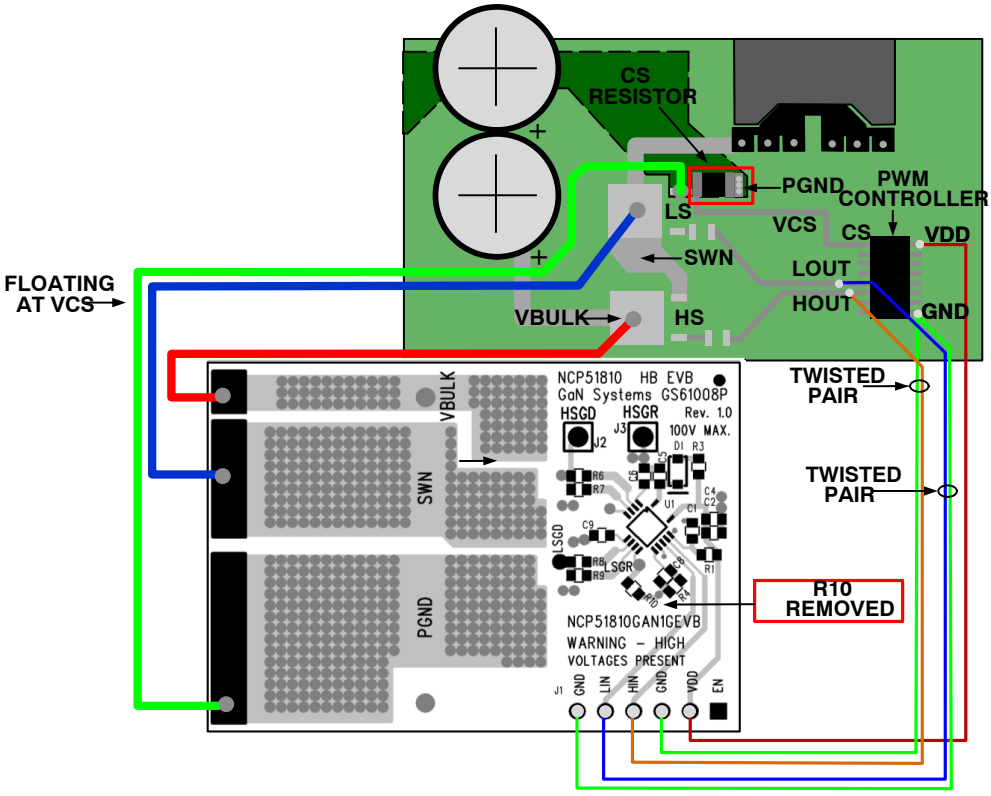


Figure 10. Connection Method #2 – LS Current Sense Resistor on Power Board

External VDD

An external VDD can be used, as long as the HIN and LIN signals still fall within the parameters listed in Table 2. If an external VDD is used, the external VDD GND connection must be connected to the power board VDD GND, as shown in Figure 11. An external VDD can be used for boards either with or without an LS Current Sense Resistor. When using an external VDD, put a 1N4148 blocking diode (or similar 60 V, 1A minimum diode) in series with VDD + to protect the VDD supply. It's also suggested to put a small electrolytic decoupling capacitor (example: 22 μF, 35 V) across the External VDD supply output, as shown in Figure 11. VDD voltage should be measured and set after the blocking diode to take into account the voltage drop across the diode.

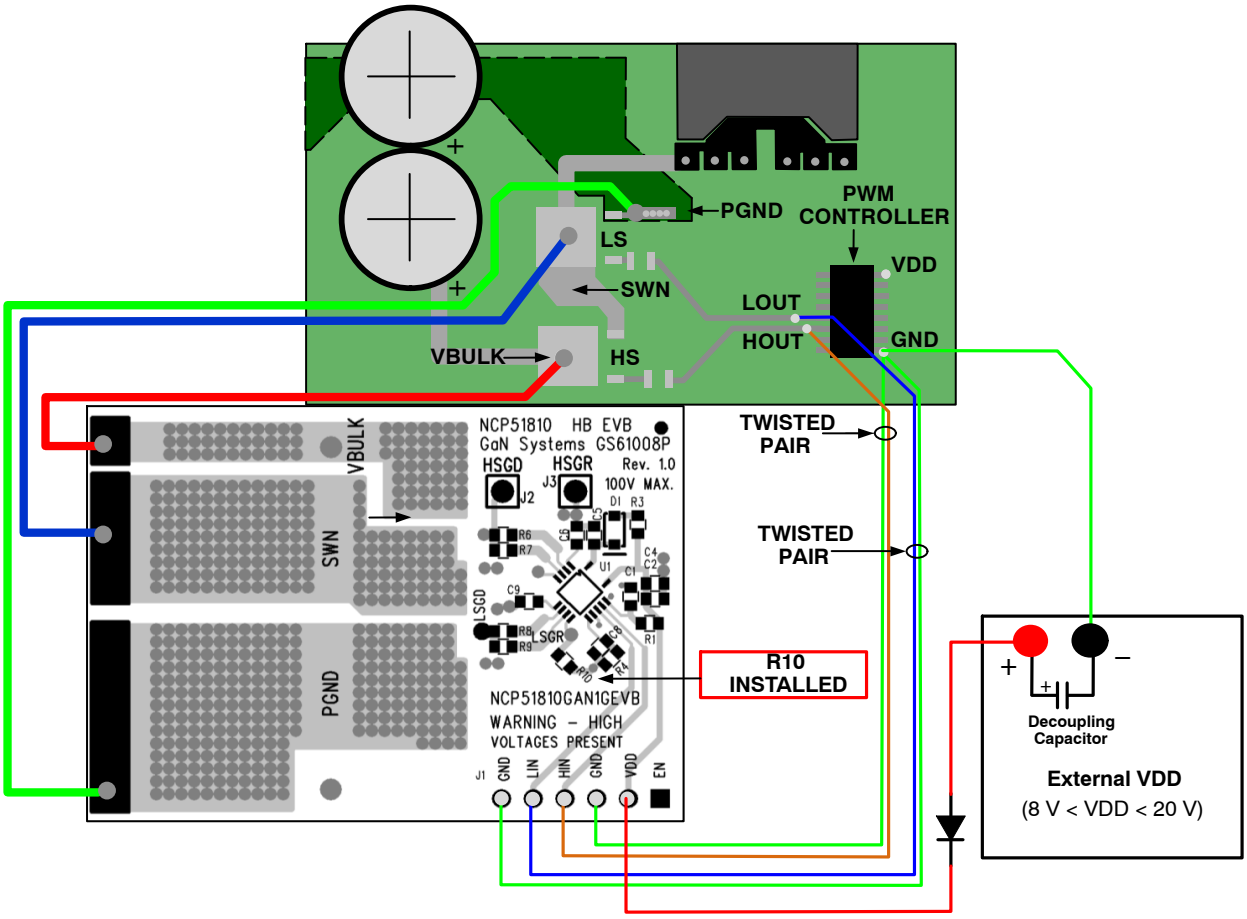


Figure 11. External VDD Connection

Thermal Considerations

Applications where higher currents could cause GaN power switch temperatures to exceed 90°C (such as a high power, synchronous buck), a voltage−isolated adhesive heatsink can be attached to the top of the EVB. The GaN power switches on this EVB are bottom−cooled. Copper heat spreaders are part of the top and bottom layer of this EVB. A voltage−isolated adhesive heatsink attached to the EVB top will aid in reducing the GaN power switch temperatures. Figure 12 shows the positioning of a heatsink.

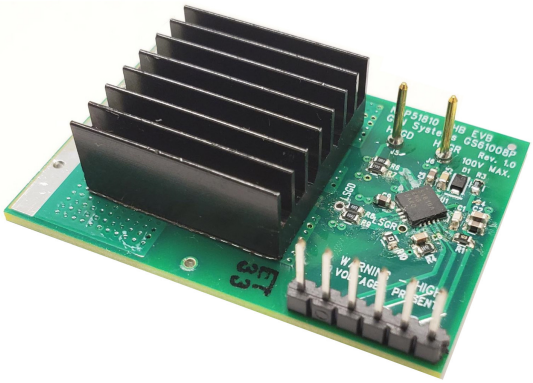


Figure 12. NCP51810 HB GaN Driver EVB and Heatsink

CONFIGURING ENABLE (EN) AND DEAD−TIME (DT)

EN Function and External Control

The NCP51810 GaN Driver EN is internally pulled low to SGND, so the driver is always defaulted to a disabled output status. Similar to HIN and LIN, EN is a Schmitt trigger TTL compatible input. Pulling the EN pin above 2.5 V typical, enables the outputs, placing the NCP51810 into an active ready state. Due to the nature of high−speed switching associated with GaN power stages, and for improved noise immunity, the EN pin is tied to V_{DD} through a 10−kΩ (R1) pull−up resistor and is bypassed by a 10 pF capacitor (C1). If an external enable signal is preferred, the external enable signal must conform to the value limits listed in Table 2. More information on EN control can be found in the NCP51810 datasheet.

When using an external active enable signal, remove R1 and connect a signal to the EN pin on the EVB. The external enable signal GND must connect to the EVB GND. The 10 pF EN bypass capacitor (C1) on the EVB must remain installed. Refer to Figure 13 for R1 and C1 locations.

DT Function and Mode Configuration

Accurately ensuring some minimal amount of dead−time between the high−side and low−side gate drive output signals is critical for safe, reliable optimized operation of any high−speed, half−bridge power stage. The NCP51810 uses a voltage−configured, dead−time control pin (DT). The NCP51810 offers four unique mode settings to utilize dead−time in such a way to be fully compatible with any control algorithm.

The EVB dead−time is preset to Mode B by a single, 60.4 kΩ resistor (R4) connected between the DT and SGND pins. This sets the dead−time voltage to 1.3 V, proportional to approximately 65 ns of dead−time. When adjusting the dead−time is required, the resistor value can be changed, which will change the voltage level on the DT pin. Follow the instructions outlined In DT Mode Descriptions to change DT modes. For noise immunity, the DT pin is bypassed with a 0.1 μF capacitor (C8). This capacitor must not be removed. More information on dead−time control can be found in the NCP51810 datasheet. Refer to Figure 13 for R4 and C8 locations.

DT Mode Descriptions

1. MODE A: Connect DT to SGND; When the DT pin voltage, V_{DT}, is less than 0.5 V typical (R_{DT} = 0 Ω), the DT programmability is disabled and fixed dead−time, anti−cross−conduction protection is enabled. If HIN and LIN are overlapping by X ns, then X ns of dead−time is automatically inserted. Conversely, if HIN and LIN have greater than 0 ns of dead−time then the dead−time is not modified by the NCP51810 and is passed through to the output stage as defined by the controller. This type of dead−time control is preferred when the controller will be making the necessary dead−time adjustments but needs to rely on the NCP51810 dead−time control function for anti−cross−conduction protection.
2. MODE B: Connect a 25 kΩ < R_{DT} < 200 kΩ Resistor from DT to SGND; Dead−time is programmable by a single resistor connected between the DT and SGND pins. The amount of desired dead time can be programmed via the dead time resistor, R_{DT}, between the range of 25 kΩ < R_{DT} < 200 kΩ to obtain an equivalent dead−time, proportional to R_{DT}, in the range of 25 ns < t_{DT} < 200 ns. If either edge between HIN and LIN result in a dead−time less than the amount set by R_{DT}, the set DT value shall be dominant. If either edge between HIN and LIN result in a dead−time greater than the amount set by R_{DT}, the controller dead−time shall be dominant.
3. MODE C: Connect a 249 kΩ Resistor from DT to SGND; Connect a 249 kΩ resistor between DT and SGND to program the maximum dead−time value of 200 ns. The control voltage range, V_{DT}, for assuring t_{DT} = 200 ns is 4 V < V_{DT} < 5 V.
4. MODE D: Connect DT to VDD; When the DT pin voltage, V_{DT}, is greater than 6 V (pulled up to VDD through 10 kΩ resistor), anti−cross−conduction protection is disabled, allowing the output signals to overlap. If choosing this operating mode while driving a half−bridge power stage, extreme caution should be taken, as cross conduction can potentially damage power components if not accounted for. This type of dead−time control is preferred when the controller will be making extremely accurate dead−time adjustments and can respond to the potential of over−current faults on a cycle−by−cycle basis.

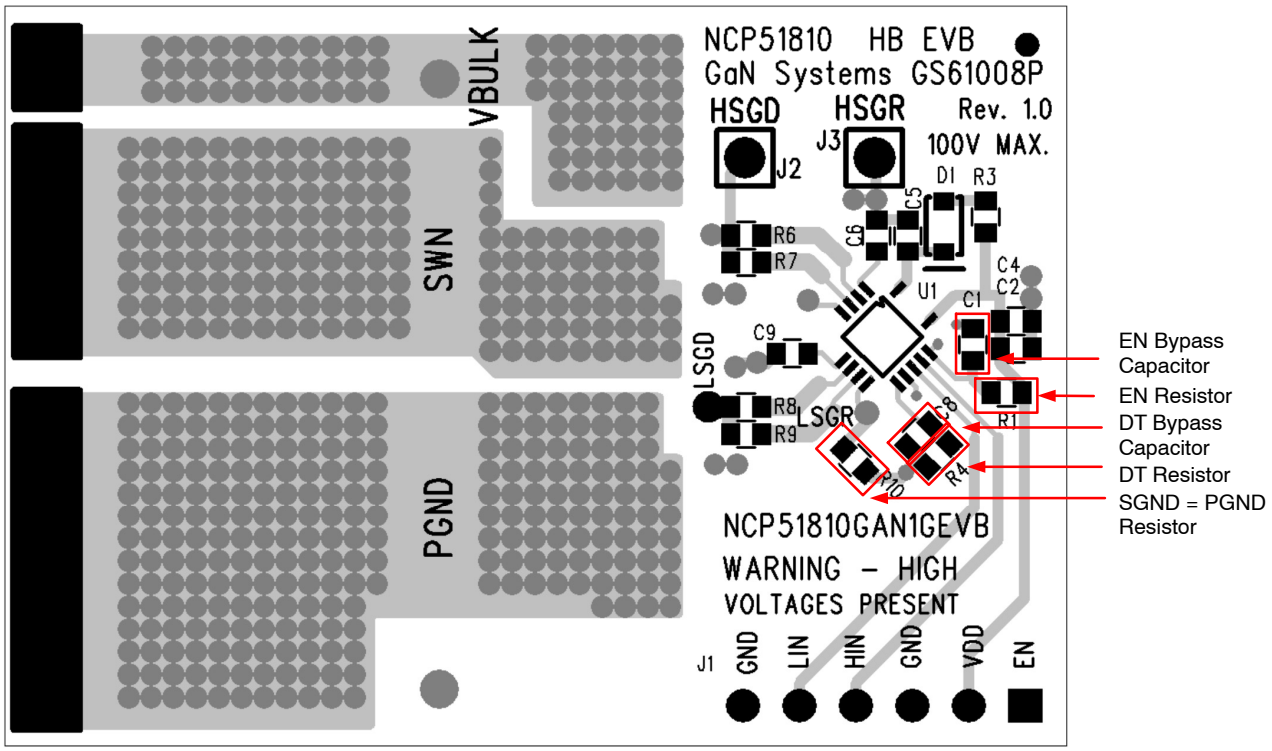


Figure 13. EN and DT Resistor and Capacitor Locations

CONCLUSION

When using this EVB with an existing silicon (Si) half−bridge power stage at normal Si frequencies (40−500 kHz), the true benefits of GaN technology (higher running frequencies, smaller magnetics, higher power density) will not be realized at the lower frequencies that Si typically operates. The goal of this EVB is to easily enable the evaluation of the NCP51810 GaN driver, mating it with existing half−bridge power topologies, and not to significantly change their operation or efficiency. This EVB can be run at high frequencies, but care must be applied to both the input signals and the power connections to be as short as possible to avoid noise injection and ringing. More information on GaN driver PCB design and layout techniques are available at ON Semiconductor/NCP51810.

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