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Basic Thermal Properties of Semiconductors

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Chapter 2

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Abstract

In applications requiring wide ambient temperature ranges, compact form factors, limited airflow, or high power dissipations, thermal design can pose a significant challenge. The basic concepts behind heat transport and thermal modeling are very straightforward, and device datasheet parameters and thermal response curves provide valuable tools to estimate device junction temperatures. Steady−state, transient, and periodic power inputs can all be modeled, and the results allow for accurate estimation of resulting temperatures and heatsinking requirements. In addition, thermal models can be used to assess the likelihood of thermal runaway and to demonstrate the thermal stability of a design.

INTRODUCTION

Three basic processes govern the removal of heat from the rectifier junction to the ambient air: conduction (heat traveling through a material); convection (heat transfer by physical motion of a fluid); and radiation (heat transfer by electromagnetic wave propagation). Heat flows by conduction from the die to the package mounting surface in stud–, base–, or surface–mount pads, but it flows from the die through the leads to the mounting terminals in a lead–mounted part. This thermal conduction can be modeled and designed for, so that the devices in question do not exceed their maximum junction temperatures. Steady state, periodic and transient thermal conditions can all be modeled and solved, allowing the design to maintain proper thermal operating points, ensure device lifetimes and prevent thermal runaway.

THERMAL MODELS

Thermal resistance may be used to form simple models to compute steady state operating temperatures for a circuit under DC or periodic conditions. With the addition of thermal capacitance, transient conditions may also be accurately modeled. The results depend on the operating conditions, including power consumption (heat generation), mounting methods, airflow and ambient temperatures. Nevertheless, the concept provides a very valuable tool for handling thermal problems.

Using a thermal model, complex thermal systems may be easily analyzed using electrical network theorems, including ohm's law, Thévenin's theorem, Norton's theorem and superposition. These techniques may be applied to case–mounted and lead–mounted devices, with one or more active die, under constant, periodic, and transient conditions.

Thermal Resistance

Just as a material offers resistance to the flow of current, it also offers resistance to the flow of heat. Resistance to heat flow is called thermal resistance, and computationally it is almost identical to electrical resistance. For steady–state conditions thermal resistance (θ) is given as:

$$\theta = \Delta T/P \qquad \text{(eq. 1)}$$

or

$$\Delta T = \theta \cdot P \qquad \text{(eq. 2)}$$

Where:
θ = Thermal resistance in °C/W
ΔT = Temperature difference between points in °C
P = Power in watts, dissipated at the point in question

The junction temperature of a semiconductor must be held below the maximum rating for the part. The junction is commonly used as a temperature reference point for thermal calculations involving semiconductors. The other reference point is the case for case–mounted parts or a specified point on a lead for axial lead mounted parts. These reference points are denoted with subscripts. For example, θ_{JC} signifies junction–to–case thermal resistance, and θ_{JL} signifies junction–to–lead thermal resistance. The corresponding temperature differences are denoted ΔT_{JC} and ΔT_{JL}, respectively.

Thermal Resistance and Thermal Characterization Parameters

Thermal resistance (θ) denotes the resistance along a specific path. When using true thermal resistances all paths must be taken into account to compute power and temperature relationships. There is a related set of characterization parameters (Ψ) that denote the relationship between power dissipation and temperature, ignoring path dependent relationships. Computationally, they are nearly identical to thermal resistance values.

$$\Psi = \Delta T/P \qquad \text{(eq. 3)}$$

Where:
Ψ = Thermal characterization parameter (in °C/W), estimating the equivalent thermal resistance for all conduction paths

For lack of a better alternative, thermal characterization parameters are often specified when the reference point does not lie on a significant heat conduction path (like the case on a surface mount device), or when the heat conduction paths are complex and hard to measure or model. In these situations, the thermal characterization parameter will be less accurate than the full thermal model, but for complex systems it is computationally much simpler than considering each thermal path and each thermal resistance separately. Instead, the single value (Ψ) can be thought to represent the temperature/power/resistance relationship between two points when all heat conduction paths are conducting, without explicit consideration of different conduction paths (assuming that the paths are conducting in similar proportions to those present when the parameter was measured). Thermal resistances can be used to model heat flow and temperature relationships, while thermal characterization parameters only give temperature relationships without any information about the direction or path of the heat flow. In datasheets, the quoted "thermal resistance" values are commonly thermal characterization parameters (Ψ), not true thermal resistances (θ).

Example 1: Differentiating θ and Ψ

Consider a system with one point of heat generation, and two paths of significant heat conduction (see Figure 1). Given the resistances for the two conduction paths, θ_{XA1} and θ_{XA2}, a thermal reference parameter, Ψ_{XA}, the power dissipation at the point of heat generation, P_D, and the ambient temperature, T_A, compute the temperature at the point of generation, T_X.

Given:

$$P_D = 6\ W$$

$$\theta_{XA1} = 2°C/W$$

$$\theta_{XA2} = 1°C/W$$

$$\Psi_{XA} = \frac{2}{3}°C/W$$

$$T_A = 25°C$$

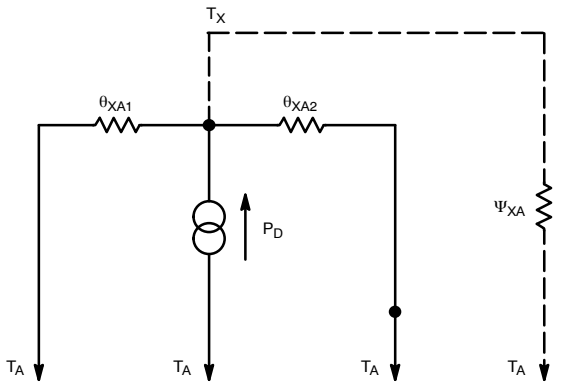


Figure 1. Thermal Network for Example 1

PROCEDURE

The node temperature can be computed from the thermal resistances (Ψ_{XA} will be ignored, since it is not a thermal resistance):

$$T_X = T_A + P_1 \cdot \theta_{XA1} \quad \text{(eq. 4)}$$

$$T_X = T_A + P_2 \cdot \theta_{XA2} \quad \text{(eq. 5)}$$

$$P_D = P_1 + P_2 \quad \text{(eq. 6)}$$

Solving the three equations simultaneously yields:

$$P_1 = 2\ W \quad \text{(eq. 7)}$$

$$P_2 = 4\ W \quad \text{(eq. 8)}$$

$$T_X = 29°C \quad \text{(eq. 9)}$$

Alternatively, it can be computed from the Ψ_{XA} value directly:

$$T_X = T_A + P_D \cdot \Psi_{XA} \quad \text{(eq. 10)}$$

$$T_X = 29°C \quad \text{(eq. 11)}$$

Use of the thermal reference parameter instead of the thermal resistances computed the resulting temperature more easily, but it did not give any information about the heat flow. The thermal resistance calculation was more involved, but it showed the heat flow as well as the resulting temperature.

Case−Mounted Rectifiers

In a case mounted device, the total thermal resistance, junction−to−case, is composed of three thermal resistances: the die, the die−bond, and the package (see Figure 2). The die−bond thermal resistance usually dominates the total resistance, and the other conduction paths (the wirebonds and the mold compound) are negligible by comparison. Actual values vary with the design of the device; the size of the chip, type of die bond, package type and package material all affect the overall thermal performance (see Figure 3). The die−bond thermal resistance will also vary among parts in the same product line, and the amount of variation will depend on the solder or bond material used in the parts.

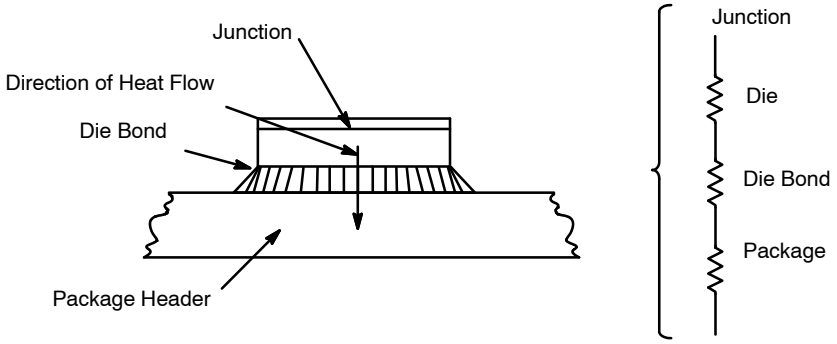


Figure 2. Thermal Resistance Components of the Junction−to−Case Thermal Resistance

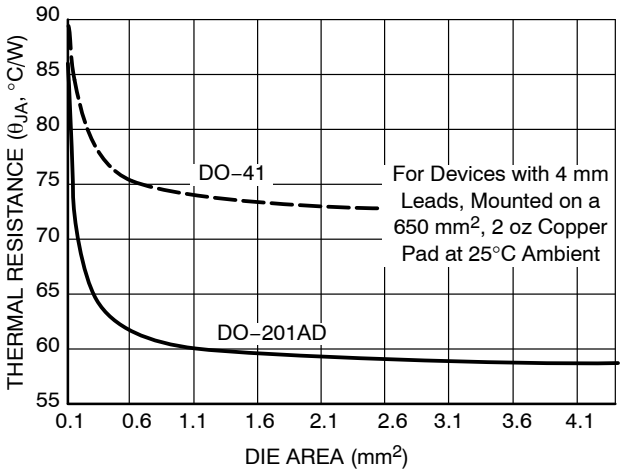


Figure 3. Approximate Thermal Resistance of Axial Rectifier Packages

In addition, some devices may have material inserted between the die and the package to reduce stress or provide electrical insulation. Differing coefficients of thermal expansion between the die and the case can require an extra material at the interface to relieve the stress, allowing a hard solder die attachment technique and improving temperature cycling behavior. In some packages, the package exterior is typically electrically connected to the die, and these parts may be manufactured with insulation inserted between the die and the package to prevent this connection. These materials, if present, add another component to the thermal resistance of the assembly.

Thermal resistance and resistivity (θ and ρ) follow equations of the same form as electrical resistance and resistivity.

$$\theta = \rho \cdot \frac{1}{A} = \frac{1}{k \cdot A} \qquad \text{(eq. 12)}$$

Where:
ρ = Thermal Resistivity
l = Length of Thermal Path
A = Area of Thermal Path
k = Thermal Conductivity

Thermal resistance is inversely proportional to area. For case mounted semiconductors, that refers to the area of heat flow through the package, which is related to, but not the same as, die area. Larger die in the same package have more contact area with the package, but the package itself has the same area regardless of the die size. Overall thermal resistance decreases with increased die area, but the decrease is not linear (see Figure 3).

Typically, the junction−to−case resistance (or junction−to−case thermal characterization parameter, Ψ) for a device will be listed on the datasheet for the part, and combined with the power consumption and external temperature, can be used to estimate the junction temperature of the device in an application.

Lead−Mounted Parts

In an axial lead−mounted rectifier, heat travels down both leads to the printed circuit board, which functions as a heat dissipater. In some cases, the heat dissipated by convection and radiation is also significant, which can make modeling a lead mounted model more complicated than a case−mounted part. However, in certain lead−mounted parts the convection and radiation can be neglected compared to the thermal resistance of the leads (for example, in DO−201AD axial devices, see Figure 4). The relative magnitude of the convection and radiation terms can be estimated by examining the relationship between lead length and thermal resistance. If the thermal resistance is linearly proportional to lead length, then the convection and radiation terms are negligible and can be ignored (see Figure 4). If the relationship is not linear, then the convection and radiation terms are significant.

Thermal resistance data is often provided by the part manufacturer under the assumption that the device leads have identical lengths. However, identical lead lengths may not result in the lowest possible thermal resistance. The overall thermal resistance is the parallel combination of the two lead resistances. It may be that the resistance through two equal length long leads (similar to the first or second mounting methods in Figure 5) is higher than the resistance through a very short lead in parallel with a very long lead (similar to the third mounting method in Figure 5). For example, if the leads must span a fixed at 10 unit length (neglecting the case length), and the thermal resistance per unit is 10°C/(W*unit), then the equivalent thermal resistance of two equal 5 unit leads is 25°C/W (symmetrical mounting), but the thermal resistance of a 1 unit length lead in parallel with a 9 unit length lead is 9°C/W (asymmetrical mounting). The reduction from 25°C/W to 9°C/W is quite significant, but to take advantage of this reduction the mounting terminal must have a low thermal resistance to ambient. In addition, this example computation ignored some of the package and die size effects, which may reduce the effectiveness of the asymmetrical mounting. If the die to lead resistance dominates the total resistance, then shortening the lead will not have a significant effect. Finally, as the span becomes smaller, the advantages of asymmetrical mounting become less significant, and a shorter span symmetrical mounting may result in a lower thermal resistance than a longer span asymmetrical mounting.

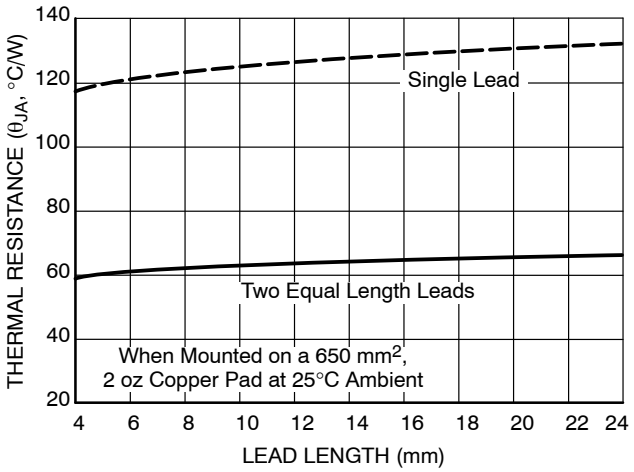
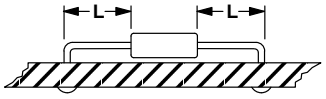
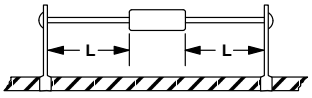


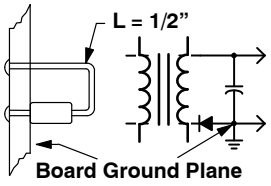
Figure 4. Approximate Thermal Resistance for DO–201AD Axial Lead Rectifiers as a Function of Lead Length



MOUNTING METHOD 1
P.C. Board Where Available
Copper Surface area is small



MOUNTING METHOD 2
Vector Push–In Terminals T–28



MOUNTING METHOD 3
P.C. Board with
Copper Surface of Area A

Figure 5. Mounting Methods for Axial Lead Parts

Table 1. TYPICAL VALUES FOR θ_{JA} IN STILL AIR (VALUES ON DEVICE DATASHEETS WILL BE MORE ACCURATE AND SHOULD BE USED WHEN AVAILABLE)

Package	Mounting Method	Lead Length L			
		1/8”	1/4”	1/2”	3/4”
DO–41	1	65	72	82	92
	2	74	81	91	101
	3	40°C/W (L = 3/8I, A = 2.25I ^{2})			
DO–201AD	1	50	51	53	55
	2	58	59	61	63
	3	28°C/W (L = 1/2I, A = 6.25I^2)			

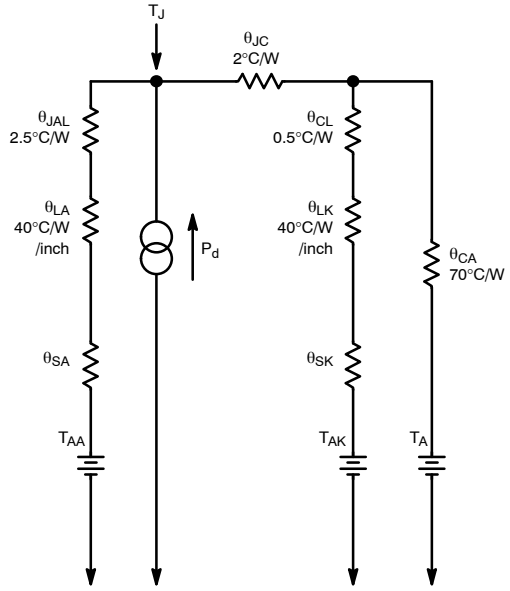


Figure 6. Approximate Thermal Model for Example 2

Table 2. DEFINITIONS FOR TERMS THERMAL MODEL FOR EXAMPLE 2

TEMPERATURES	THERMAL RESISTANCES
T_A = Ambient	θ_{CA} = Case–to–Ambient
T_{AA} = Anode Heat Sink Ambient	θ_{SA} = Anode Lead Heat Sink–to–Ambient
T_{AK} = Cathode Heat Sink Ambient	θ_{SK} = Cathode Lead Heat Sink–to–Ambient
T_{LA} = Anode Lead	θ_{LA} = Anode Lead
T_{LK} = Cathode Lead	θ_{LK} = Cathode Lead
T_J = Junction	θ_{CL} = Case to Cathode Lead
	θ_{JC} = Junction–to–Case*
	θ_{JAL} = Junction–to–Anode Lead

*Case temperature is referenced at cathode end.

Example 2: Calculating Junction Temperatures from a Generic Thermal Model

Compute the junction temperature and junction−to−ambient thermal resistance (using the generic thermal model in Figure 6), given the following:
Cathode Lead Length = 0.25 in
Anode Lead Length = 0.5 in
T_A = 60°C
T_{AA} = 70°C
T_{AK} = 80°C
$\theta_{SA} = \theta_{SK}$ = 40°C/W (typical for printed circuit board wiring)
P_D = 2 W

PROCEDURE

Using the lead lengths, $R_{\theta SA}$, $R_{\theta SK}$, the data in Figure 6, and summing series resistances gives the thermal circuit in Figure 7A. This can be simplified by applying Thévenin's theorm to the thermal network (see Figure 7B), giving a junction temperature of 112.7°C. Considering the ambient temperature, the power dissipation in the part, and the junction temperature, the effective thermal resistance junction to ambient can be calculated.

$$\Delta T = P_D \times R_{eff} \quad \text{(eq. 13)}$$

$$R_{eff} = (T_J - T_A)/P_D \quad \text{(eq. 14)}$$

$$R_{eff} = (112.7^\circ C - 60^\circ C)/2\ W \quad \text{(eq. 15)}$$

$$R_{eff} = 26.4^\circ C/W \quad \text{(eq. 16)}$$

However, this resistance is specific to the operating conditions, and would not be expected to stay the same if the ambient, heatsink, or power dissipation changed. More generally, describing the thermal properties of an axial lead part with a single thermal resistance number must be used with caution, because the ambient temperature is generally not the same as the temperature at the effective heat sink of the leads. Furthermore, with an asymmetrically mounted part, the asymmetrical thermal resistance will result in asymmetrical heat flow and asymmetrical lead temperatures. If the mounting points are not both at the ambient temperature, the single effective thermal resistance number will give less accurate results than a more detailed thermal model. In some cases, this representation could be improved by replacing the T_{AA} and T_{AK} with thermal resistances to the ambient temperature, and by adding a thermal resistance from the anode to the cathode through the board.

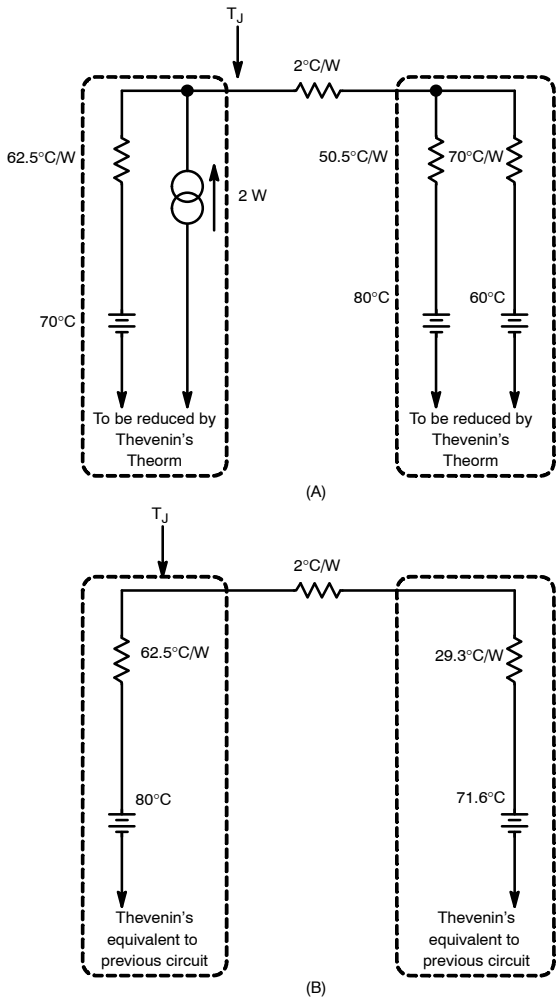


Figure 7. Circuit for Example 2, Simplified by Summing Series Resistances (A) and by Thévenin's Theorem Applied Separately to Both Sides of the Circuit (B)

THERMAL RC NETWORKS

Any arbitrary thermal network can be represented by thermal resistances, capacitances and time dependent temperatures. The quality of the thermal network is related to how accurately those resistances and capacitances represent the actual connections in the system. Obviously, reducing complicated sets of three dimensional objects, fluids and connections to a handful of nodes, resistances, and capacitances is an approximation. In many cases, only a few nodes in the system are actually important (the junction, the heatsink, the ambient air), so accurate results can be found using only a few thermal connections. In a more complicated system, it may be necessary to include more nodes, more capacitances, and more thermal resistances in order to accurately model the important points in the system.

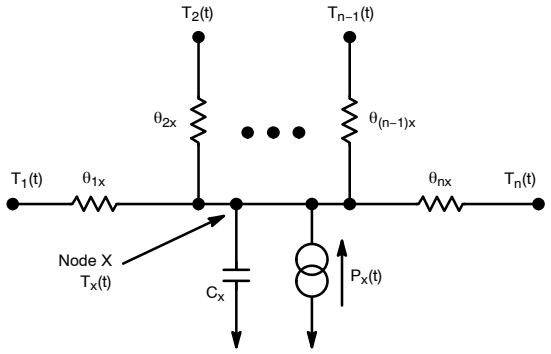


Figure 8. Arbitrary Thermal Network Relative to a Particular Node

It is possible to mathematically manipulate the power and temperature in the same fashion as voltage and current. The power dissipated at a node, power entering the node, and power leaving the node must be balanced (similar to Kirchhoff's current law), and the temperature changes around a closed temperature loop must sum to zero (similar to Kirchhoff's voltage law). Given the thermal resistance connections, the thermal capacitances, and the temperatures at the surrounding nodes, the temperature over time at a given node is a simple combination of the heat in, heat out, and heat stored.

$$P_x(t) - \sum_{i=1}^{n} \frac{T_x(t) - T_i(t)}{\theta_{ix}} = C_x \frac{dT_x(t)}{dt} \quad \text{(eq. 17)}$$

Where:

C_x = Thermal capacitance at the node, equal to the product of its mass and specific heat

For a system with multiple nodes, this will lead to a set of equations, one for every free node in the system. Depending on the information available, it is normally advantageous to reduce the number of nodes, so only things with useful physical meanings would be included (like device junctions, heatsinks, and the ambient environment), while all other terms would be lumped together wherever possible. The equations can then be solved simultaneously by standard mathematical methods, including Fourier transforms and linear algebra, like a typical electrical network.

Grounded and Non−Grounded Thermal Models

Thermal behavior could be modeled with a network of any arbitrary shape, with any set of connections, provided that the results accurately reflect the system being modeled. Depending on how the thermal capacitors are connected, these are referred to as grounded and non−grounded models. In a grounded model, each thermal capacitance is represented as a capacitance to thermal ambient (ground). In a non−grounded model, a least one thermal capacitance is represented as a capacitance between adjacent nodes (see Figures 9 and 10).

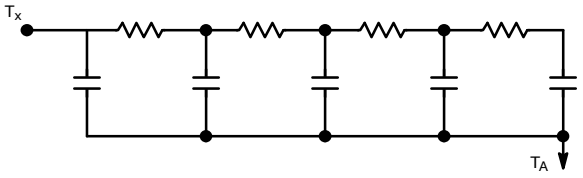


Figure 9. Grounded Thermal Model for a Resistance Path (Cauer Ladder)

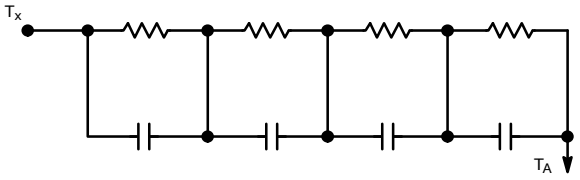


Figure 10. Non−Grounded Thermal Model for a Resistance Path (Foster Ladder)

Comparing grounded and non−grounded ladder structures, both models can be made mathematically equivalent for the two endpoints, T_X and T_A, but they will not be equivalent for each intermediate node along the path. In the grounded model, the intermediate nodes could potentially correspond to physical locations on the path, which could be measured. The non−grounded model may be computationally easier to work with, and mathematically equivalent for the endpoints, however the intermediate nodes will not have any physical meaning. This is due to a fundamental difference between stored charge and stored heat. At first glance, the equations for heat storage and charge storage (on a capacitor) appear very similar (see Equations 18 and 19). Equating heat with current; capacitance with the volume, density, specific heat product; and temperature with potential, they are almost identical. However, temperature is absolute, and potential is relative. Voltages always represent the potential difference between two points (as in Equation 18). For heat transfer, only the absolute temperature matters (as in Equation 19).

$$i = C \cdot \frac{\partial}{\partial t}(V_1 - V_2) \quad \text{(eq. 18)}$$

Where:
i = Current (charge per unit time) flowing into the capacitor
c = Capacitance of the capacitor
$V_1 - V_2$ = Potential difference between the two sides of the capacitor

$$Q = \rho \cdot V \cdot c \cdot \frac{\partial}{\partial t} T \qquad \text{(eq. 19)}$$

Where any temperature gradient across the object is ignored, and:
Q = Heat stored in the object
ρ = Density of the object
V = Volume of the object
c = Specific heat of the object
T = Temperature of the object

For example, consider a capacitor with stored charge, with the negative end grounded. The stored charge produces a voltage at the positive end of the capacitor (V_{cap}). If the negative end of the capacitor is connected to a node at some potential, (V_{in}), then the potential at the positive end of the capacitor instantly increases (V_{in} + V_{cap}), because the potential difference across the capacitor is constant for a given charge on the capacitor. The same is not true in the thermal equivalent. Using a similar example, consider a block of some known mass heated to a given temperature (T_{cap}), sitting in an ambient environment. It has a thermal capacitance, and it has stored heat, but no matter what it is connected to, or how it is connected, there will not be an instantaneous temperature change. If the ambient temperature changes instantly (T_{in}), the block may heat or cool over time, but the instantaneous temperature of the block at the moment the environment changes will be the same (T_{cap}). There is no way to stack temperature differences across thermal capacitors the same way voltage differences can be stacked across electrical capacitors.

Unlike electrical capacitors, thermal capacitors must have one side of the capacitor grounded to have any physical meaning. However, non−grounded models can still work mathematically, and while the intermediate nodes may not represent any physical locations, non−grounded models can still generate accurate results, and may be computationally advantageous. Lastly, it is extra effort to force the model to accurately produce the response of additional intermediate nodes, and depending on the complexity of the system it may not be possible anyway. If the extra nodes can be measured, than it might improve the model, but just because grounded capacitor networks could be physically accurate for intermediate nodes does not mean that they are, or that there would be an advantage to having them physically accurate for the intermediate nodes. As a result, either type of model may be used, depending on the circumstances.

Thermal Response Curves

A practical method of handling the transient thermal problem is to measure the thermal response of the semiconductor to a step of input power. Initially, the thermal resistance will be negligible, and as time passes it will increase until it eventually reaches the steady−state thermal resistance. The power dissipation and temperature change can be measured and plotted with time (see Figures 11, 12, and 13). The response over time is referred to as the single pulse duty cycle curve, because the thermal resistance at a given time is equal to the effective thermal resistance at the end of a single pulse, if the pulse duration is the same as the given time. This distinction is important for understanding duty cycle curves, which measure the response to a periodic input (see Periodic Response and Duty Cycle Curves section on Page 15).

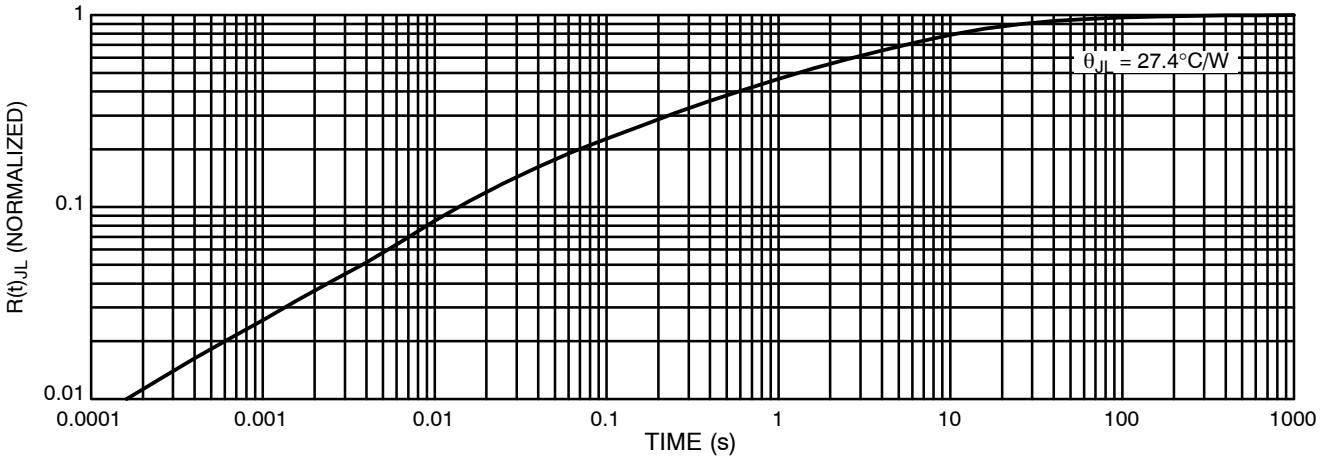


Figure 11. Transient Thermal Response, r(t), Normalized to Steady State Thermal Resistance

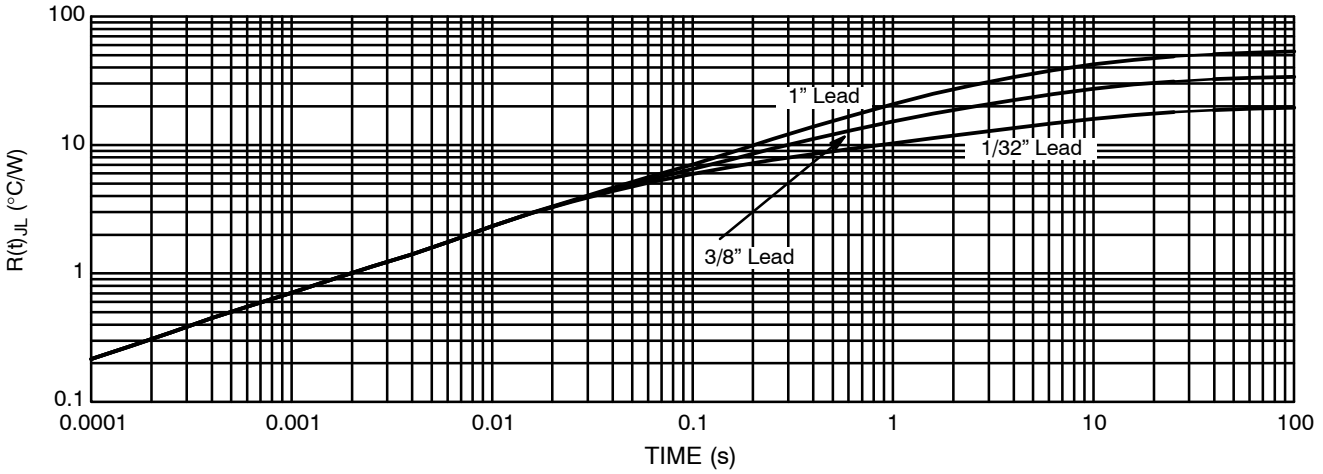


Figure 12. Transient Thermal Response, $R(t)_{JL}$, For the Same Part with Different Lead Lengths

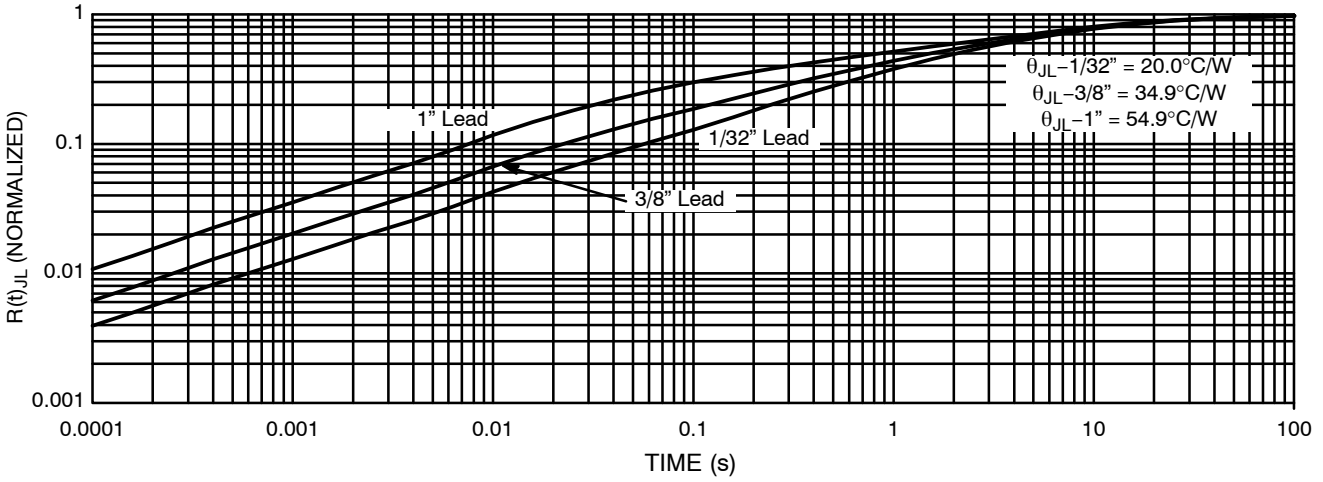


Figure 13. Transient Thermal Response, r(t), for Different Lead Lengths, Normalized to Steady–State Thermal Resistances for Each Lead Length

This transient thermal impedance may be normalized to a specific thermal resistance:

$$R_{Jx}(t) = r(t) \cdot \theta_{Jx} \quad \text{(eq. 20)}$$

Where:
r(t) = Fraction of steady state value at a given time (the normalized transient response)
θ_{Jx} = Thermal resistance, junction to a reference point (x)

The choice of reference point depends on the type of part (the case for case−mounted parts, the leads or ambient for lead−mounted parts – and the subscript 'x' is replaced with an appropriate letter to denote the reference point). Datasheets may contain plots of thermal resistances over time which may or may not be normalized to a steady−state thermal resistance (see Figures 11 and 12). Normalized curves present unitless data; to perform useful calculations, normalized thermals responses must first be scaled up by the resistance the curve is normalized to. Plots of data that are not normalized will have units (usually °C/W). Once the data has been scaled appropriately, it can be used to find junction temperatures over time, provided that the conditions of the test match the conditions being calculated for (including, but not limited to, lead lengths, board heatsinking capabilities, ambient airflow and ambient temperatures).

Superposition of Thermal Responses

For an arbitrary pulse train, which is not periodic, the superposition principle allows the summation of the individual power pulse effects to calculate the resulting junction temperature. Complex power inputs may be thought of as combinations of step inputs, and the response of the system is the sum of the step inputs:

$$\Delta T(t) = \sum_{i=1}^{n} P_i \cdot R\left(t - t_i\right) \quad \text{(eq. 21)}$$

Where:
P_i = power of input i
t_i = time step input i is applied
R(t) = measured transient thermal response of the device to an input power step of duration t
n = number of power contributions

As long as the input can be broken down into a sum of step inputs, then the junction temperature can be calculated by superposition (see Figure 14). A ramp may be crudely represented by a sum of equal, time delayed step functions, and a pulse may be represented by a step up added to a time delayed step down.

Example 3: Calculating Transient Junction Temperatures by Superposition

Given a measured thermal response (note that for this example the thermal response was empirically fitted from measured data, and that this will only be accurate for the device measured, under specific conditions, and only for a limited range), find the junction temperature rise as a function of time, and the maximum change in temperature, given a square pulse of input power.

Thermal Response:

$$R_{Jx}(t) = 1.5 - \frac{1.4}{\sqrt{t}} \text{ in } °C/W \quad \text{(eq. 22)}$$

Where:
t = Time, in ms

Power Input:

$$P_D(t) = 5 \text{ W} \quad \text{for } 0 \le t \le 1 \text{ ms} \quad \text{(eq. 23)}$$

$$P_D(t) = 0 \quad \text{otherwise} \quad \text{(eq. 24)}$$

Assume all other conditions for the circuit (board set up, airflow, ambient temperature, etc) are the same as the conditions for the measured step response.

PROCEDURE

The input may be described as the sum of two step functions:

$$P_D(t) = P_{D1}(t) + P_{D2}(t) \quad \text{(eq. 25)}$$

Where:

$$P_{D1}(t) = 5 \text{ W} \quad \text{for } t \ge 0 \quad \text{(eq. 26)}$$

$$P_{D2}(t) = -5 \text{ W} \quad \text{for } t > 1 \text{ ms} \quad \text{(eq. 27)}$$

Initially, only the first input step will affect the temperature change. Solving for the temperature change due to the first step, with time in ms:

$$\Delta T(t) = P_{D1}(t) R_{Jx}(t) \text{ for } 0 \le t \le 1 \text{ ms} \quad \text{(eq. 28)}$$

$$\Delta T(t) = 5\left(1.5 - \frac{1.4}{\sqrt{t}}\right) \text{ for } 0 \le t \le 1 \text{ ms} \quad \text{(eq. 29)}$$

$$\Delta T(t) = 7.5 - \frac{7}{\sqrt{t}} \text{ for } 0 \le t \le 1 \text{ ms} \quad \text{(eq. 30)}$$

Using the formula for superposition:

$$\Delta T(t) = \sum_{n=0}^{\infty} P_n \cdot R_{Jx}(t - t_n) \quad \text{(eq. 31)}$$

Substituting the input steps:

$$\Delta T(t) = P_{D1}(t) R_{Jx}\left(t - t_1\right) + P_{D2}(t) R_{Jx}\left(t - t_2\right) \quad \text{(eq. 32)}$$

Solving for the temperature change due to both steps, with time in ms:

$$\Delta T(t) = \left(7.5 - \frac{7}{\sqrt{t}}\right) + \left(\frac{7}{\sqrt{t-1}} - 7.5\right) \text{ for } t > 1 \text{ ms} \quad \text{(eq. 33)}$$

$$\Delta T(t) = \frac{7}{\sqrt{t-1}} - \frac{7}{\sqrt{t}} \text{ for } t > 1 \text{ ms} \quad \text{(eq. 34)}$$

Together, Equations 33 and 34 describe the junction temperature over time. The maximum temperature rise occurs at the end of the power input, at t = 1 ms.

$$\Delta T(1) = 0.5°C$$

Superposition of Rectangular Pulses

To solve for the effects due to a single pulse, that pulse can be represented by the superposition of two step inputs. The first step occurs at the start of the pulse, with a magnitude equal to that of the pulse. The second step occurs at the end of the pulse, with a magnitude opposite that of the pulse.

$$\Delta T(t) = P \cdot \left[R(t - t_1) - R_{Jx}(t - t_2)\right] \quad \text{(eq. 35)}$$

Where:
P = power of input pulse
t_1 = pulse start time
t_2 = pulse end time

For a series of pulses, the junction temperature at the end of the n^{th} pulse is the algebraic sum of all preceding pulse contributions.

$$T(t_{n,end}) = \sum_{i=1}^{n} P_i\left[R\left(t_{n,end} - t_{i,start}\right) - R\left(t_{n,end} - t_{i,end}\right)\right] \quad \text{(eq. 36)}$$

Where:
P_i = power of input pulse i
t_i = timing of pulse i

While the effects of multiple pulses can be summed, the time dependence still makes the timing of the pulses significant. A small pulse followed by a large pulse will generate different temperatures than a large pulse followed by a small pulse, and adjacent or overlapping pulses generate different temperatures than widely spaced pulses. However, as long as the timing and pulse height are accurate, the resulting temperature can be calculated for any combination of rectangular pulses, and for any time. This technique is called the pulse−by−pulse method.

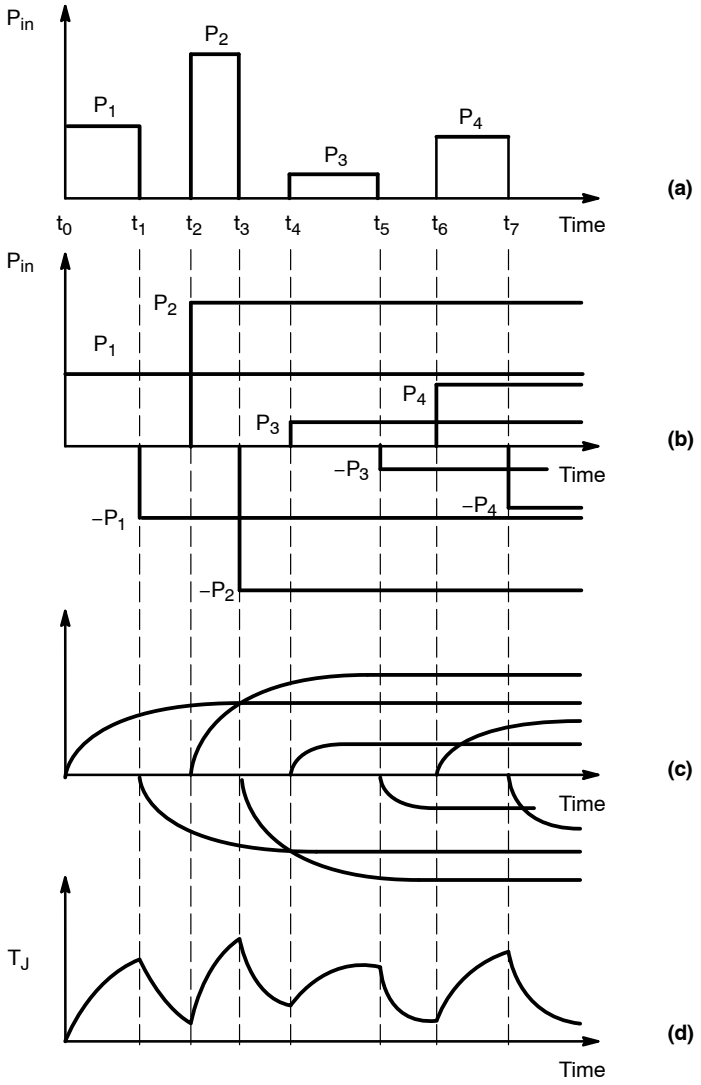


Figure 14. Superposition Applied to Junction Temperatures
(a) Power Dissipation in the Device
(b) Power Dissipation Represented by an Equivalent Set of Step Functions
(c) Temperature Change With Time for Each Step Function Separately
(d) The Final Junction Temperature Over Time, Given by the Sum of the Step Responses

When modeling power surges or overloads that occur within uniform trains of repetitive pulses, more accurate answers can be obtained with less work by using a model based on averaging the power pulses (see Figure 15). The average power is followed by one pulse of the repetitive train and then the overload pulse. The temperature is calculated at the end of the surge or overload.

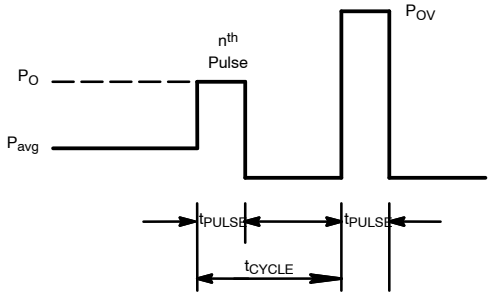


Figure 15. Model for a Repetitive Equal Pulse Train During Overload

Example 4: Temperature Changes Due to a Set of Pulses

Given three power input pulses (in Table 3, see Figure 16), using the transient response in Figure 12, find the temperature at the end of each pulse.

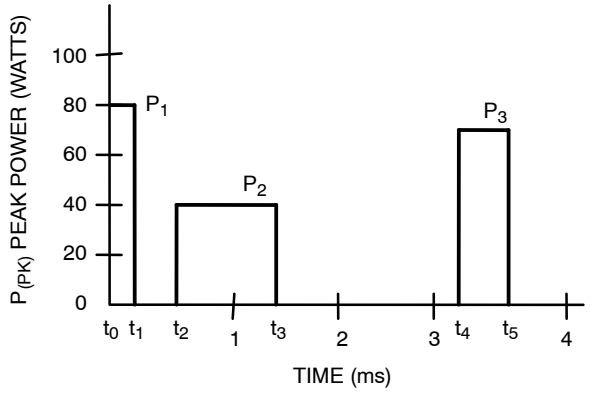


Figure 16. Power Pulse Train (for Example 4)

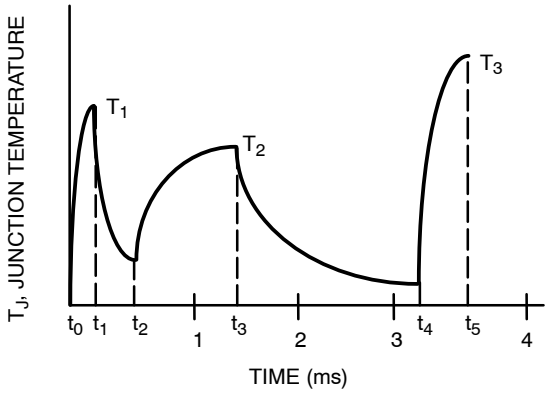


Figure 17. Resulting Junction Temperature (for Example 4)

Table 3. INPUT PULSES FOR EXAMPLE 4

P_1 = 80 W	t_0 = 0	t_1 = 0.1 ms
P_2 = 40 W	t_2 = 0.3 ms	t_3 = 1.3 ms
P_3 = 70 W	t_4 = 3.3 ms	t_5 = 3.5 ms

PROCEDURE

The temperature at the end of each pulse is a combination of the terms for all previous pulses, by superposition.

$$T_1 = P_1 \cdot R(t_1) \quad \text{(eq. 37)}$$

$$T_2 = P_1 \cdot \left[R(t_3) - R(t_3 - t_1)\right] + P_2 \cdot R(t_3 - t_2) \quad \text{(eq. 38)}$$

$$T_3 = P_1 \cdot \left[R(t_5) - R(t_5 - t_1)\right] + P_2 \cdot \left[R(t_5 - t_2) - R(t_5 - t_3)\right] + P_3 R(t_5 - t_4) \quad \text{(eq. 39)}$$

Simply finding the appropriate thermal resistances, for the specified durations, and substituting them into the above equations will give the peak temperatures. However, examining the transient response in Figure 12, reading accurate R(t) values from the curve is not possible. To get around this difficulty, the values will be estimated by power law interpolation.

The resistances in Figure 12 are basically linear for small time values (when plotted on a log scale). This corresponds to a function of the form in Equation 40.

$$R(t) = a \cdot t^n \quad \text{(eq. 40)}$$

The constant of proportionality (a) can be determined from any point on the curve, and the exponent (n) can be determined from any two points on the curve based on the constant of proportionality being constant.

$$a = \frac{R(t_1)}{{t_1}^n} = \frac{R(t_2)}{{t_2}^n} \quad \text{(eq. 41)}$$

Equation 41 can be solved for the exponent (n).

$$n = \frac{\log\left[\frac{R(t_2)}{R(t_1)}\right]}{\log\left[\frac{t_2}{t_1}\right]} \quad \text{(eq. 42)}$$

Picking two distant points from the linear portion of the curve, 0.22°C/W at 0.0001s, and 3.3°C/W at 0.02s, and solving for the proportionality constant and exponent gives an approximation for the form of the R(t) curve.

$$a = 24.4 \quad \text{(eq. 43)}$$

$$n = 0.51 \quad \text{(eq. 44)}$$

$$R(t) = 24.4 \cdot t^{0.51} \,^\circ\text{C/W} \quad \text{(eq. 45)}$$

R(t) values for the pulse durations in Equations 37, 38, and 39 can be found using Equation 45.

Table 4. TIME DEPENDENT THERMAL RESISTANCE VALUES FOR EXAMPLE 4

	Time (ms)	R(t) (°C/W)
t1	0.1	0.223
t2	0.3	0.390
t3	1.3	0.823
t4	3.3	1.32
t5	3.5	1.36
t3–t2	1	0.720
t3–t1	1.2	0.790
t5–t4	0.2	0.317
t5–t3	2.2	1.08
t5–t2	3.2	1.30
t5–t1	3.4	1.34

Finally the thermal resistances can be used in Equations 37, 38 and 39 to determine the resulting temperature changes (see Table 5).

PERIODIC RESPONSES AND DUTY−CYCLE CURVES

The maximum junction temperature for a given periodic power dissipation can be calculated using the transient thermal response to a single input power step. With a periodic power input, the junction heats up when power is applied, and cools off when power is not being dissipated in the device. After many cycles, the heating and cooling will reach equilibrium, and the maximum junction temperature for the periodic input will stabilize. For an arbitrary case, the resulting temperature change can be calculated using superposition of an infinite train of pulses. This is commonly quoted in the form of the first or second order approximation (see Equations 46 and 47).

For a square wave power input, the first order approximation of the thermal resistance is:

$$R(f, D) = D \cdot \theta_{Jx}(\infty) + (1 - D)\theta_{Jx}(D/f) \quad \text{(eq. 46)}$$

For a square wave power input, the second order approximation of the thermal resistance is:

$$R(f, D) = D \cdot \theta_{Jx}(\infty) + (1 - D)\theta_{Jx}(D/f + 1/f) + \theta_{Jx}(D/f) - \theta_{Jx}(1/f) \quad \text{(eq. 47)}$$

Where:
D = positive duty cycle (as a fraction)
f = frequency of the waveform
When D is 1, the response will match the steady state thermal response of the package (constant power input). When D is 0, the resistance is equivalent to a single pulse response.

Square−wave duty cycle curves are often found in datasheets or handbooks. These present the effective thermal resistance for the device when a square wave power input is applied, given the positive duty cycle (D), and frequency positive power pulse.

Table 5. THERMAL CONTRIBUTIONS FROM EACH POWER PULSE IN EXAMPLE 4

Time	P1 Temperature Contribution (°C)	P2 Temperature Contribution (°C)	P3 Temperature Contribution (°C)	Total Temperature Change (°C)
End of P1	17.80	0.00	0.00	17.80
End of P2	2.63	28.80	0.00	31.44
End of P3	1.60	9.07	22.18	32.85

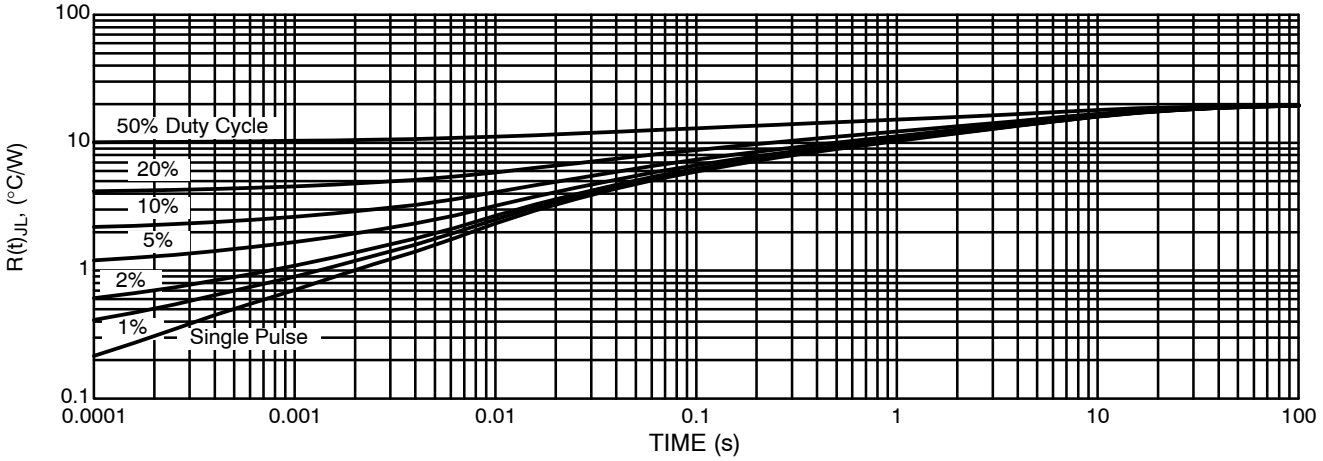


Figure 18. Thermal Resistance Over Time for Differing Square Wave Duty Cycles with a 1/32” Lead Length

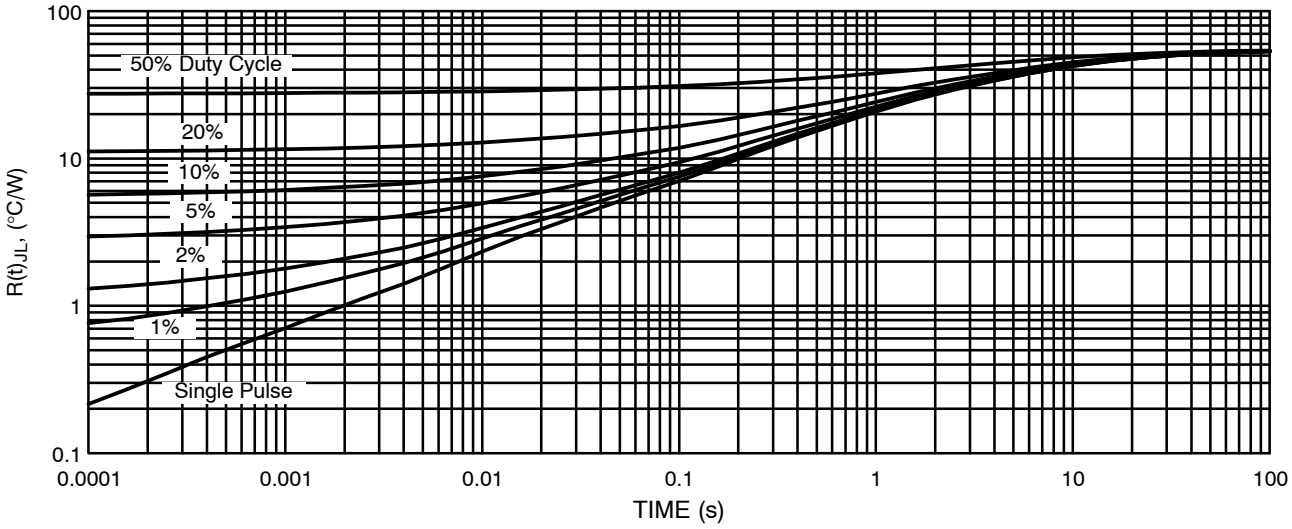


Figure 19. Thermal Resistance Over Time for Differing Square Wave Duty Cycles with a 1” Lead Length

In most datasheets, this will be plotted against ’t,’ which represents the on time of the pulse (t_{on}), not changes over time or the period of the signal (see Figures 18 and 19).

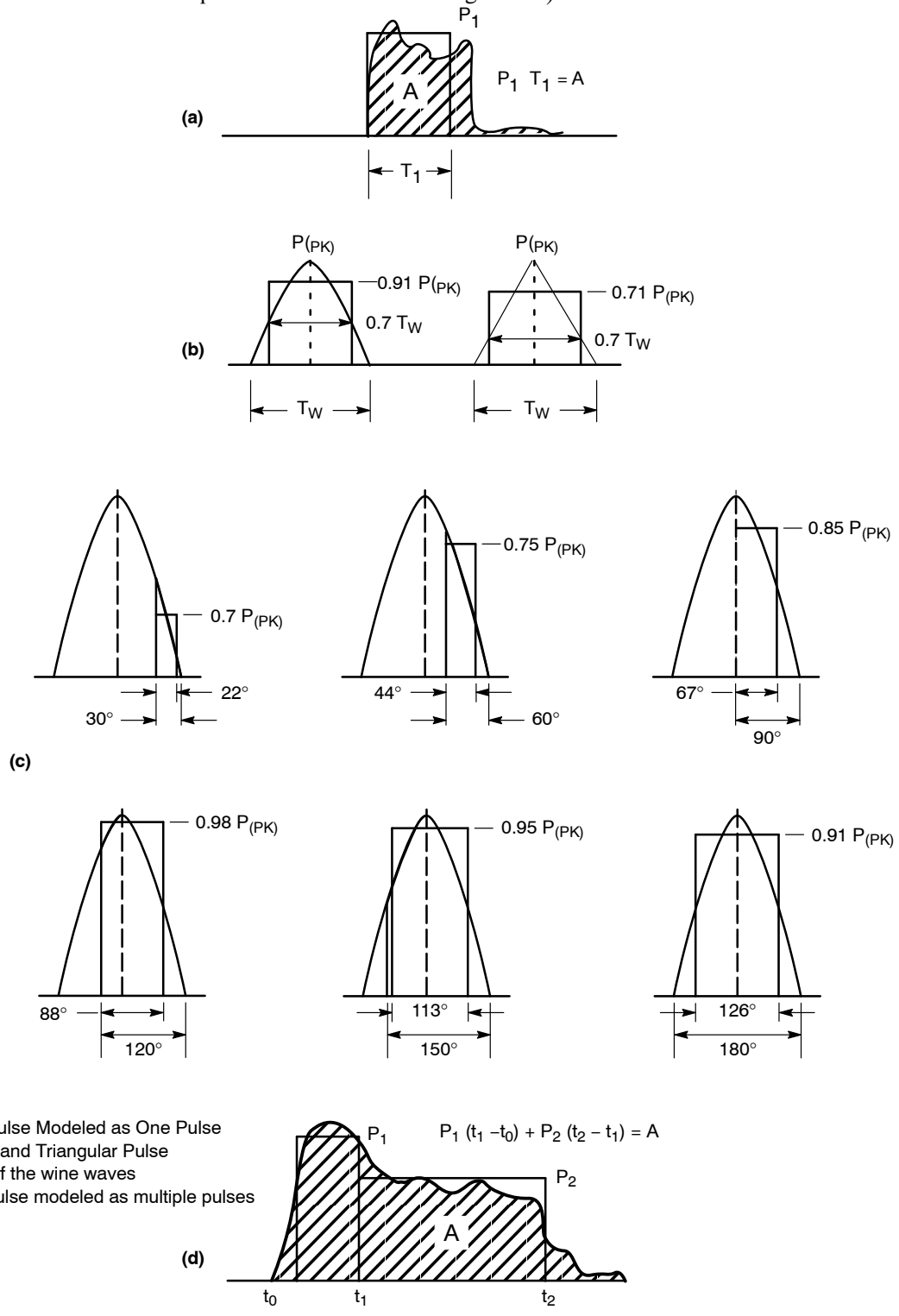
$$t_{on} = D/f \qquad \text{(eq. 48)}$$

Keep in mind that these duty cycle curves do not represent instantaneous temperature, but rather the peak temperature which is reached after an infinite number of such cycles have been repeated. Like the single pulse curves, results calculated this way are only valid for the test conditions under which the original thermal response data is measured.

Non−Rectangular Power Transients

Thermal response curves are based on a step change of power; the response will not be the same for other waveforms. Generally, a waveform that is not square can be approximated as a square wave of similar duration and total power. As long as the total power remains similar, the calculated results will be similar. Based on experience, square wave approximations of common waveforms have been developed (see Figure 20). For a pulse that is nearly rectangular, a square wave with equal peak amplitude, narrower width, and equal total area makes a conservative model. Sine wave, triangular, and $\sin^2$ power pulses can be modeled with square waves of reduced amplitude (91%, 71%, and 71% of peak, respectively, see Figure 20b) and reduced width (70% of the baseline width).

Rectifier diode forward power pulses are a combination of sin and $\sin^2$ waveforms if the current varies sinusoidally. In general, suitable modeling results if the amplitude waveform factor (F_A) is about 0.91 when the peak current is low, 0.71 when the peak current (and forward voltage drop) are high. Rectifiers used with SCRs in phase control circuits must handle current pulses that are fractions of sine waves (see Figure 20c, for SCR power loss empirically developed model rules; these are less conservative than the other model equivalents). Power pulses having more complex waveforms can be modeled as combinations of pulses (see Figure 20d).



(a) Arbitrary Pulse Modeled as One Pulse
(b) Sine wave and Triangular Pulse
(c) Fractions of the wine waves
(d) Arbitrary pulse modeled as multiple pulses

Figure 20. Models for Frequently Encountered Power Pulses

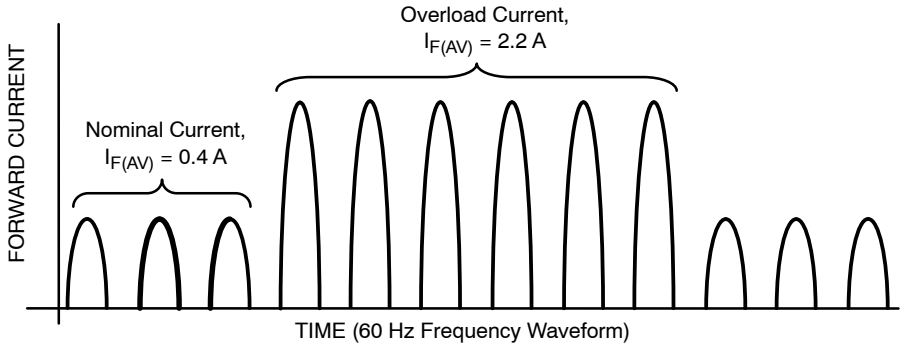


Figure 21. Overload Current Conditions (for Example 5)

The general formula for converting waveforms to equivalent square waves is to keep the total power (area) constant, while adjusting the peak power and duration (height and width).

$$T_M \cdot F_A \cdot P_{PK} = P_{AV} \cdot T_W \qquad \text{(eq. 49)}$$

or

$$T_M = \frac{P_{AV} \cdot T_W}{F_A \cdot P_{PK}} \qquad \text{(eq. 50)}$$

Where:
P_{AV} = average power in the original waveform
T_M = pulse width of model
T_W = time duration of original waveform
F_A = amplitude waveform factor
P_{PK} = peak power of original waveform

Results obtained from these substitutions are approximate; higher peak power, shorter duration waveforms do result in higher peak junction temperatures than lower peak power, longer waveforms even at the same total power dissipation.

Example 5: Maximum Junction Temperature During Overload

Given a rectifier performing half−wave rectification on a 60 Hz input, calculate the maximum junction temperature (relative to ambient) achieved after the device moves from standard operation (0.4 A peak forward current) to overload (2.2 A peak forward current, see Figure 21). Assume the device has reached steady state operation before the overload is applied, and that the overload current lasts for six cycles. Use the thermal response in Figure 12, with 3/8” leads.

Table 6. GIVEN INFORMATION FOR EXAMPLE 5

Average Power Dissipation at 0.4 A (AC, RMS)	P_0	0.4 W
Average Power Dissipation at 2.2 A (AC, RMS)	P_1	3.0 W
Peak Power Dissipation at 2.2 A (Instantaneous)	$P_{1,peak}$	12 W

PROCEDURE

Using the nominal operation, a steady state junction temperature can be calculated before the overload. The overload can be approximated by two square power pulses: one averaging the first five overload pulses, and then the sixth and final overload pulse. This will give an approximate value for the final junction temperature, and will only require the superposition of the steady state operation and three step responses (average overload for five cycles, off period before the final overload pulse, and then the final overload pulse itself).

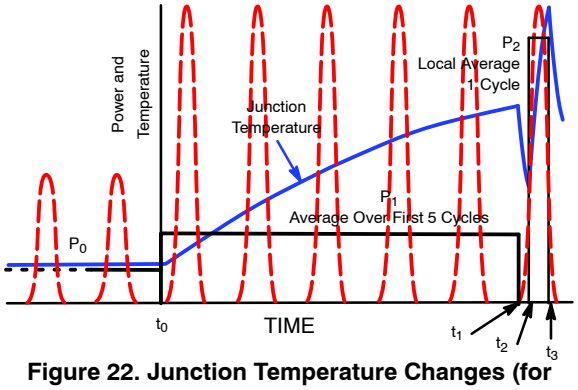


Figure 22. Junction Temperature Changes (for Example 5)

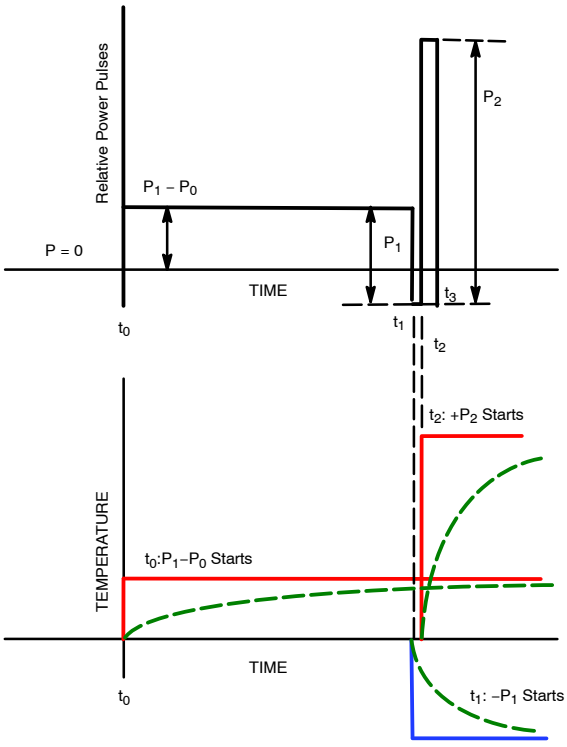


Figure 23. Junction Temperature Changes (for Example 5)

$$T_3 = P_0 \cdot \theta_{JA} + (P_1 - P_0) \cdot R(t_3 - t_0) - P_1 \cdot (t_3 - t_1) + P_2 \cdot R(t_3 - t_2) \quad \text{(eq. 51)}$$

The initial state is given by the average power dissipation during normal operation (P_0), and the steady state thermal response ($R(\infty)$, which is θ_{JA} from the steady state thermal model). The second step input is an increase from the steady state average power to the overload power, ($P_1 - P_0$), occurring at the time the overload starts (t_0, 0 ms). The third step input is the return from average overload to zero ($-P_1$), occurring before the final overload pulse (t_1, 5 full cycles after t_0, at 60 Hz).

$$t_1 = t_0 + 5 \cdot \frac{1}{f} = 0 \text{ ms} + \frac{5}{60 \text{ Hz}} = 83.3 \text{ ms} \quad \text{(eq. 52)}$$

The fourth and final input is the last overload pulse (P_2 at t_2), and it lasts half a cycle (until t_3). This requires approximating the sinusoidal pulse as a square wave ($P_2 = 0.91^* P_{1,peak}$, with its pulse width calculated by forcing equal total power for the new pulse, and the start time calculated by centering the pulse in the first half of the final overload cycle).

$$P_2 = 0.91 \cdot P_{1,peak} = 0.91 \cdot 12 \text{ W} = 10.9 \text{ W} \quad \text{(eq. 53)}$$

$$t_3 - t_2 = \frac{P_{AV} \cdot T_W}{F_A \cdot P_{PK}} = \frac{P_1 \cdot 1/f}{F_A \cdot P_{1,peak}} = \frac{3 \text{ W} \cdot 1/60 \text{ Hz}}{0.91 \cdot 12 \text{ W}} = 4.58 \text{ ms} \quad \text{(eq. 54)}$$

$$t_2 = t_1 + \frac{1}{2} \cdot \left[\frac{1}{2} \cdot \frac{1}{f} - (t_3 - t_2)\right] = 83.3 \text{ ms} + \frac{1}{2} \cdot \left[\frac{1}{2} \cdot \frac{1}{60 \text{ Hz}} - (4.58 \text{ ms})\right] = 85.2 \text{ ms} \quad \text{(eq. 55)}$$

At the end of this pulse (t_3), the junction will have reached the highest temperature for these inputs (T_3). As in Example 6, interpolation must be used to accurately estimate values from the thermal response (R(t) curve). This yields R(t) values which may be substituted into Equation 51.

Table 7. INTERPOLATED R(t) VALUES FOR EXAMPLE 5

t_3 = 89.8 ms	$R(t_3)$ = 6.24
$t_3 - t_2$ = 4.6 ms	$R(t_3 - t_2)$ = 1.57
$t_3 - t_1$ = 6.5 ms	$R(t_3 - t_1)$ = 1.87
Steady State	$R_{(inf)}$ = 34.9

Solving Equation 51 yields the maximum temperature increase.

$$T_3 = 41.7^\circ \text{C}$$

THERMAL RUNAWAY

Rectifier switching losses and reverse leakage current generally increase with temperature. Power dissipation in the rectifier can cause the junction temperature to increase, and as the junction temperature increases, the power losses increase. At the same time, the heat conducted, junction–to–ambient, will increase with junction temperature. Under most conditions, the power losses, temperature increases, and heat conduction will stabilize, and the device can operate normally. If the power losses outpace the heat conduction, and temperature increases do not stabilize, the device is said to be in thermal runaway. In thermal runaway, unless some other portion of the circuit limits the rectifier current, the device temperature will increase until the device is damaged or destroyed.

For a thermal system to be stable, the system must be capable of dissipating more heat than is generated. The system is at a stable operating point if the heat generated is equal to the heat conducted out of the package, and an increase in temperature will result in a greater increase in heat conduction than heat generation.

$$P_D(T_J) = \frac{T_J - T_a}{\theta_{JA}} \quad \text{(eq. 56)}$$

$$\frac{\partial P_D}{\partial T_J} < \frac{1}{\theta_{JA}} \quad \text{(eq. 57)}$$

This can be analyzed graphically [2]. If the operating points for the device are plotted (power dissipation as a function of junction temperature), and the thermal resistance of the system is plotted on the same graph (using ambient temperature as the x−intercept, and $1/\theta_{JA}$ as the slope), then the intersections of the curves will denote the possible operating points. At any temperature for which the resistance line is below the operating curve, the device temperature will be increasing as the device produces more heat than is conducted away. At any temperature for which the resistance line is above the operating curve, the temperature will be decreasing as the more heat is conducted out of the package than is produced at the junction. At the curve intersections, the heat production and heat conduction are balanced, and the device is at thermal equilibrium. Not all intersections are stable. At some equilibrium points, any extra power dissipation (from a small power transient) will cause the device to leave the stable point and enter thermal runaway (see Figure 24a). It is possible, with a poor combination of power level, high ambient temperature and system heatsinking ability, for a device to be in thermal runaway regardless of junction temperature. Graphically, this will occur when the operating curve and thermal resistance line do not intersect, or only intersect at a single unstable point (see Figure 24d).

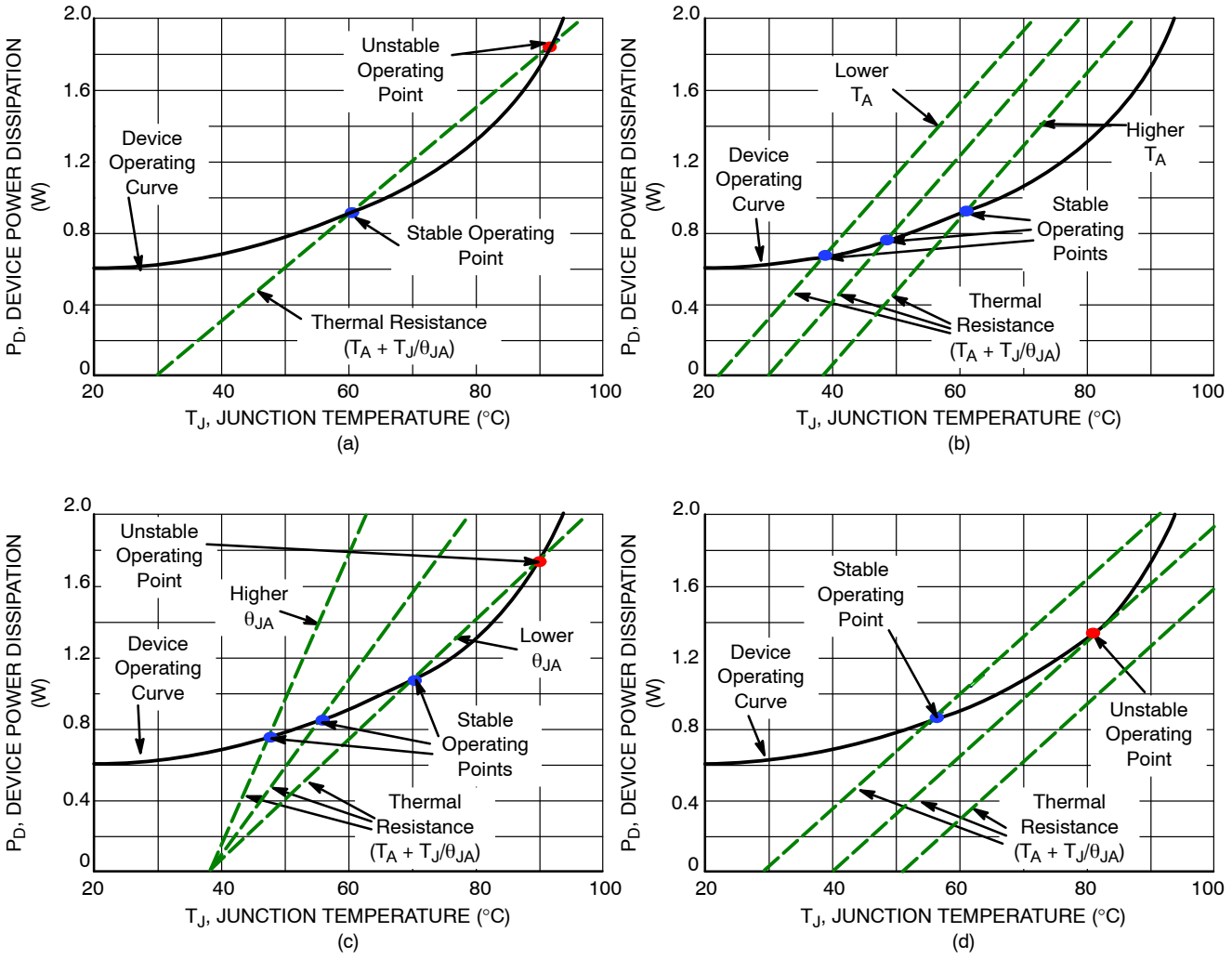


Figure 24. Graphical Analysis of Thermal Operation

(a) Finding a stable operating point
(b) Effect of ambient temperature changes on thermal operation
(c) Effect of junction to ambient thermal resistance changes
(d) Analysis including thermal resistance and ambient temperature combinations which do not have stable operating points

For rectifiers, leakage current, and therefore reverse bias power dissipation, typically follow a power–law relationship.

$$I_R(T) = I_o \cdot e^{\frac{T}{\lambda}} \quad \text{(eq. 58)}$$

Where:
I_o = a proportionality constant particular to the rectifier
λ = a constant particular to the temperature dependence of the rectifier, commonly between 14 and 15.

$$P_{R,avg}(T) = V_R \cdot \left(I_o \cdot e^{\frac{T}{\lambda}}\right) \quad \text{(eq. 59)}$$

I_o and λ can be found experimentally for the device, or estimated from the datasheet. Using these numbers, and Equations 56, 57, and 59, either the maximum allowable ambient temperature, minimum required thermal resistance, or maximum junction temperature can be solved for (given the other two). For forward conduction, the forward voltage and current would be used in place of the reverse voltage and current to find the device operating points. In addition, the operating points for a periodic application can be estimated (ignoring switching losses) by average power dissipations (forward and reverse, weighted by duty cycle) and equivalent thermal resistances (see Periodic Responses discussed previously).

THERMAL DESIGN

The datasheets for most discrete semiconductors will state the minimum and maximum operating and storage temperatures for the device; for rectifiers this is usually from −65°C up to 150°C or 175°C. While it is possible to operate a device at the maximum junction temperature for a short time, this parameter is the peak temperature the junction of the device can operate at. The normal operating point of the device junction in the application should be designed at a lower temperature. Operating a device at the maximum temperature risks failure from a transient thermal spike, and reduces the device lifetime. If the thermal characteristics of a system are insufficient for a device, there are three basic solutions:

- Reduce θ_{JA}. Increasing the copper area around the device in the board, increasing the copper thickness, adding a heatsink to the device, or increasing the airflow over the device will all decrease the thermal resistance to ambient and lower the junction operating temperature.
- Decrease the ambient temperature. Operating the device in a cooler environment will decrease the junction operating temperature.
- Change the device. A device with a larger die or a less thermally resistant package may decrease the overall thermal resistance of the system. Similarly, a device which dissipates less power in the application will also operate at a lower temperature. For zener rectifiers dealing with transient voltage spikes, a more thermally capacitive package may also reduce the maximum junction temperature. For other rectifiers, this could necessitate a device with a lower forward voltage drop, lower reverse leakage current, or lower switching charge, depending on the application.

With proper thermal design, the devices will function reliably for the full device lifetime.

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