# Schottky Power Rectifier, Switch Mode, 10 A, 35 V

# MBRD1035CTL, NRVBD1035VCTL, SBRD81035CTL Series

The MBRD1035CTL employs the Schottky Barrier principle in a large area metal-to-silicon power diode. State of the art geometry features epitaxial construction with oxide passivation and metal overlay contact. Ideally suited for low voltage, high frequency switching power supplies, free wheeling diode and polarity protection diodes.

#### **Features**

- Highly Stable Oxide Passivated Junction
- Guardring for Stress Protection
- Matched Dual Die Construction –
   May be Paralleled for High Current Output
- High dv/dt Capability
- Short Heat Sink Tap Manufactured Not Sheared
- Very Low Forward Voltage Drop
- Epoxy Meets UL 94 V-0 @ 0.125 in
- SBRD8 and NRVBD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### **Mechanical Characteristics:**

- Case: Epoxy, Molded
- Weight: 0.4 Gram (Approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead and Mounting Surface Temperature for Soldering Purposes: 260°C Max. for 10 Seconds
- ESD Rating:
  - Human Body Model = 3B (> 8 kV)
  - Machine Model = C (> 400 V)



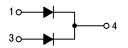
ON Semiconductor®

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# SCHOTTKY BARRIER RECTIFIER 10 AMPERES 35 VOLTS



DPAK CASE 369C



#### MARKING DIAGRAM



A = Assembly Location\*

Y = Year

WW = Work Week

B1035CL = Device Code

G = Pb-Free Package

\* The Assembly Location Code (A) is front side optional. In cases where the Assembly Location is stamped in the package bottom (molding ejecter

#### **ORDERING INFORMATION**

pin), the front side assembly code may be blank.

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

#### **MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V <sub>RRM</sub> V <sub>RWM</sub> V <sub>R</sub>	35	V
Average Rectified Forward Current (T <sub>C</sub> = 115°C) Per Leg Per Package	I <sub>O</sub>	5.0 10	А
Peak Repetitive Forward Current (Square Wave, Duty = 0.5, T <sub>C</sub> = 115°C) Per Leg	I <sub>FRM</sub>	10	А
Non-Repetitive Peak Surge Current (Surge applied at rated load conditions, halfwave, single phase, 60 Hz) Per Package	I <sub>FSM</sub>	50	Α
Storage / Operating Case Temperature	T <sub>stg,</sub> T <sub>c</sub>	-55 to +150	°C
Operating Junction Temperature (Note 1)	TJ	-55 to +150	°C
Voltage Rate of Change (Rated V <sub>R</sub> , T <sub>J</sub> = 25°C)	dv/dt	10,000	V/µs

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case Per Leg	$R_{ hetaJC}$	3.0	°C/W
Thermal Resistance, Junction-to-Ambient (Note 2) Per Leg	$R_{ hetaJA}$	137	°C/W

<sup>2.</sup> Rating applies when using minimum pad size, FR4 PC Board

## **ELECTRICAL CHARACTERISTICS**

Rating	Symbol	Value	Unit
$\label{eq:maximum Instantaneous Forward Voltage (Note 3) (See Figure 2)} \\ Per Leg \\ (I_F = 5 \text{ Amps, } T_J = 25^{\circ}\text{C}) \\ (I_F = 5 \text{ Amps, } T_J = 100^{\circ}\text{C}) \\ (I_F = 10 \text{ Amps, } T_J = 25^{\circ}\text{C}) \\ (I_F = 10 \text{ Amps, } T_J = 100^{\circ}\text{C}) \\ \end{aligned}$	V <sub>F</sub>	0.47 0.41 0.56 0.55	V
Maximum Instantaneous Reverse Current (Note 3) (See Figure 4) Per Leg $ (V_R=35 \text{ V}, T_J=25^\circ\text{C}) \\ (V_R=35 \text{ V}, T_J=100^\circ\text{C}) \\ (V_R=17.5 \text{ V}, T_J=25^\circ\text{C}) \\ (V_R=17.5 \text{ V}, T_J=100^\circ\text{C}) $	I <sub>R</sub>	2.0 30 0.20 5.0	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

<sup>1.</sup> The heat generated must be less than the thermal conductivity from Junction–to–Ambient:  $dP_D/dT_J < 1/R_{\theta JA}$ .

<sup>3.</sup> Pulse Test: Pulse Width ≤ 250 μs, Duty Cycle ≤ 2.0%

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>		
MBRD1035CTLG		75 Units / Rail		
SBRD81035CTLG*		75 Units / Rail		
SBRD81035CTLG-VF01*	DPAK	75 Units / Rail		
MBRD1035CTLT4G	(Pb-Free)	2,500 Units / Tape & Reel		
NRVBD1035VCTLT4G*		2,500 Units / Tape & Reel		
SBRD81035CTLT4G*		2,500 Units / Tape & Reel		

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### TYPICAL CHARACTERISTICS

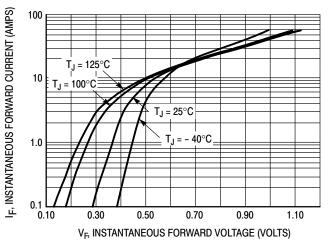


Figure 1. Typical Forward Voltage Per Leg

Figure 2. Maximum Forward Voltage Per Leg

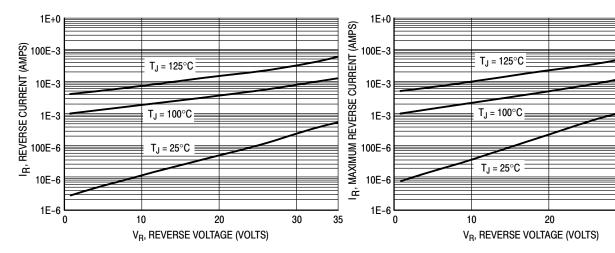


Figure 3. Typical Reverse Current Per Leg

Figure 4. Maximum Reverse Current Per Leg

35

<sup>\*</sup>SBRD8 and NRVBD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

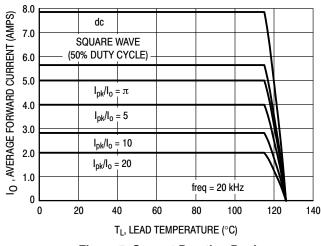


Figure 5. Current Derating Per Leg

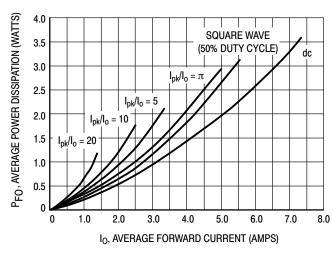


Figure 6. Forward Power Dissipation Per Leg

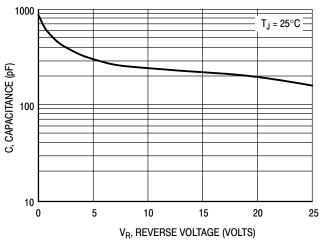


Figure 7. Capacitance Per Leg

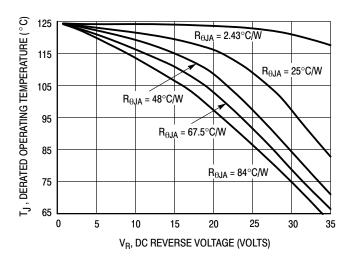


Figure 8. Typical Operating Temperature
Derating Per Leg \*

r(t) = thermal impedance under given conditions,

Pf = forward power dissipation, and

Pr = reverse power dissipation

This graph displays the derated allowable  $T_J$  due to reverse bias under DC conditions only and is calculated as  $T_J = T_{Jmax} - r(t)Pr$ , where r(t) = Rthja. For other power applications further calculations must be performed.

<sup>\*</sup> Reverse power dissipation and the possibility of thermal runaway must be considered when operating this device under any reverse voltage conditions. Calculations of  $T_J$  therefore must include forward and reverse power effects. The allowable operating  $T_J$  may be calculated from the equation:  $T_J = T_{Jmax} - r(t) (Pf + Pr) \text{ where}$ 

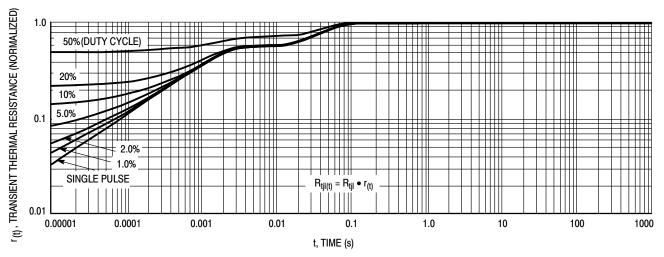


Figure 9. Thermal Response Junction to Case (Per Leg)

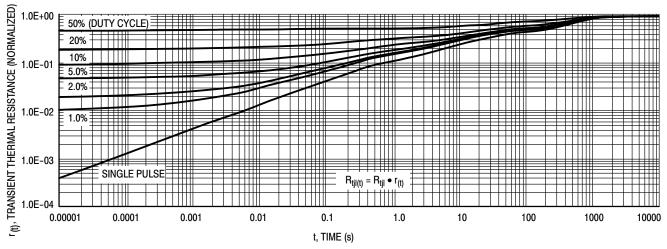
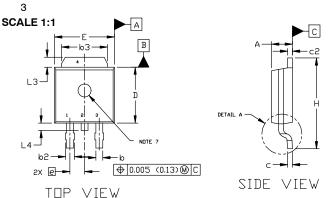


Figure 10. Thermal Response Junction to Ambient (Per Leg)

# **DPAK (SINGLE GAUGE)**

CASE 369C **ISSUE G** 

**DATE 31 MAY 2023** 

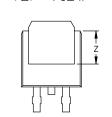


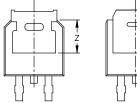


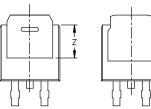
- DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994. CONTROLLING DIMENSION: INCHES
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS 63,
- L3. AND Z. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH,
  PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR
  GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE DUTERMOST EXTREMES OF THE PLASTIC BODY.

  DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
- OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
Α	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
С	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
е	0.090 BSC		2.29 BSC	
Н	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.050 B2C		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4		0.040		1.01
Z	0.155		3.93	





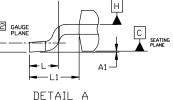


BOTTOM VIEW

5.80

BOTTOM VIEW ALTERNATE

CONSTRUCTIONS [0.228] 6.20 L2 GAUGE PLANE [0.244] 2.58 3.00 [0.102] [0.118] 1.60 [0.063] 6.17



STYLE 5: PIN 1. GATE

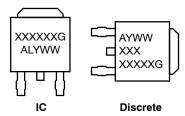
2. ANODE

3 CATHODE

ANODE

CW ROTATED 90°

#### **GENERIC MARKING DIAGRAM\***



= Device Code
= Assembly Location
= Wafer Lot
= Year
= Work Week
= Pb-Free Package

RECOMMENDED MOUNTING FOOTPRINT\* \*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DUWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

[0.243]

STYLE 1: PIN 1. BASE STYLE 2: PIN 1. GATE STYLE 3: PIN 1. ANODE STYLE 4: PIN 1. CATHODE 2. COLLECTOR 2. DRAIN 2. CATHODE 2. ANODE 3 SOURCE 3 FMITTER 3 ANODE 3 GATE

COLLECTOR 4. DRAIN 4. CATHODE 4. ANODE STYLE 6: STYLE 7: PIN 1. GATE 2. COLLECTOR STYLE 8: STYLE 9: PIN 1. MT1 2. MT2

STYLE 10: PIN 1. N/C 2. CATHODE 3. ANODE PIN 1. ANODE 2. CATHODE PIN 1. CATHODE 2. ANODE 3 CATHODE 3 FMITTER 3 RESISTOR ADJUST 4. COLLECTOR 4. CATHODE 4. ANODE CATHODE

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DPAK (SINGLE GAUGE)		PAGE 1 OF 1

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3 GATE

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