

1.8 V / 2.5 V 10 Gbps Equalizer Receiver with 1:6 Differential CML Outputs

Multi-Level Inputs W / Internal Termination

NB7VQ1006M

Description

The NB7VQ1006M is a high performance differential 1:6 CML fanout buffer with a selectable Equalizer receiver. When placed in series with a Data path operating up to 10 Gb/s, the NB7VQ1006M will compensate the degraded data signal transmitted across a FR4 PCB backplane or cable interconnect and output six identical CML copies of the input signal. Therefore, the serial data rate is increased by reducing Inter-Symbol Interference (ISI) caused by losses in copper interconnect or long cables.

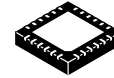
The Equalizer ENable pin (EQEN) allows the IN/IN inputs to either flow through or bypass the Equalizer section. Control of the Equalizer function is realized by setting EQEN; When EQEN is set Low, the IN/IN inputs bypass the Equalizer. When EQEN is set High, the IN/IN inputs flow through the Equalizer. The default state at startup is LOW. As such, the NB7VQ1006M is ideal for SONET, GigE, Fiber Channel, Backplane and other Data distribution applications.

The differential inputs incorporate internal 50 Ω termination resistors that are accessed through the VT pin. This feature allows the NB7VQ1006M to accept various logic level standards, such as LVPECL, CML or LVDS. This feature provides transmission line termination at the receiver, eliminating external components. The outputs have the flexibility of being powered by either a 1.8 V or 2.5 V supply.

The NB7VQ1006M is a member of the GigaComm™ family of high performance Clock/Data products.

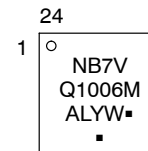
Features

- Maximum Input Data Rate > 10 Gbps
- Maximum Input Clock Frequency > 7.5 GHz
- Backplane and Cable Interconnect Compensation
- 225 ps Typical Propagation Delay
- 30 ps Typical Rise and Fall Times
- Differential CML Outputs, 400 mV Peak-to-Peak, Typical
- Operating Range: $V_{CC} = 1.71 \text{ V to } 2.625 \text{ V}$, $GND = 0 \text{ V}$
- Internal Input Termination Resistors, 50 Ω
- QFN-24 Package, 4 mm x 4 mm
- $-40^{\circ}\text{C to } +85^{\circ}\text{C}$ Ambient Operating Temperature
- This Device is Pb-Free, Halogen Free and is RoHS Compliant



QFN-24
MN SUFFIX
CASE 485L

MARKING DIAGRAM*

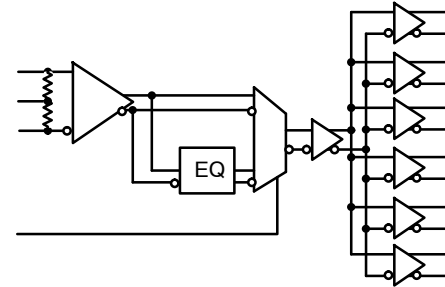


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note [AND8002/D](#).

SIMPLIFIED BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
NB7VQ1006MMNG	QFN-24 (Pb-Free)	92 Units / Tube
NB7VQ1006MMNTXG	QFN-24 (Pb-Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

NB7VQ1006M

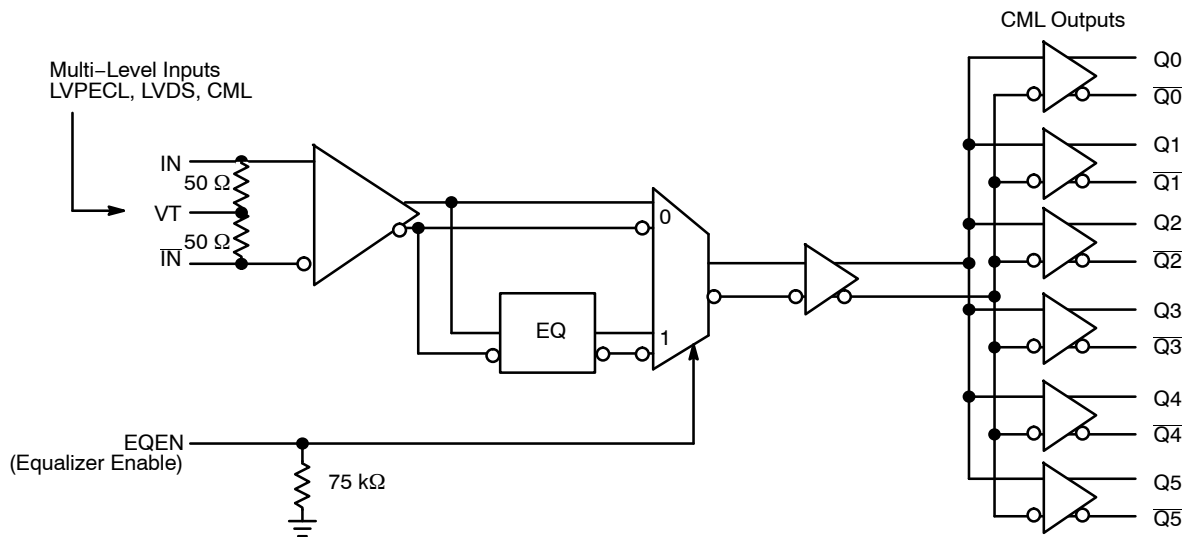


Figure 1. Detailed Block Diagram of NB7VQ1006M

Table 1. EQUALIZER ENABLE FUNCTION

EQEN	Function
0	IN/ $\overline{\text{IN}}$ Inputs Bypass the EQualizer Section
1	IN/ $\overline{\text{IN}}$ Inputs Flow through the EQualizer Section

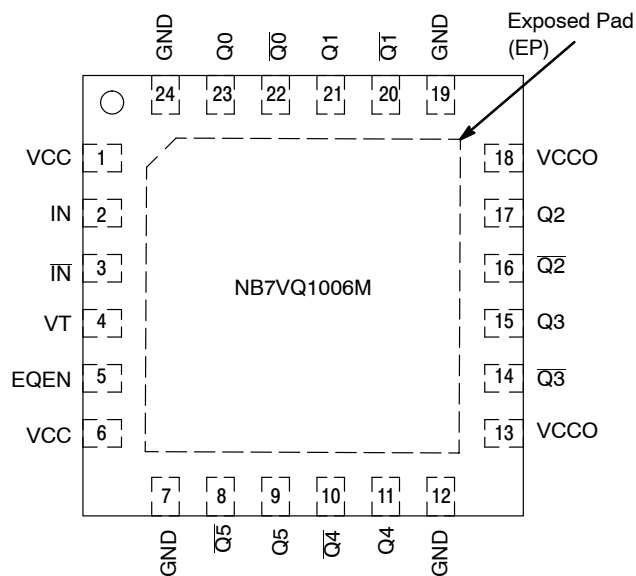


Figure 2. QFN-24 Lead Pinout (Top View)

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1	VCC		Positive Supply Voltage for the Core Logic
2	IN	LVPECL, CML, LVDS Input	Non-inverted Differential Clock/Data Input. (Note 1)
3	$\overline{\text{IN}}$	LVPECL, CML, LVDS Input	Inverted Differential Clock/Data Input. (Note 1)
4	VT		Internal 50 Ω Termination Pin for IN and $\overline{\text{IN}}$
5	EQEN	LVC MOS Input	Equalizer Enable Input; pin will default LOW when left open (has internal pull-down resistor)
6	VCC		Positive Supply Voltage for the Core Logic
7	GND		Negative Supply Voltage
8	$\overline{\text{Q5}}$	CML	Inverted Differential Output. Typically terminated with 50 Ω resistor to V_{CC} .
9	Q5	CML	Non-inverted Differential Output. Typically terminated with 50 Ω resistor to V_{CC} .
10	$\overline{\text{Q4}}$	CML	Inverted Differential Output. Typically terminated with 50 Ω resistor to V_{CC} .
11	Q4	CML	Non-inverted Differential Output. Typically terminated with 50 Ω resistor to V_{CC} .
12	GND		Negative Supply Voltage
13	VCCO		Positive Supply Voltage for the pre-amplifier and output buffer
14	$\overline{\text{Q3}}$	CML	Inverted Differential Output. Typically terminated with 50 Ω resistor to V_{CC} .
15	Q3	CML	Non-inverted Differential Output. Typically terminated with 50 Ω resistor to V_{CC} .
16	$\overline{\text{Q2}}$	CML	Inverted Differential Output. Typically terminated with 50 Ω resistor to V_{CC} .
17	Q2	CML	Non-inverted Differential Output. Typically terminated with 50 Ω resistor to V_{CC} .
18	VCCO		Positive Supply Voltage for the pre-amplifier and output buffer
19	GND		Negative Supply Voltage
20	$\overline{\text{Q1}}$	CML	Inverted Differential Output. Typically terminated with 50 Ω resistor to V_{CC} .
21	Q1	CML	Non-inverted Differential Output. Typically terminated with 50 Ω resistor to V_{CC} .
22	$\overline{\text{Q0}}$	CML	Inverted Differential Output. Typically terminated with 50 Ω resistor to V_{CC} .
23	Q0	CML	Non-inverted Differential Output. Typically terminated with 50 Ω resistor to V_{CC} .
24	GND		Negative Supply Voltage
–	EP	–	The Exposed Pad (EP) on the QFN–24 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to GND and is recommended to be electrically connected to GND on the PC board.

1. In the differential configuration when the input termination pin (VT) is connected to a common termination voltage or left open, and if no signal is applied on IN/ $\overline{\text{IN}}$, then the device will be susceptible to self-oscillation.
2. All VCC, VCCO and GND pins must be externally connected to the same power supply voltage to guarantee proper device operation.

Table 3. ATTRIBUTES

Characteristics	Value
ESD Protection Human Body Model Machine Model	> 4 kV > 200 V
Moisture Sensitivity (Note 1)	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	244
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC} , V_{CCO}	Positive Power Supply	GND = 0 V		3.0	V
V_I	Input Voltage	GND = 0 V		-0.5 to $V_{CC} + 0.5$	V
V_{INPP}	Differential Input Voltage $ I_N - \bar{I}_N $			1.89	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)			± 40	mA
I_{OUT}	Output Current Through R_T (50 Ω Resistor)			± 40	mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 1) TGSD 51-6 (2S2P Multilayer Test Board) with Filled Thermal Vias	0 lfpm 500 lfpm	QFN-24 QFN-24	37 32	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	QFN-24	11	°C/W
T_{sol}	Wave Solder (Pb-Free)			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

NB7VQ1006M

Table 5. DC CHARACTERISTICS – CML OUTPUT ($V_{CC} = V_{CCO} = 1.71 \text{ V}$ to 2.625 V ; $GND = 0 \text{ V}$ $T_A = -40^\circ\text{C}$ to 85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
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POWER SUPPLY CURRENT (Inputs and Outputs open)

I_{CC}	Power Supply Current, Core Logic $V_{CC} = 2.5\text{V}$		100	115	mA
I_{CCO}	$V_{CC} = 1.8\text{V}$		85	95	
	Power Supply Current, Outputs $V_{CCO} = 2.5\text{V}$		180	200	
	$V_{CCO} = 1.8\text{V}$		150	175	

CML OUTPUTS (Notes 1 and 2) (Figure 10)

V_{OH}	Output HIGH Voltage $V_{CCO} = 2.5 \text{ V}$ $V_{CCO} = 1.8 \text{ V}$	$V_{CCO} - 40$ 2460 1760	$V_{CCO} - 10$ 2490 1790	V_{CCO} 2500 1800	mV
V_{OL}	Output LOW Voltage $V_{CCO} = 2.5\text{V}$ $V_{CCO} = 2.5\text{V}$ $V_{CCO} = 1.8\text{V}$ $V_{CCO} = 1.8\text{V}$	$V_{CCO} - 600$ 1900 $V_{CCO} - 525$ 1275	$V_{CCO} - 500$ 2000 $V_{CCO} - 425$ 1375	$V_{CCO} - 400$ 2100 $V_{CCO} - 300$ 1500	mV

DATA/CLOCK INPUTS (I_N , $\bar{I}_N$) (Note 3) (Figures 6 & 7)

V_{IHD}	Differential Input HIGH Voltage	1100		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	GND		$V_{CC} - 100$	mV
V_{ID}	Differential Input Voltage ($V_{IHD} - V_{ILD}$)	100		1200	mV
I_{IH}	Input HIGH Current	-150	30	+150	μA
I_{IL}	Input LOW Current	-150	-40	+150	μA

CONTROL INPUTS (EQEN)

V_{IH}	Input HIGH Voltage	$V_{CC} \times 0.65$		V_{CC}	mV
V_{IL}	Input LOW Voltage	GND		$V_{CC} \times 0.35$	mV
I_{IH}	Input HIGH Current	-150	25	+150	μA
I_{IL}	Input LOW Current	-150	10	+150	μA

TERMINATION RESISTORS

R_{TIN}	Internal Input Termination Resistor	45	50	55	Ω
R_{TOUT}	Internal Output Termination Resistor	45	50	55	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. CML outputs loaded with 50Ω to V_{CC} for proper operation.
2. Input and output parameters vary 1:1 with V_{CC}/V_{CCO} .
3. V_{IHD} , V_{ILD} , V_{ID} and V_{CMR} parameters must be complied with simultaneously.

NB7VQ1006M

Table 6. AC CHARACTERISTICS ($V_{CC} = V_{CCO} = 1.71 \text{ V}$ to 2.625 V ; $GND = 0 \text{ V}$ $T_A = -40^\circ\text{C}$ to 85°C (Note 1))

Symbol	Characteristic	Min	Typ	Max	Unit
f_{DATA}	Maximum Operating Input Data Rate	10			Gbps
f_{MAX}	Maximum Input Clock Frequency $V_{CC} = 2.5\text{V}$ $V_{CC} = 1.8\text{V}$	7.5 6.5			GHz
V_{OUTPP}	Output Voltage Amplitude EQEN = 0 or 1 $f_{in} \leq 5.0 \text{ GHz}$ $V_{CC} = 2.5\text{V}$ $f_{in} \leq 7.5 \text{ GHz}$ $V_{CC} = 2.5\text{V}$ (See Figures 4, Note 2) $f_{in} \leq 5 \text{ GHz}$ $V_{CC} = 1.8\text{V}$ $f_{in} \leq 6.5 \text{ GHz}$ $V_{CC} = 1.8\text{V}$	275 225 225 200	440 360 360 315		mV
V_{CMR}	Input Common Mode Range (Differential Configuration, Note 3) (Figure 8)	1050		$V_{CC} - 50$	mV
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential, IN/IN to Qn/Qn	170	225	315	ps
$t_{PLH} \text{ TC}$	Propagation Delay Temperature Coefficient -40°C to $+85^\circ\text{C}$		30		fs/ $^\circ\text{C}$
t_{DC}	Output Clock Duty Cycle	48	50	52	%
t_{SKEW}	Duty Cycle Skew (Note 4) Within Device Skew (Note 5) Device to Device Skew (Note 6)		0.15 10 20	1 25 40	ps
t_{JITTER}	Random Clock Jitter RJ(RMS), 1000 cycles (Note 7) EQEN = 1 $f_{in} \leq 5.0 \text{ GHz}$ $5 \text{ GHz} \leq f_{in} \leq 7.5 \text{ GHz}$ Deterministic Jitter (DJ) (Note 8) EQEN = 1, FR4 = 12", $\leq 10 \text{ Gbps}$ $V_{CC} = 2.5 \text{ V}$ $V_{CC} = 1.8 \text{ V}$		0.2 0.2 3 3	0.7 1.2 40 20	ps
V_{INPP}	Input Voltage Swing (Differential Configuration) (Note 9) (Figure 6)	100		1200	mV
t_r , t_f	Output Rise/Fall Times Qn/Qn, (20%–80%)		30	65	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Measured using a 400 mV source, 50% duty cycle 1GHz clock source. All outputs must be loaded with external 50Ω to V_{CCO} . Input edge rates 40 ps (20% – 80%).
2. Output voltage swing is a single ended measurement operating in differential mode.
3. V_{CMR} min varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{CC} . The V_{CMR} range is referenced to the most positive side of the differential input signal.
4. Duty cycle skew is measured between differential outputs using the deviations of the sum of T_{pw-} and T_{pw+} @ 5 GHz.
5. Within device skew compares coincident edges.
6. Device to device skew is measured between outputs under identical transition
7. Additive CLOCK jitter with 50% duty cycle clock signal.
8. Additive Peak-to-Peak jitter with input NRZ data at PRBS23.
9. Input voltage swing is a single-ended measurement operating in differential mode, with minimum propagation change of 25 ps.

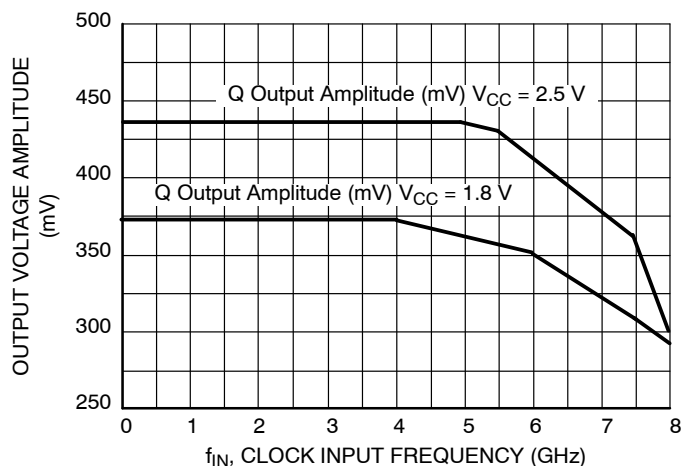


Figure 3. Output Voltage Amplitude (V_{OUTPP}) vs. Input Frequency (f_{in}) at Ambient Temperature (Typ), (EQEN = 0)

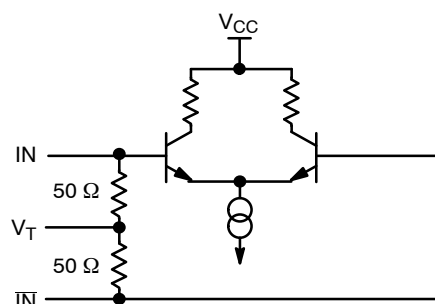


Figure 4. Input Structure

NB7VQ1006M

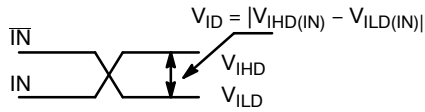


Figure 5. Differential Inputs Driven Differentially

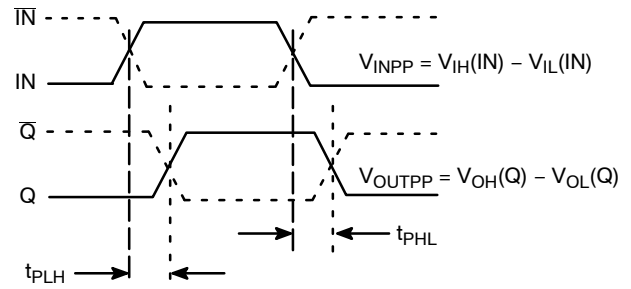


Figure 6. AC Reference Measurement

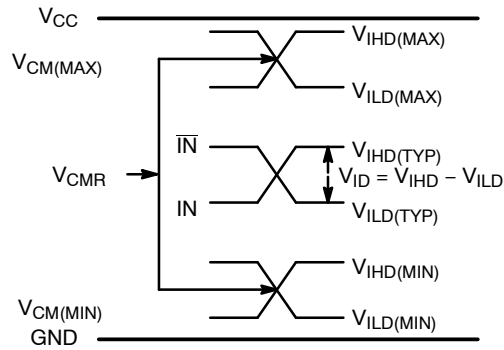


Figure 7. V_{CM} Diagram

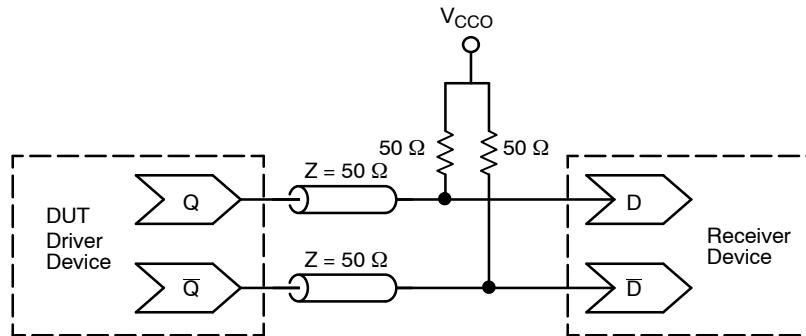


Figure 8. Typical Termination for CML Output Driver and Device Evaluation

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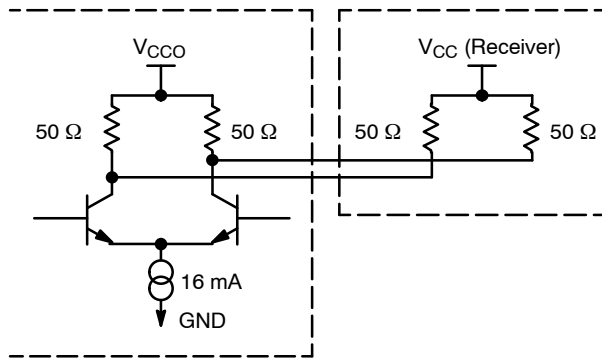


Figure 9. Typical CML Output Structure and Termination

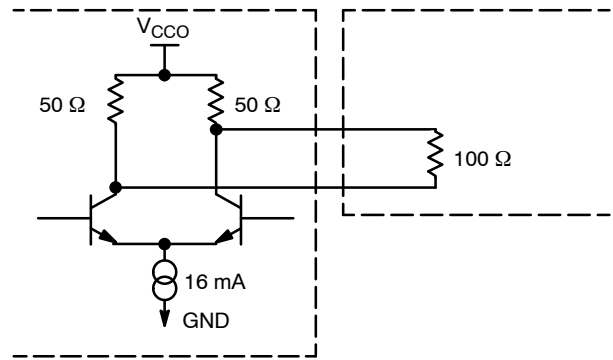


Figure 10. Alternative Output Termination

APPLICATION INFORMATION

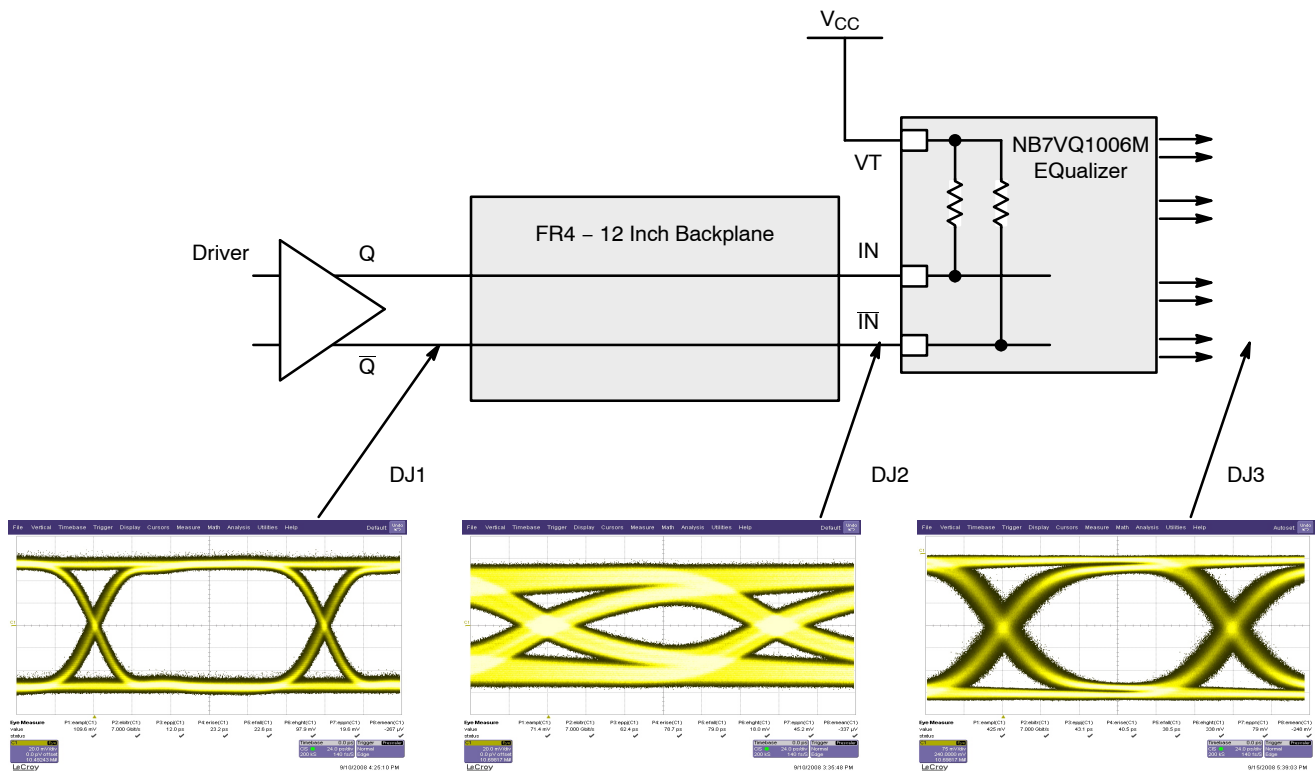


Figure 11. Typical NB7VQ1006 Equalizer Application and Interconnect with PRBS23 pattern at 7.0 Gbps

NB7VQ1006M

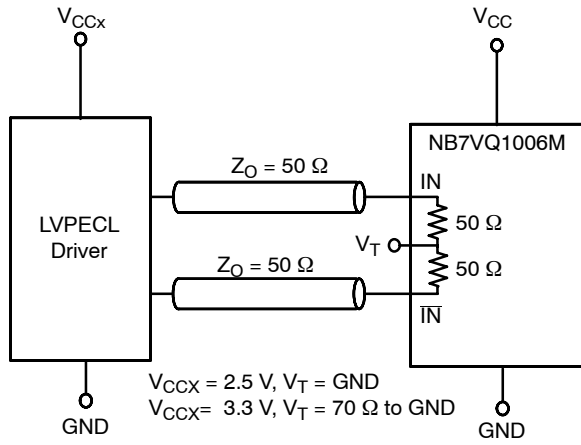


Figure 12. LVPECL Interface

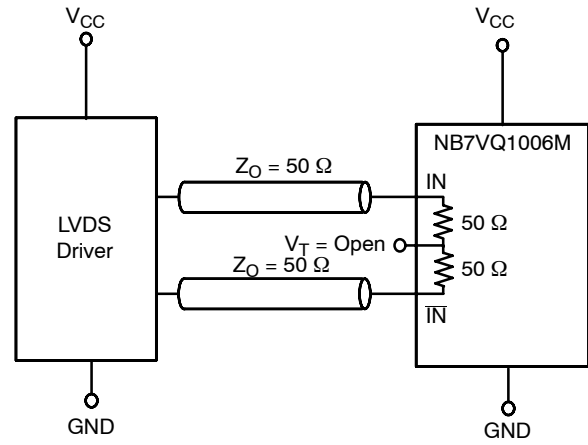


Figure 13. LVDS Interface

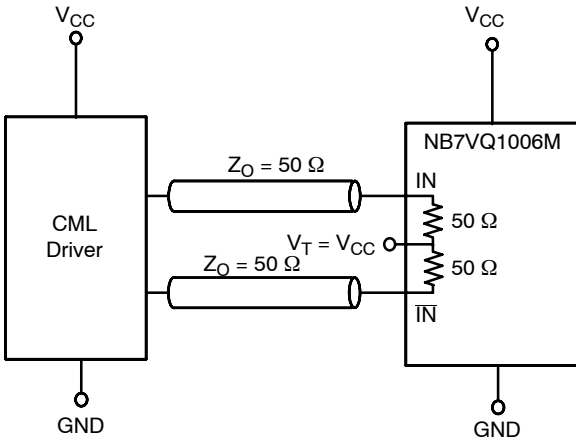
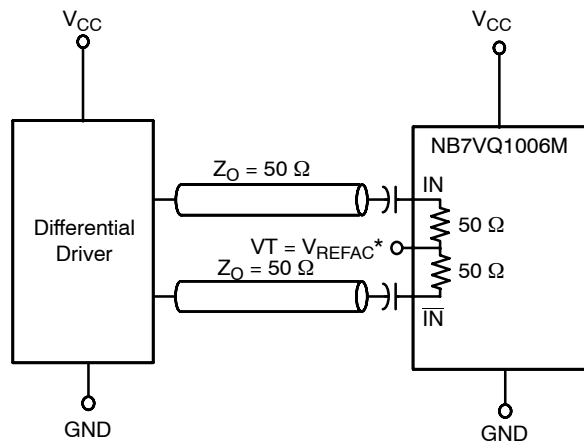


Figure 14. Standard 50 Ω Load CML Interface



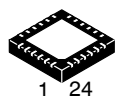
**Figure 15. Capacitor-Coupled
Differential Interface
(VT Connected to External V_{REFAC})**

*V_{REFAC} bypassed to ground with a 0.01 μF capacitor

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

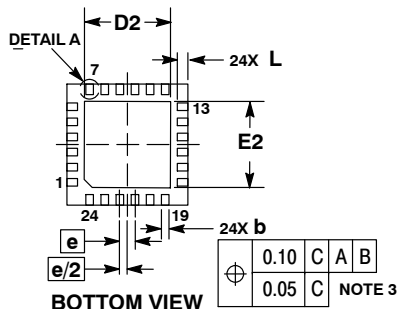
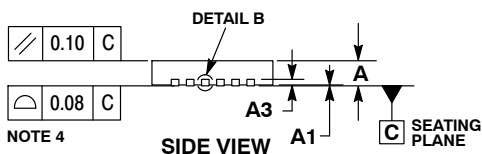
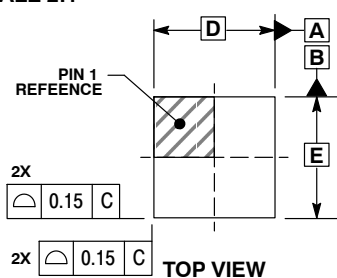
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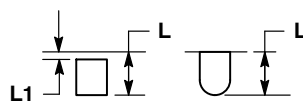
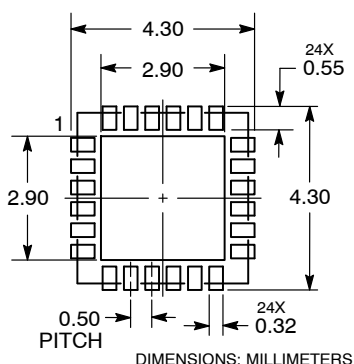
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QFN24, 4x4, 0.5P
CASE 485L
ISSUE B

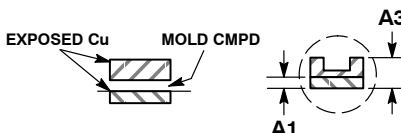
DATE 05 JUN 2012



RECOMMENDED SOLDERING FOOTPRINT



DETAIL A
ALTERNATE
CONSTRUCTIONS



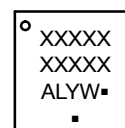
DETAIL B
ALTERNATE TERMINAL
CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.20	0.30
D	4.00	BSC
D2	2.70	2.90
E	4.00	BSC
E2	2.70	2.90
e	0.50	BSC
L	0.30	0.50
L1	0.05	0.15

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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DESCRIPTION:	QFN24, 4X4, 0.5P	PAGE 1 OF 1

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