NCN4557

1.8 V/3.0 V Dual SIM/SAM/ Smart Card Power Supply and Level Shifter

The NCN4557 is a dual interface analog circuit designed to translate the voltages between SIM, SAM or Smart Cards and a microcontroller (or similar control device). It integrates two LDOs for power conversion and three level shifters per channel allowing the management of two independent chip cards. The device fulfills the ISO7816 and EMV smart card interface requirements as well as the GSM and 3G mobile standard. Due to a built−in sequencer, the device enables automatic activation and deactivation. Through the ENABLE pin a low current shutdown mode can be activated extending the battery life.

The card power supply voltage (1.8 V or 3.0 V) and the card socket A or B are selected using two dedicated pins (SEL0 & SEL1).

Features

- Supports 1.8 V or 3.0 V Operating SIM/SAM/Smart Cards
- The LDOs are able to Supply more than 50 mA Under 1.8 V and 3.0 V
- Built−in Active and Passive Pullup Resistor for I/O and CRD_IOA/B Pins in Both Directions
- All Pins are Fully ESD Protected According to ISO−7816 Specifications – ESD Protection on Card Pins in Excess of 8.0 kV (JEDEC HBM)
- Built−in Sequencer for Activation and Deactivation
- Supports up to more than 5.0 MHz Clock
- Very Compact Low−Profile 3x3 QFN−16 Package
- These are Pb−Free Devices*

Applications

- SIM Card Interface Circuit for 2G, 2.5G and 3G Mobile Phones
- Wireless PC/Laptop Cards (PCMCIA Cards)
- POS Terminals (SAM Card Interfaces)
- Smart Card Readers

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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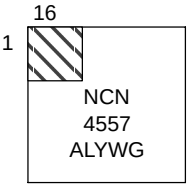
MARKING DIAGRAM

QFN16
MT SUFFIX
CASE 488AK



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

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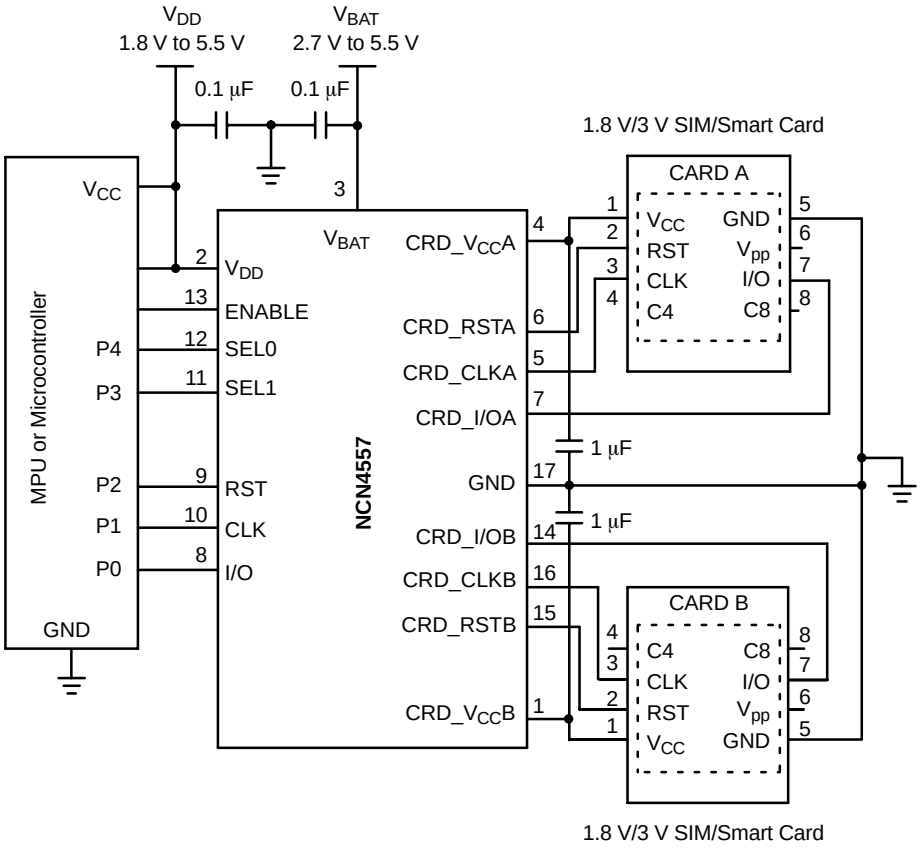


Figure 1. Typical Interface Application

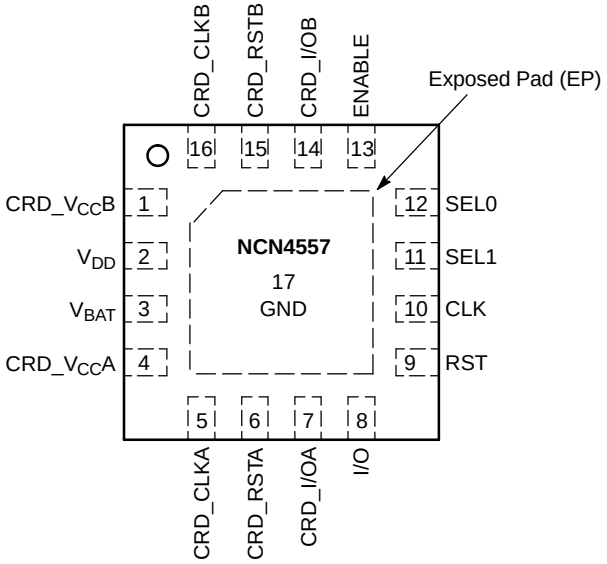


Figure 2. QFN−16 Pinout (Top View)

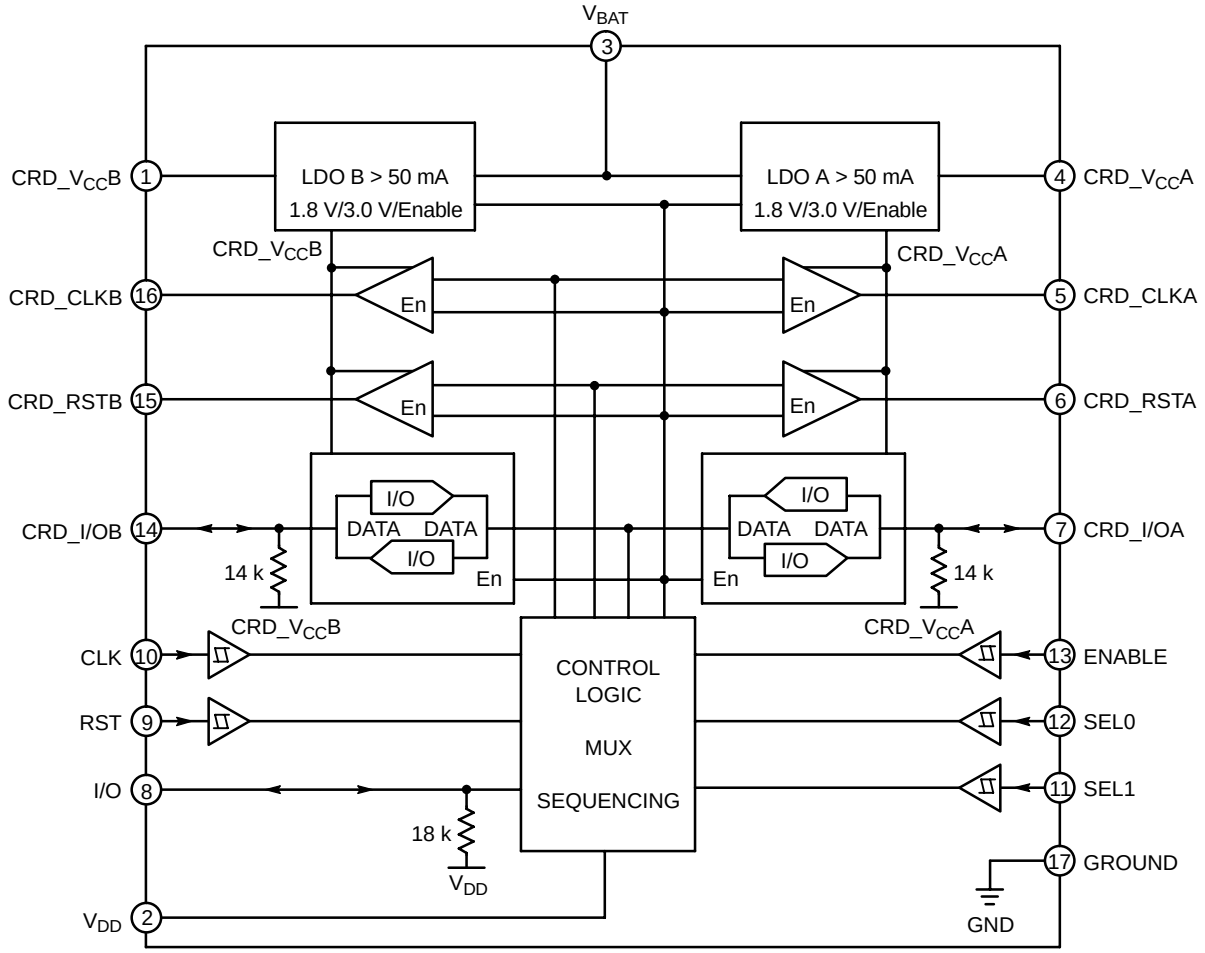


Figure 3. NCN4557 Block Diagram

PIN DESCRIPTIONS

PIN	Name	Type	Description
1	CRD_V_{CC}B	POWER	This pin is connected to the Card power supply pin (C1) (Card B).The corresponding LDO is programmable using the pins SEL0, SEL1 and ENABLE to provide 1.8 V, 3.0 V or 0 V (disable). CRD_V_{CC}B can not be active when CRD_V_{CC}A is active and conversely.
2	V_{DD}	POWER	This pin is connected to the controller power supply. It configures the level shifter input stage to accept the signal coming from the microcontroller. A 0.1 μF capacitor shall be used to bypass the power supply voltage. When V_{DD} is below 1.5 V typical CRD_V_{CC}A and B are disabled; the NCN4557 comes into a shutdown mode.
3	V_{BAT}	POWER	DC/DC converter power supply input shared by the LDOs A & B. This pin has to be bypassed by a 0.1 μF capacitor.
4	CRD_V_{CC}A	POWER	This pin is connected to the Card power supply pin (C1) (Card A).The corresponding LDO is programmable using the pins SEL0, SEL1 and ENABLE to provide 1.8 V, 3.0 V or 0 V (disable). CRD_V_{CC}A can not be active when CRD_V_{CC}B is active and conversely.
5	CRD_CLKA	OUTPUT	This pin is connected to the clock pin (C3) of the card connector A. The clock (CLK) signal comes from the external clock generator (standalone clock source or microcontroller). The internal level shifter adapts the voltage levels CLK to CRD_CLKA. An internal active pull− down NMOS device maintains this pin to Ground during either the CRD_V_{CC}A start−up sequence, or when CRD_V_{CC}A = 0 V.
6	CRD_RSTA	OUTPUT	This pin is connected to the RESET pin (C2) of the card connector A. A level translator adapts the RESET signal from the microcontroller to the external card A. The output current is internally limited to 15 mA max. Similarly to the CRD_CLK A or B pins this pin is maintained Low when CRD_V_{CC}A = 0 V and during the corresponding LDO transient phase of power−up.
7	CRD_I/OA	INPUT / OUTPUT	This pin handles the connection to the serial I/O pin (C7) of the card connector A. A bidirectional level translator adapts the serial I/O signal between the card and the micro−controller. A 14 kΩ (typical) pull−up resistor provides a High Impedance state to the card I/O link; during the operating phase, a dynamic pull−up circuit is activated making the CRD_I/OA rise time compliant with the ISO7816, EMV, GSM and related standards. An internal active pull−down MOS device forces this pin to Ground during either the CRD_V_{CC}A start−up sequence or when CRD_V_{CC}A = 0 V. The CRD_I/OA pin is internally limited by a 15 mA max current.
8	I/O	INPUT / OUTPUT	This pin is connected to an external microcontroller or cellular phone management unit (Baseband circuit or PMU). A bidirectional level translator adapts the serial I/O signal between the smart card A or B and the controller. Only one card, the selected card, communicates through the bidirectional I/O interface. A built−in 18 kΩ typical resistor provides a high impedance state when the interface is not activated. An additional dynamic pullup circuit accelerates the I/O rise time making the bidirectional channel perfectly balanced in regards to the standard rise time requirements.
9	RST	INPUT	The RESET signal present at this pin is connected to the card through the internal level shifter which translates the levels according to the CRD_V_{CC}A or B programmed value.
10	CLK	INPUT	The clock signal, coming from the external controller, must have a Duty Cycle within the Min/Max values defined by the specification (typically 50%). The built−in level shifter translates the input signal to the external card CLK input.
11	SEL1	INPUT	SEL1 allows the selection of the Card A or B (Table 1). SEL1 = Low → Card A selected SEL1 = High → Card B selected
12	SEL0	INPUT	SEL0 allows programming CRD_V_{CC}A or B (1.8 V or 3.0 V) (Table 1). SEL0 = Low → CRD_V_{CC}A/B = 1.8 V SEL0 = High → CRD_V_{CC}A/B = 3.0 V
13	ENABLE	INPUT	Power Up and Down pin: ENABLE = Low → Low current shutdown mode activated ENABLE = High → Normal Operation A Low level on this pin switches off the card interface.
14	CRD_I/OB	INPUT / OUTPUT	This pin handles the connection to the serial I/O pin (C7) of the card connector B. A bidirectional level translator adapts the serial I/O signal between the card and the micro−controller. A 14 kΩ (typical) pull−up resistor provides a High Impedance state to the card I/O link; during the operating phase a dynamic pull−up circuit is activated making the CRD_I/OB rise time compliant with the ISO7816, EMV, GSM and related standards. An internal active pulldown MOS device forces this pin to Ground during either the CRD_V_{CC}B start−up sequence or when CRD_V_{CC}B = 0 V. The CRD_I/OB pin is internally limited by a 15 mA maximum current.
15	CRD_RSTB	OUTPUT	This pin is connected to the RESET pin of the card connector B. A level translator adapts the RESET signal from the microcontroller to the external card B. The output current is internally limited by a 15 mA max current. Similarly to the CRD_CLK A or B pins this pin is maintained Low when CRD_V_{CC}B = 0 V and during the corresponding LDO transient phase of powerup.
16	CRD_CLKB	OUTPUT	This pin is connected to the clock pin (C3) of the card connector B. The clock (CLK) signal comes from the external clock generator (standalone clock source or microcontroller). The internal level shifter adapts the voltage levels CLK to CRD_CLKB. An internal active pull down NMOS device maintains this pin to Ground during either the CRD_V_{CC}B start−up sequence, or when CRD_V_{CC}B = 0 V.
17	GND	GND	This pin number is the Exposed Pad which is the electrical Ground of the device. It must be soldered to the PCB ground plane.

ATTRIBUTES

Characteristics		Values
ESD protection Human Body Model (HBM): Card Pins (1, 4, 5, 6, 7, 14, 15 , 16 & 17) (Note 1) All Other Pins (Note 1) Machine Model (MM): Card Pins (1, 4, 5, 6, 7, 14, 15 , 16 & 17) All Other Pins Charged Device Model (CDM): Card Pins (1, 4, 5, 6, 7, 14, 15 , 16 & 17) All Other Pins		 8 kV 2 kV 600 V 200 V 2 kV 400 V
Moisture sensitivity (Note 2)	QFN−16	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. Human Body Model (HBM): R =1500 Ω, C = 100 pF.
2. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
LDO Power Supply Voltage	V_{BAT}	$-0.5 \le V_{BAT} \le 6$	V
Power Supply Microcontroller Side	V_{DD}	$-0.5 \le V_{DD} \le 6$	V
External Card Power Supply	CRD_V_{CC}	$-0.5 \le$ CRD_$V_{CC} \le 6$	V
Digital Input Pins	V_{in} I_{in}	$-0.5 \le V_{in} \le V_{DD} + 0.5$ but < 6.0 ±5	V mA
Digital Output Pins	V_{out} I_{out}	$-0.5 \le V_{out} \le V_{DD} + 0.5$ but < 6.0 ± 10	V mA
CRD Output Pins CRD_I/O & CRD_RST Pins CRD_CLK Pin	V_{out} I_{out}	$-0.5 \le V_{out} \le$ CRD_V_{CC} + 0.5 but < 6.0 15 (Internally Limited) 70 (Internally Limited)	V mA
QFN−16 Low Profile package Power Dissipation @ T_A = +85°C Thermal Resistance Junction−to−Air	 P_D $R_{\theta JA}$	 450 90	 mW °C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range	T_J	−40 to +125	°C
Maximum Junction Temperature	T_{Jmax}	+125	°C
Storage Temperature Range	T_{stg}	−65 to + 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

POWER SUPPLY SECTION (−40°C to +85°C)

Pin	Symbol	Rating	Min	Typ	Max	Unit
3	V_{BAT}	Power Supply	2.7		5.5	V
3	I_{VBAT}	Operating current CRD_V_{CC}A = 3.0 V, CRD_V_{CC}B = 0 V, I_{CC}A & B = 0 mA CRD_V_{CC}A = 1.8 V, CRD_V_{CC}B = 0 V, I_{CC}A & B = 0 mA CRD_V_{CC}A = 0 V, CRD_V_{CC}B = 3.0 V, I_{CC}A & B = 0 mA CRD_V_{CC}A = 0 V, CRD_V_{CC}B = 1.8 V, I_{CC}A & B = 0 mA		 26 25 26 25	 80 80 80 80	μA
3	I_{VBAT_SD}	Shutdown current – ENABLE = Low			3	μA
2	V_{DD}	Operating Voltage	1.8		5.5	V
2	I_{VDD}	Operating Current (CLK & RST Low)		0.1	2	μA
2	I_{VDD_SD}	Shutdown Current – ENABLE = Low		0.05	1	μA
2	V_{DD}	Undervoltage Lockout	0.6		1.5	V
1,4	CRD_V_{CC}A or B	3.0 V Mode, V_{BAT} = 3.3 V to 5.5 V, I_{CRD_VCC} = 0 mA to 50 mA 1.8 V Mode, V_{BAT} = 2.7 V to 5.5 V, I_{CRD_VCC} = 0 mA to 50 mA	2.75 1.65	3.0 1.8	3.25 1.95	V
1,4	$I_{CRD_VCC_SC}$	Short –Circuit Current – CRD_V_{CC} Shorted to GND, T_A = 25°C		50	175	mA
7,13,14		Channel Turn−on Time I_{CC}A or B = 0 mA, ENABLE rise edge to CRD_I/OA or B rise edge		 0.8	 2.5	ms

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

DIGITAL INPUT/OUTPUT SECTION CLK, RST, I/O, ENABLE, SEL0, SEL1 (−40°C to + 85°C)

Pin	Symbol	Rating	Min	Typ	Max	Unit
9,10	V_{IH} V_{IL}	High Level Input Voltage (RST, CLK) Low Level Input Voltage (RST, CLK)	0.85 * V_{DD}		V_{DD} 0.15 * V_{DD}	V
11,12,13	V_{IH} V_{IL}	High Level Input Voltage (ENABLE, SEL0, SEL1) Low Level Input Voltage (ENABLE, SEL0, SEL1)	0.85 * V_{DD}		V_{DD} 0.15 * V_{DD}	V
9,10,11, 12,13	I_{IH}, I_{IL}	Input current (RST, CLK, ENABLE, SEL0, SEL1)	−1		1	μA
8	$V_{OH_I/O}$ $V_{OL_I/O}$	High Level Output Voltage (CRD_ I/O = CRD_V_{CC}, $I_{OH_I/O}$=−20 μA) Low Level Output Voltage (CRD_ I/O = 0 V, $I_{OL_I/O}$ = 500 μA)	0.75 * V_{DD}		V_{DD} 0.3	V
8	t_R, t_F	Rise and Fall times (I/O), C_{out} = 30 pF			0.8	μs
8	$R_{pu_I/O}$	I/0 Pullup Resistor	12	18	24	kΩ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

CARD INTERFACE SECTION (−40°C to +85°C)

Pin	Symbol	Rating	Min	Typ	Max	Unit
6,15	CRD_RSTA CRD_RSTB	CRD_V_{CC} = +3 V				
		Output RESET V_{OH} @ ICRD_rst = −20 μA	0.9 * CRD_V_{CC}		CRD_V_{CC}	V
		Output RESET V_{OL} @ ICRD_rst = +200 μA	0		0.3	V
		Output RESET Rise Time @ C_{out} = 30 pF			0.8	μs
		Output RESET Fall Time @ C_{out} = 30 pF			0.8	μs
		CRD_V_{CC} = +1.8 V				V
		Output RESET V_{OH} @ ICRD_rst = −20 μA	0.9 * CRD_V_{CC}		CRD_V_{CC}	V
		Output RESET V_{OL} @ ICRD_rst = +200 μA	0		0.3	μs
		Output RESET Rise Time @ C_{out} = 30 pF			0.8	μs
		Output RESET Fall Time @ C_{out} = 30 pF			0.8	
5,16	CRD_CLKA CRD_CLKB	CRD_V_{CC} = +3 V				
		Output Duty Cycle	40		60	%
		Max Output Frequency	5			MHz
		Output V_{OH} @ ICRD_clk = −20 μA	0.9 * CRD_V_{CC}		CRD_V_{CC}	V
		Output V_{OL} @ ICRD_clk = +200 μA	0		0.3	V
		Output CRD_CLK Rise Time @ C_{out} = 30 pF			18	ns
		Output CRD_CLK Fall Time @ C_{out} = 30 pF			18	ns
		CRD_V_{CC} = +1.8 V				
		Output Duty Cycle	40		60	%
		Max Output Frequency	5			MHz
		Output V_{OH} @ ICRD_clk = −20 μA	0.9 * CRD_V_{CC}		CRD_V_{CC}	V
		Output V_{OL} @ ICRD_clk = +200 μA	0		0.3	V
		Output CRD_CLK Rise Time @ C_{out} = 30 pF			18	ns
		Output CRD_CLK Fall Time @ C_{out} = 30 pF			18	ns
7,14	CRD_I/OA CRD_I/OB	CRD_V_{CC} = +3 V				
		Output V_{OH} @ I_{CRD_IO} = −20 μA, $V_{I/O}$ = V_{DD}	0.8 * CRD_V_{CC}		CRD_V_{CC}	V
		Output V_{OL} @ I_{CRD_IO} = +1 mA, $V_{I/O}$ = 0V	0		0.4	V
		CRD_I/O Rise Time @ C_{out} = 30pF			0.8	μs
		CRD_I/O Fall Time @ C_{out} = 30 pF			0.8	μs
		CRD_V_{CC} = +1.8 V				
		Output V_{OH} @ I_{CRD_IO} = −20 μA, $V_{I/O}$ = V_{DD}	0.8 * CRD_V_{CC}		CRD_V_{CC}	V
		Output V_{OL} @ I_{CRD_IO} = +1 mA, $V_{I/O}$ = 0 V	0		0.3	V
		CRD_I/O Rise Time @ C_{out} = 30 pF			0.8	μs
		CRD_I/O Fall Time @ C_{out} = 30 pF			0.8	μs
		Short−Circuit Current, $V_{I/O}$ = 0 V		4	15	mA
8	$R_{pu_CRD_I/O}$	Card I/O Pullup Resistor	10	14	18	kΩ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. All the dynamic specifications (AC specifications) are guaranteed by design over the operating temperature range.

TYPICAL CHARACTERISTICS

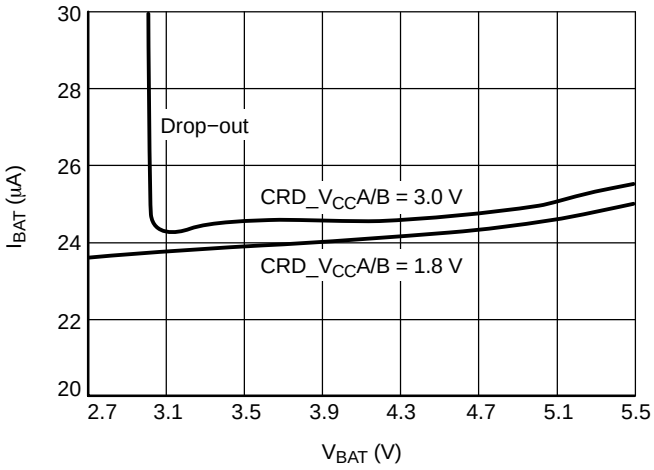


Figure 4. I_{BAT} Operating Current vs. V_{BAT}, T_A = 25°C, I_{CC} = 0 mA

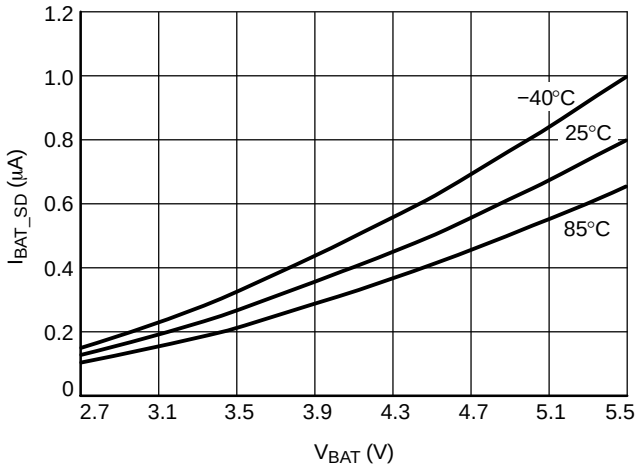


Figure 5. I_{BAT} Shutdown Current vs. V_{BAT}

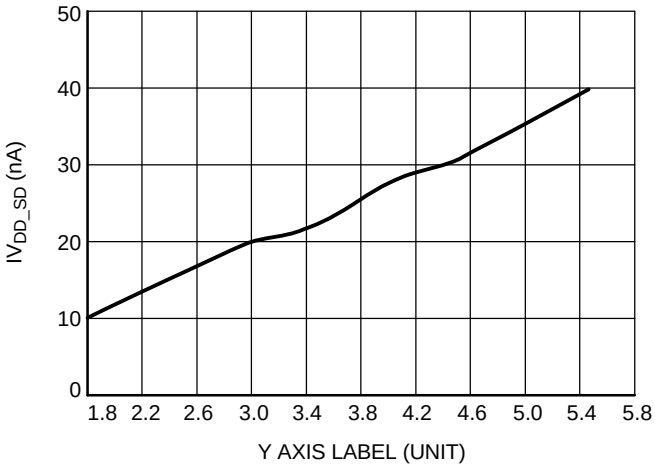


Figure 6. IV_{DD} Shutdown Current vs. V_{DD}, T_A = 25°C, V_{BAT} = 5.5 V

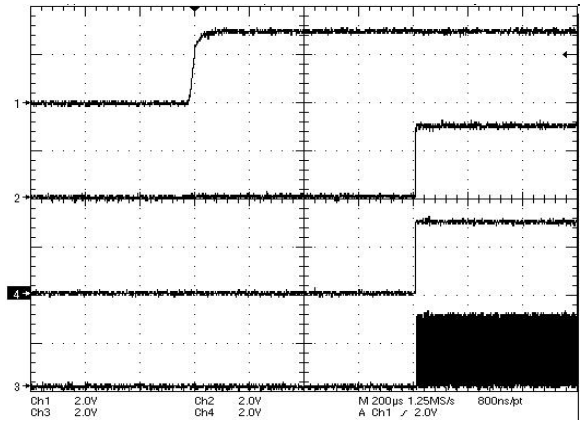


Figure 7. Activation Sequence, Ch1 : CRD_V_{CC}, Ch2 : CRD_IO, Ch4 : CRD_RST, Ch3 : CRD_CLK

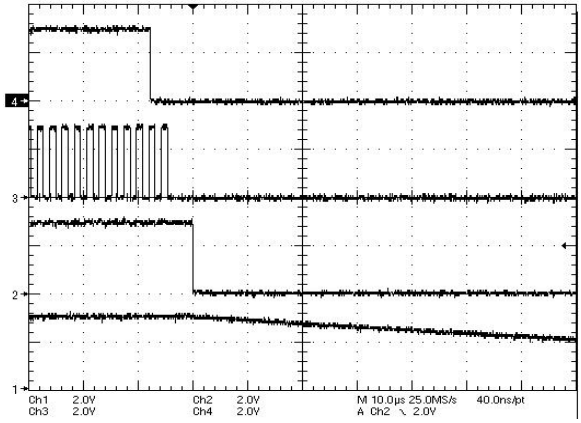


Figure 8. Automatic Deactivation Ch4: CRD_RST, Ch3: CRD_CLK, Ch2: CRD_IO, Ch1: CRD_V_{CC}

APPLICATION INFORMATION

The NCN4557 is a dual LDO−based DC/DC converter and level shifter able to handle independently 2 smart card interfaces. When one of these interfaces is operating the other one is not active and conversely. Class B (3.0 V) and C (1.8 V) cards can be used.

The Card and the CRD_V_{CC} power supply are selected using the pins SEL0, SEL1 and ENABLE according to Table 1.

Table 1. CARD AND CRD_V_{CC} SELECTION

ENABLE	SEL1	SEL0	Card# / CRD_V_{CC}
1	0	0	Card A / 1.8 V
1	0	1	Card A / 3.0 V
1	1	0	Card B / 1.8 V
1	1	1	Card B / 3.0 V
0	X	X	A & B Disabled

Card Supply Converter

The built−it NCN4557 DC/DC converters are Low Drop−Out Voltage Regulators capable to supply a current in excess of 50 mA under 1.8 V or 3.0 V. These voltages are selected according to Table 1. Using the Boolean input ENABLE pin the NCN4557 device can be disabled setting the circuit in a shutdown mode for which the power consumption features values typically in the range of a few tens of nA. Figure 9 shows a simplified view of the NCN4557 voltage regulator. The CRD_V_{CC} output is internally current limited and protected against short circuits. The short−circuit current IV_{CC} varies with V_{BAT} typically in the range of 30 mA to 60 mA.

In order to guarantee a stable and satisfying operating of the LDO the CRD_V_{CC} output will be connected to a 1.0 μF bypass ceramic capacitor to the ground. At the input, V_{BAT} will be bypassed to the ground with a 0.1 μF ceramic capacitor.

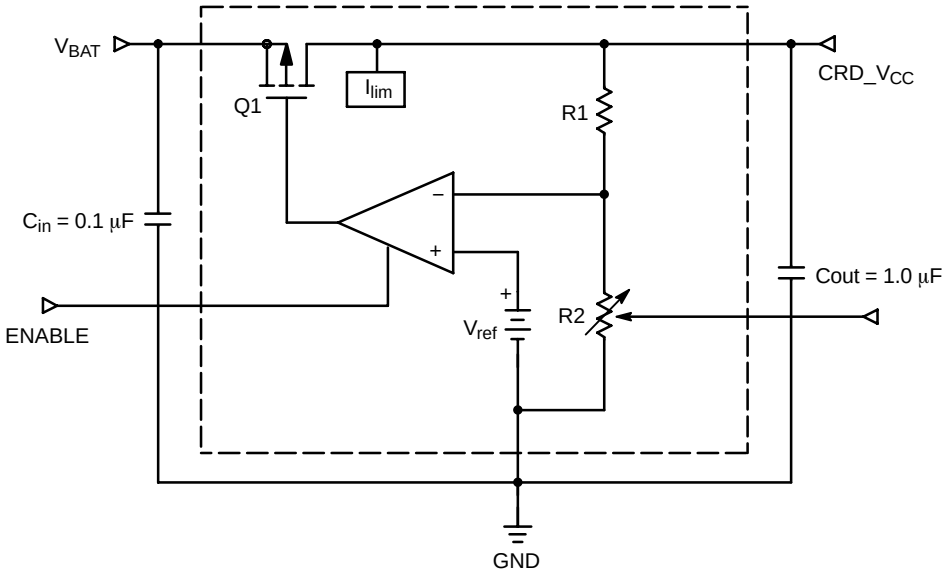


Figure 9. Simplified Block Diagram of the LDO Voltage Regulator

Level Shifters

The level shifters accommodate the voltage difference that might exist between the microcontroller and the smart card. The RESET and CLOCK level shifters are mono−directional and feature both the same architecture.

The bidirectional I/O line provides a way to automatically adapt the voltage difference between the controller and the card in both directions. In addition with the pull−up resistor, a dynamic pullup circuit (Figure 10, Q1 and Q2) provides a fast charge of the stray capacitance, yielding a rise time fully within the ISO7816, EMV and GSM specifications.

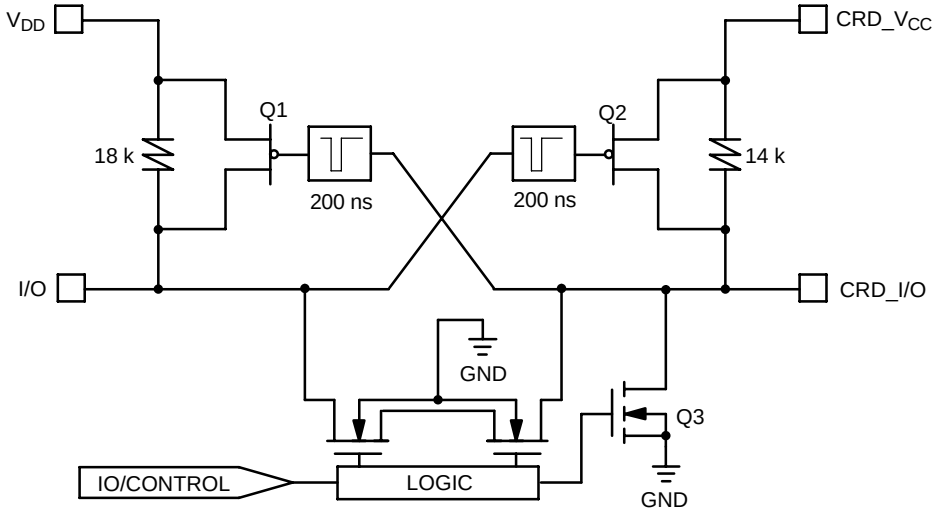


Figure 10. Basic I/O line Interface

The typical waveform provided in Figure 11 shows how the accelerator operates. During the first 200 ns (typical), the slope of the rise time is solely a function of the pullup resistor associated with the stray capacitance. During this period, the PMOS devices are not activated since the input voltage is below their V_{gs} threshold. When the input slope crosses the V_{gsth}, the opposite one shot is activated, providing a low impedance to charge the capacitance, thus increasing the rise time as depicted in Figure 11. The same mechanism applies for the opposite side of the line to make sure the system is optimum.

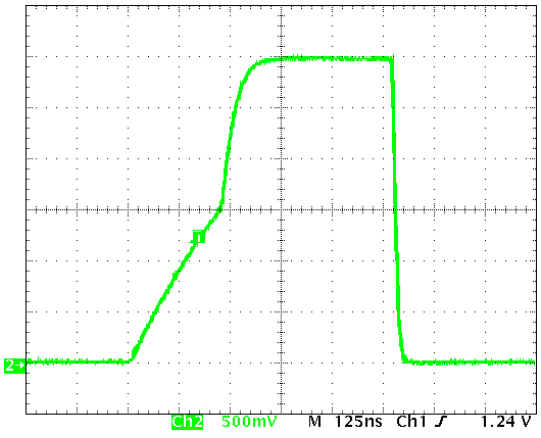


Figure 11. CRD_IO Typical Rise and Fall Times with Stray Capacitance > 30 pF
(33 pF capacitor connected on the board)

Powerup Sequence

The powerup sequence makes sure all the card−related signals are LOW during the CRD_V_{CC} positive going slope. The Powerup sequence is activated by setting the ENABLE Boolean signal HIGH. CRD_RST, CRD_CLK and CRD_I/O are maintained LOW during the activation stage until CRD_V_{CC} reaches its nominal value (1.8 V or 3.0 V). Figure 7 shows the typical NCN4557 activation sequence.

About 800 μs after CRD_V_{CC} has reached its nominal voltage value, CRD_IO and CRD_RST are released.

CRD_CLK is enabled during the rising slope of the second clock cycle after CRD_IO and CRD_RST are enabled.

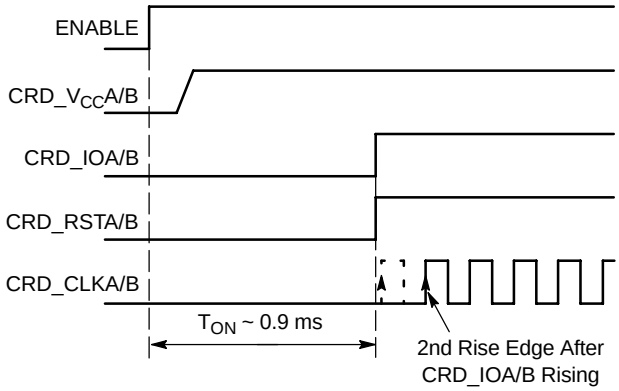


Figure 12. NCN4557 Power−Up

In all cases the application software is responsible for the smart card signal sequence (contact activation sequence, cold reset and warm reset sequences).

Powerdown Sequence

The NCN4557 provides a powerdown sequence which is activated by setting the ENABLE Boolean signal LOW. The communication I/O session is terminated immediately according to the ISO7816 and EMV specifications as depicted in Figures 8 and 13.

ISO7816 Sequence:

- CRD_RST is forced to LOW
- CRD_CLK is forced to LOW 2 clock cycles after ENABLE is set LOW unless CRD_CLK is already in

this state or 8 μs after the ENABLE pin is set LOW in the other cases.

- CRD_I/O is forced to LOW about 8 μs after the ENABLE pin is set LOW.
- Then CRD_V_{CC} Supply Shuts Off

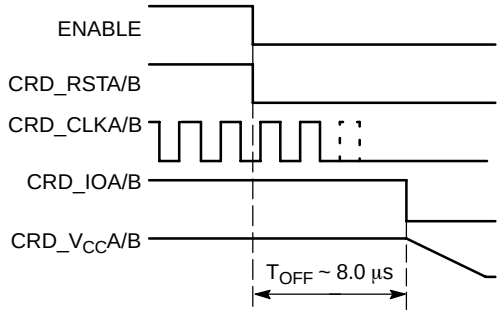


Figure 13. NCN4557 Power Down Sequence

Input Schmitt Triggers

All the logic input pins (excepted I/O and CRD_I/O, Figure 3) have built−in Schmitt trigger circuits to prevent the NCN4557 against uncontrolled operation. The typical dynamic characteristics of the related pins are depicted in Figure 14.

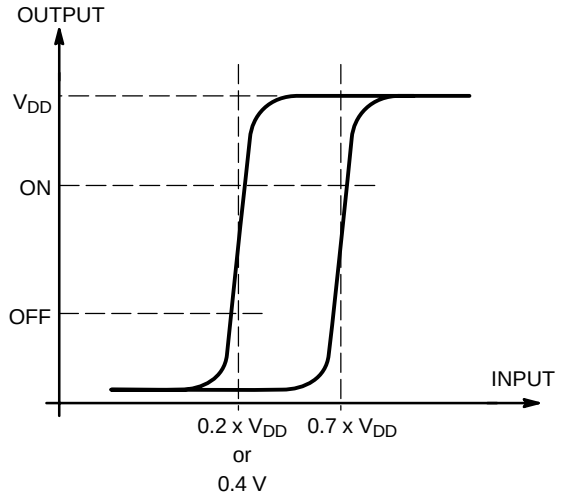


Figure 14. Typical Schmitt Trigger Characteristics

Shutdown Operating

In order to save power or for other purpose required by the application it is possible to put the NCN4557 in a shutdown mode by setting LOW the pin ENABLE. On the other hand the device enters automatically in a shutdown mode when V_{DD} becomes lower than 1.0 V typically.

ESD Protection

The NCN4557 CRD interface features an Human Body Model ESD voltage protection in excess of 8 kV for all the CRD pins (CRD_IOA & B, CRD_CLKA & B, CRD_RSTA & B, CRD_V_{CC}A & B and GND). All the other pins (microcontroller side) sustain at least 2 kV. These values are guaranteed for the device in its full integrity without considering the external capacitors added to the circuit for a proper operating. Consequently in the operating conditions it is able to sustain much more than 8 kV on its CRD pins making it perfectly protected against electrostatic discharge well over the Human Body Model ESD voltages required by the ISO7816 standard (4 kV).

Printed Circuit Board Layout

Careful layout routing will be applied to achieve a good and efficient operating of the device in its mobile or portable environment and fully exploit its performance.

The bypass capacitors have to be connected as close as possible to the device pins (CRD_V_{CC}A and B, V_{DD} or V_{BAT}) in order to reduce as much as possible parasitic behaviors (ripple and noise). It is recommended to use ceramic capacitors.

The exposed pad of the QFN−16 package will be connected to the ground. A relatively large ground plane is recommended.

ORDERING INFORMATION

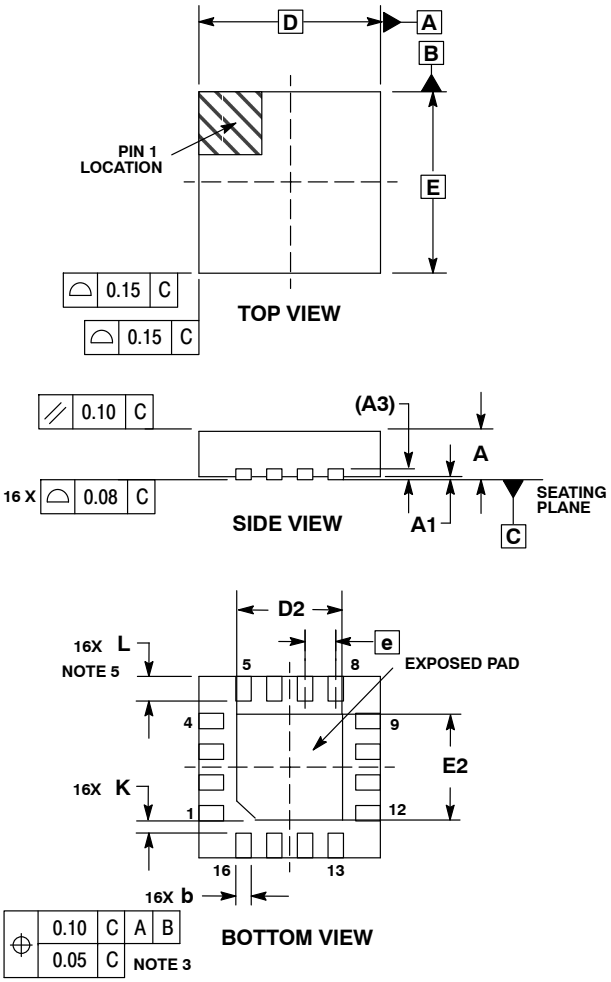
Device	Package	Shipping†
NCN4557MTG	QFN−16 (Pb−Free)	123 Units / Rail
NCN4557MTR2G	QFN−16 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

QFN16 3*3*0.75 MM, 0.5 P
CASE 488AK−01
ISSUE O

DATE 13 SEP 2004

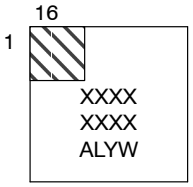
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM SPACING BETWEEN LEAD TIP AND FLAG.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.20	−−−
L	0.30	0.50

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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DESCRIPTION:	**QFN16, 3*3*0.75 MM, 0.5 PITCH**		**PAGE 1 OF 1**

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