NCN5193

HART Modem

Description

The NCN5193 is a single−chip, CMOS modem for use in highway addressable remote transducer (HART) field instruments and masters. The modem and a few external passive components provide all of the functions needed to satisfy HART physical layer requirements including modulation, demodulation, receive filtering, carrier detect, and transmit−signal shaping. In addition, the NCN5193 also has an integrated DAC for low-BOM current loop slave transmitter implementation.

The NCN5193 uses phase continuous frequency shift keying (FSK) at 1200 bits per second. To conserve power the receive circuits are disabled during transmit operations and vice versa. This provides the half−duplex operation used in HART communications.

Features

- Single−chip, Half−duplex 1200 Bits per Second FSK Modem
- Bell 202 Shift Frequencies of 1200 Hz and 2200 Hz
- 1.8 V − 3.5 V Power Supply
- Transmit−signal Wave Shaping
- Receive Band−pass Filter
- Low Power: Optimal for Intrinsically Safe Applications
- Compatible with 1.8 V or 3.3 V Microcontroller
- Internal Oscillator Requires 460.8 kHz, 920 kHz, 1.84 MHz or 3.68 MHz Crystal or Ceramic Resonator
- SPI Communication
- Integrated 17 bit Sigma-Delta DAC
- Meets HART Physical Layer Requirements
- Industrial Temperature Range of −40°C to +85°C
- Available in 32−pin NQFP Package
- These are Pb−Free Devices

Applications

- HART Multiplexers
- HART Modem Interfaces
- 4 − 20 mA Loop Powered Transmitters

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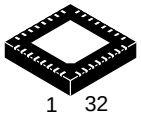
MARKING DIAGRAM



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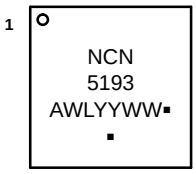

NCN5193 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

HART® COMMUNICATION PROTOCOL

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BLOCK DIAGRAM

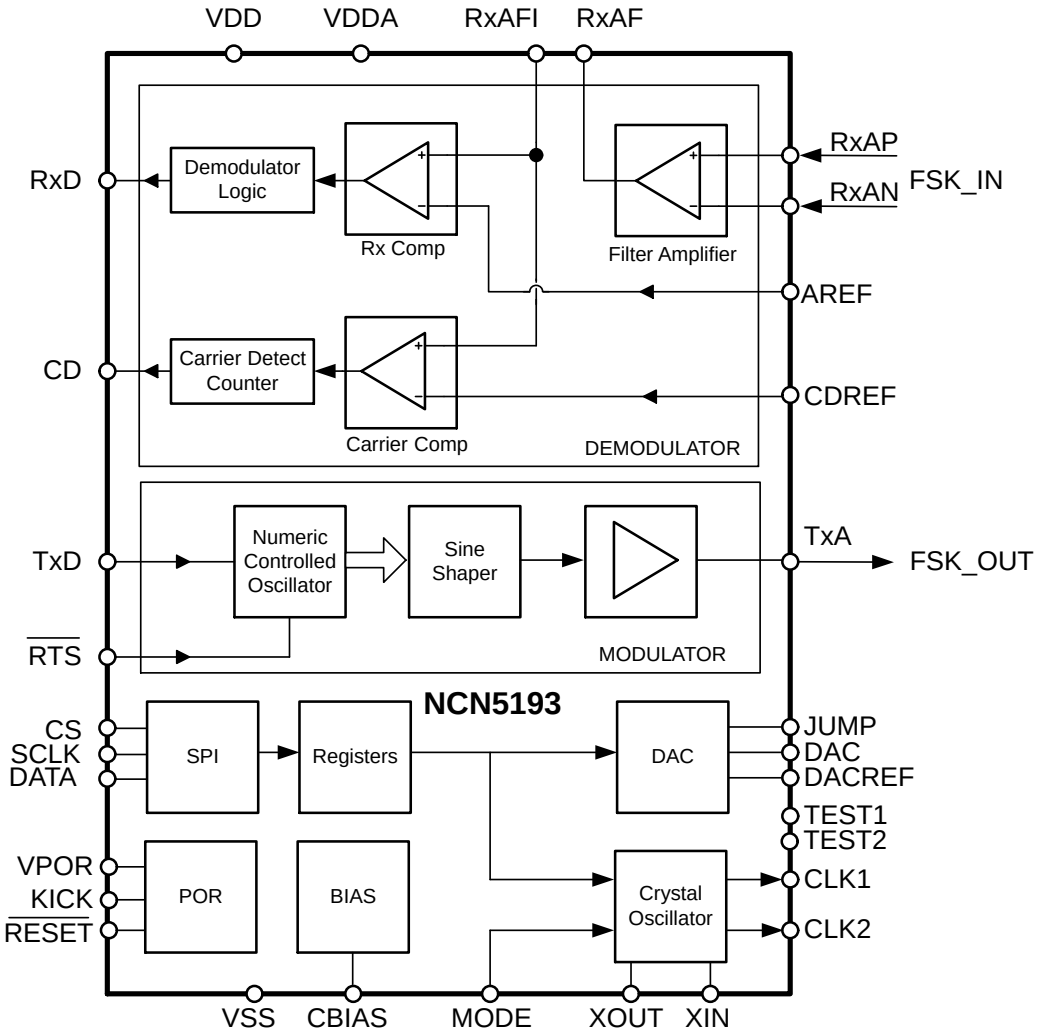


Figure 1. Block Diagram NCN5193

ELECTRICAL SPECIFICATIONS

Table 1. ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature	−40	+85	°C
T_S	Storage Temperature	−55	+150	°C
T_J	Junction Temperature	−40	+85	°C
V_{DD}	Supply Voltage	−0.3	4.0	V
V_{IN}, V_{OUT}	DC Input, Output	−0.3	V_{DD} + 0.3	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. CMOS devices are damaged by high−energy electrostatic discharge. Devices must be stored in conductive foam or with all pins shunted. Precautions should be taken to avoid application of voltages higher than the maximum rating. Stresses above absolute maximum ratings may result in damage to the device.

Table 2. DC CHARACTERISTICS (V_{DD} = 1.8 V to 3.5 V, V_{SS} = 0 V, T_A = −40°C to +85°C)

Symbol	Parameter	V_{DD}	Min	Typ	Max	Units
V_{DD}	DC Supply Voltage		1.8		3.5	V
V_{IL}	Input Voltage, Low	1.8 – 3.5 V			0.2 * V_{DD}	V
V_{IH}	Input Voltage, High	1.8 – 3.5 V	0.8 * V_{DD}			V
V_{OL}	Output Voltage, Low (I_{OL} = 0.67 mA)	1.8 – 3.5 V			0.4	V
V_{OH}	Output Voltage, High (I_{OH} = −0.67 mA)	1.8 – 3.5 V	V_{DD} − 0.4			V
I_{IL}/I_{IH}	Input Leakage Current				±1	μA
I_{DD}	Total Power Supply Current		70	190	500	μA
I_{DDA}	Static Analog Supply Current		45		270	μA
I_{DDQ}	Static Digital Current		0		30	μA
I_{DDD}	Dynamic Digital Current		25		200	μA
A_{REF}	Analog Reference		1.2	1.235	2.6	V
CD_{REF} (Note 2)	Carrier Detect Reference (A_{REF} – 0.08 V)			1.15		V
I_{BIAS}	Comparator Bias Current (R_{BIAS} = 120 kΩ, A_{REF} = 1.235 V)			2.5		μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. The HART specification requires carrier detect (CD) to be active between 80 and 120 mVp−p. Setting CD_{REF} at A_{REF} − 0.08 VDC will set the carrier detect to a nominal 100 mVp−p.

Table 3. AC CHARACTERISTICS (V_{DD} = 1.8 V to 3.5 V, V_{SS} = 0 V, T_A = −40°C to +85°C) (Note 3)

Pin Name	Description	Min	Typ	Max	Units
RxAP, RxAN	Receive analog input Leakage current Frequency – mark (logic 1) Frequency – space (logic 0)	 1190 2180	 1200 2200	 ±150 1210 2220	 nA Hz Hz
RxAF	Output of the high−pass filter Slew rate Gain bandwidth (GBW) Voltage range	 300 0.15	 0.04 	 V_{DD} – 0.15	 V/μs kHz V
RxAFI	Carrier detect and receive filter input Leakage current			 ±500	 nA
TxA	Modulator output Frequency – mark (logic 1) Frequency – space (logic 0) Amplitude (IAREF 1.235 V) Slew Rate − mark (logic 1) Slew Rate − space (logic 0) Loading (IAREF = 1.235 V)	 30	 1196.9 2194.3 500 1860 3300 	 	 Hz Hz mV V/s V/s kΩ
RxD	Receive digital output Rise/fall time			 20	ns
CD	Carrier detect output Rise/fall time			 20	ns

3. The modulator output frequencies are proportional to the input clock frequency (460.8 kHz/920 kHz/1.84 MHz / 3.68 MHz).

Table 4. MODEM CHARACTERISTICS (V_{DD} = 1.8 V to 3.5 V, V_{SS} = 0 V, T_A = −40°C to +85°C)

Parameter	Min	Typ	Max	Units
Demodulator jitter Conditions 1. Input frequencies at 1200 Hz ± 10 Hz, 2200 Hz ± 20 Hz 2. Clock frequency of 460.8 kHz ± 0.1% 3. Input (RxAP) asymmetry, 0			12	% of 1 bit

Table 5. CERAMIC RESONATOR AND CRYSTAL − External Clock Specifications
(V_{DD} = 1.8 V to 3.5 V, V_{SS} = 0 V, T_A = −40°C to +85°C)

Parameter	Min	Typ	Max	Units
460.8 kHz / 920 kHz / 1.84 MHz / 3.68 MHz Ceramic resonator or crystal oscillation frequency tolerance			1.0	%
External Clock Duty cycle Amplitude	35	50 $V_{OH} - V_{OL}$	65	% V

Table 6. DAC CHARACTERISTICS (V_{DD} = 3.0 V to 5.5 V, V_{SS} = 0 V, T_A = −40°C to +85°C)

Parameter	Min	Typ	Max	Units
Bandwidth (Note 4)		25		Hz
Resolution		17		Bit
Maximum Output Return−to−Zero		AVDD/2		V

4. The DAC is a sigma−delta type modulator. Therefore, the bandwidth is determined by the external filter. Decreasing the bandwidth will increase DAC accuracy.

TYPICAL APPLICATION

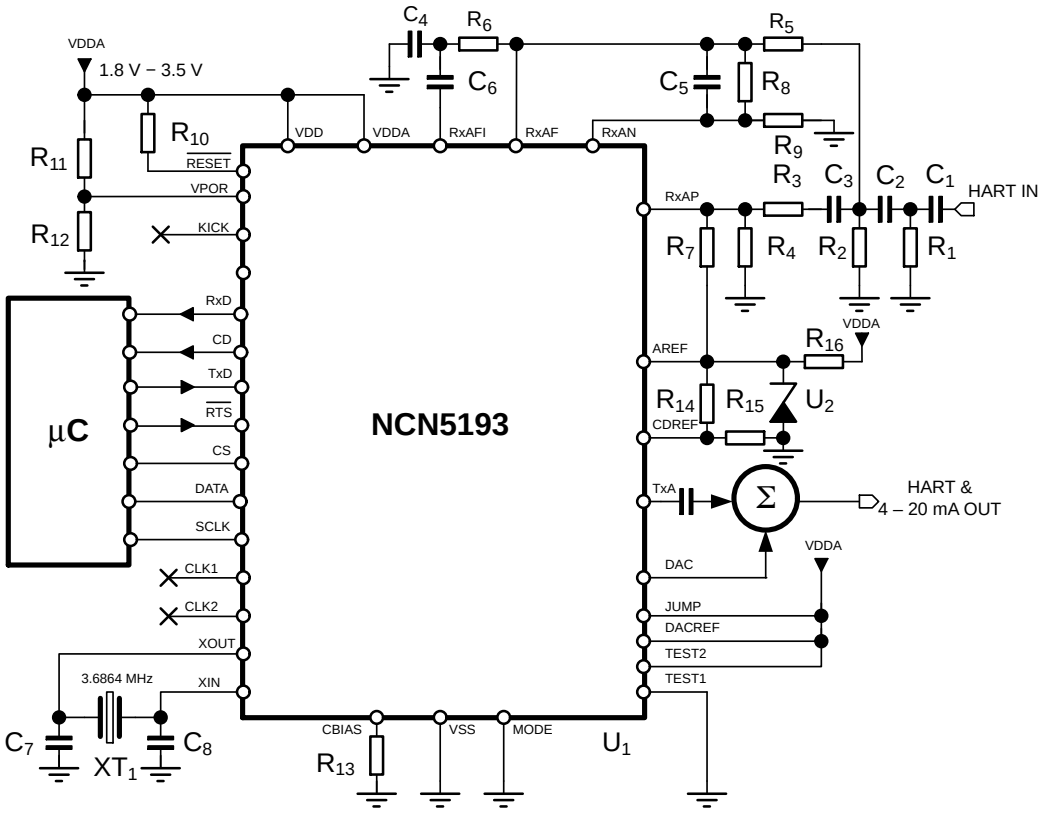


Figure 2. Application Diagram NCN5193

Table 7. TYPICAL BILL OF MATERIALS

Reference Designator	Value (Typical)	Tolerance	Manufacturer	Part Number
U1	–	–	ON Semiconductor	NCN5193
U2	–	–	ON Semiconductor	LM285
R1, R2	1.5M	1%		
R3, R5	806k	1%		
R4	1.3M	1%		
R6	174k	1%		
R7	2.2M	1%		
R8, R9	422k	1%		
R11	240k	1%		
R12, R15, R10	200k	1%		
R13	120k	1%		
R14, R16	14k7	1%		
C1	1 nF	5%		
C2	470 pF	5%		
C3	200 pF	5%		
C4	220 pF	5%		
C5	20 pF	5%		
C6	330 pF	5%		
C7, C8	18 pF	10%		
XT1	3.6864 MHz	100 ppm	Raltron	AS−3.6864−18

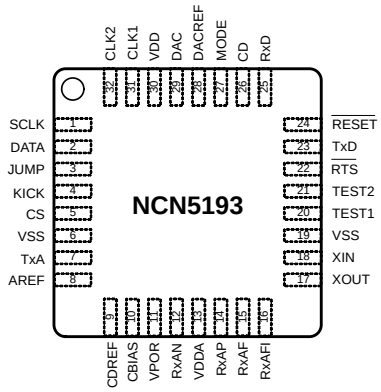


Figure 3. Pin Out NCN5193 in 32-pin NQFP (top view)

Table 8. PIN OUT SUMMARY 32−PIN NQFP

Pin No.	Signal Name	Type	Pin Description
1	SCLK	Input	SPI Serial Clock
2	DATA	Input	SPI Serial Data
3	JUMP	Input	Sigma−Delta Modulator Alarm condition value
4	KICK	Input	Watchdog kick
5	CS	Input	SPI Serial Chip Select
6	VSS	Ground	Ground
7	TxA	Output	Transmit Data Modulator output
8	AREF	Input	Analog reference voltage
9	CDREF	Input	Carrier detect reference voltage
10	CBIAS	Output	Comparator bias current
11	VPOR	Input	POR measurement point
12	RxAN	Input	Receive filter amplifier negative terminal
13	VDDA	Power	Analog supply voltage
14	RxAP	Input	Receive filter amplifier positive terminal
15	RxAF	Output	Analog receive filter output
16	RxAFI	Input	Analog receive comparator input
17	XOUT	Output	Crystal oscillator output
18	XIN	Input	Crystal oscillator input
19	VSS	Ground	Ground
20	TEST1	Input	Test pin. Tie to GND
21	TEST2	Input	Test pin. Tie to VDD
22	RTSB	Input	Request to send
23	TxD	Input	Input transmit data, transmit HART data stream from microcontroller
24	RESETB	Open Drain	Reset all digital logic when low
25	RxD	Output	Received demodulated HART data to microcontroller
26	CD	Output	Carrier detect output
27	MODE	Input	Mode pin to select external or internal oscillator
28	DACREF	Input	Sigma−Delta Modulator Reference Voltage
29	DAC	Output	Sigma−Delta Modulator Output
30	VDD	Power	Digital supply voltage
31	CLK1	Output	Programmable Clock Output 1
32	CLK2	Output	Programmable Clock Output 2
−	EP	Ground	Exposed pad. Connect to GND

Table 9. PIN DESCRIPTIONS

Symbol	Pin Name	Description
AREF	Analog reference voltage	Receiver Reference Voltage. See Table 2.
CDREF	Carrier detect reference voltage	Carrier Detect Reference voltage. The value should be 80 mV below AREF to set the carrier detection to a nominal of 100 mV_{p-p}.
RESETB	Reset digital logic	When at logic low (V_{SS}) this input holds all the digital logic in reset. During normal operation RESETB should be at V_{DD}.
RTSB	Request to send	Active−low input selects the operation of the modulator. TxA is enabled when this signal is low. This signal must be held high during power−up.
RxAP	Analog filter amplifier positive terminal	Positive terminal of the receive filter. For a reference implementation of the receive filter see Figure 2
RxAN	Analog filter amplifier positive terminal	Negative terminal of the receive filter. For a reference implementation of the receive filter see Figure 2
RxAFI	Analog receive comparator input	Positive input of the carrier detect comparator and the receiver filter comparator.
TxD	Digital transmit input	Input to the modulator accepts digital data in NRZ form. When TxD is low, the modulator output frequency is 2200 Hz. When TxD is high, the modulator output frequency is 1200 Hz.
XIN	Oscillator input	Input to the internal oscillator must be connected to a parallel mode ceramic resonator when using the internal oscillator or grounded when using an external clock signal.
XOUT	Oscillator output	Output from the internal oscillator must be connected to an external clock signal or to a parallel mode ceramic resonator when using the internal oscillator.
CLK1	Programmable Clock Output	Output signal derived from oscillator output, frequency division set by internal register.
CLK2	Programmable Clock Output	Output signal derived from oscillator output, frequency division set by internal register.
CBIAS	Comparator bias current	Connection to the external bias resistor. R_{BIAS} should be selected such that AREF / R_{BIAS} = 10 μA ± 5%
CD	Carrier detect output	Output goes high when a valid input is recognized on RxA. If the received signal is greater than the threshold specified on CDREF for four cycles of the RxA signal, the valid input is recognized.
RxAF	Analog receive filter output	The output of the three pole high pass receive data filter
RxD	Digital receive output	Signal outputs the digital receive data. When the received signal (RxA) is 1200 Hz, RxD outputs logic high. When the received signal (RxA) is 2200 Hz, RxD outputs logic low. The HART receive data stream is only active if Carrier Detect (CD) is high.
MODE	Digital input	Selects the clock source. Connecting this pin to VDD disables the internal oscillator. The chip then requires an external clock source. Connecting this pin to VSS enables the internal oscillator to drive the external crystal or ceramic resonator
TxA	Analog transmit output	Transmit Data Modulator Output. A trapezoidal shaped waveform with a frequency of 1200 Hz or 2200 Hz corresponding to a data value of 1 or 0 respectively applied to TxD. TxA is active when RTSB is low. TxA equals 0.5 V when RTSB is high.
SCLK	SPI bus clock line	Serial communication clock line
DATA	SPI bus data line	Serial communication data line.
CS	SPI bus chip select	Serial communication chip select line. Pulled high by microcontroller while a frame is transmitted.
JUMP	DAC Alarm value	When a problem is detected, such as a clock failure or the watchdog going off, the DAC will jump to VSS or DACREF, depending on whether this pin is connected to VSS or VDD respectively.
DACREF	DAC Reference	This is the high value of the output and can be connected to any voltage between AREF and VDD.
DAC	DAC Output	Output of a 17 bit Sigma−Delta Modulator
KICK	Watchdog Kick	Periodically a pulse should be provided to reset the watchdog. This can be configured in internal registers for an internal 1.8kHz signal, or to an external signal provided to this pin.
VPOR	POR Input	Input to the POR comparator. The voltage on this pin is compared with AREF. An external resistor divider should divide the supply voltage to this pin.
VDD	Digital power	Power for the digital modem circuitry
VDDA	Analog supply voltage	Power for the analog modem circuitry
VSS	Ground	Digital ground
VSSA	Analog ground	Analog ground

Functional Description

The NCN5193 is a single-chip modem for use in Highway Addressable Remote Transducer (HART) field instruments and masters. The modem IC contains a transmit data modulator with signal shaper, carrier detect circuitry, an analog receiver, demodulator circuitry and an oscillator, as shown in the block diagram in Figure 1.

The modulator accepts digital data at its digital input TxD and generates a trapezoidal shaped FSK modulated signal at the analog output TxA. A digital “1” or mark is represented with a frequency of 1200 Hz. A digital “0” or space is represented with a frequency of 2200 Hz. The used bit rate is 1200 baud.

The demodulator receives the FSK signal at its analog input, filters it with a band-pass filter and generates 2 digital signals: RxD: Received Data and CD: Carrier Detect. At the digital output RxD the original modulated signal is received. CD outputs the Carrier Detect signal. It goes logic high if the received signal is above 100 mVpp during 4 consecutive carrier periods.

The oscillator provides the modem with a stable time base using either a simple external resonator or an external clock source.

Detailed Description

Modulator

The modulator accepts digital data in NRZ form at the TxD input and generates the FSK modulated signal at the TxA output.

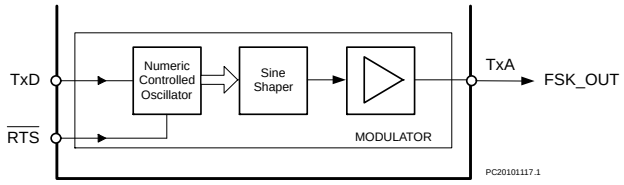


Figure 4. Modulator Block Diagram

A logic “1” or mark is represented by a frequency f_m = 1200 Hz. A logic “0”or space is represented by a frequency f_s = 2200 Hz.

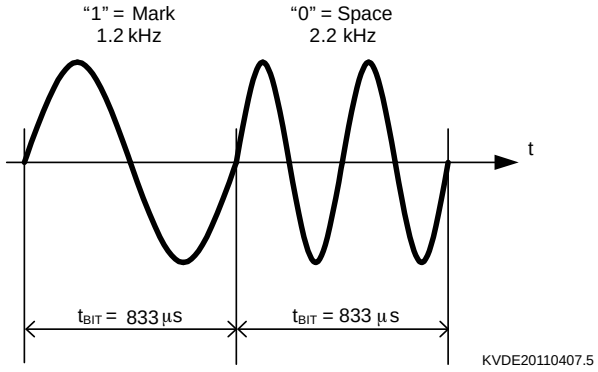


Figure 5. Modulation Timing

The Numeric Controlled Oscillator (NCO) works in a phase continuous mode preventing abrupt phase shifts when switching between mark and space frequency. The control signal “Request To Send” (RTSB) enables the NCO. When RTSB is logic low the modulator is active and NCN5193 is in transmit mode. When RTSB is logic high the modulator is disabled and NCN5193 is in receive mode.

The digital outputs of the NCO are shaped in the Wave Shaper block to a trapezoidal signal. This circuit controls the rising and falling edge to be inside the standard HART waveshape limits. Figure 6 shows the transmit-signal forms captured at TxA for mark and space frequency. The slew rates are SR_m = 1860 V/s at the mark frequency and SR_s = 3300 V/s at the space frequency. For AREF = 1.235 V, TxA will have a voltage swing from approximately 0.25 to 0.75 V_{DC}.

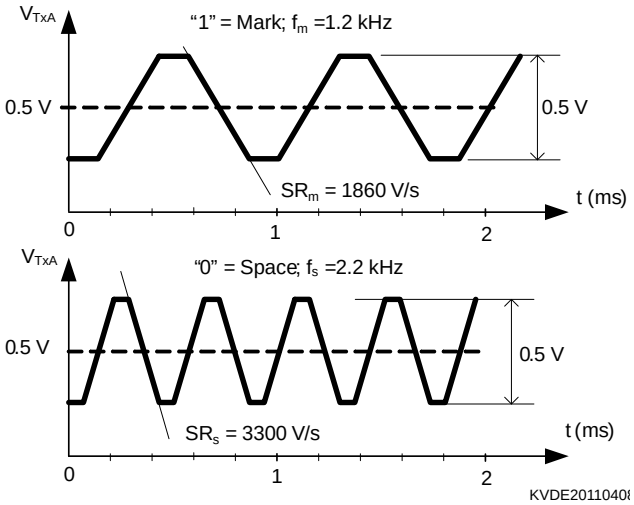


Figure 6. Modulator shaped output signal for Mark and Space frequency at TxA pin.

Demodulator

The demodulator accepts a FSK signal at the RxA input and reconstructs the original modulated signal at the RxD output. Figure 7 illustrates the demodulation process.

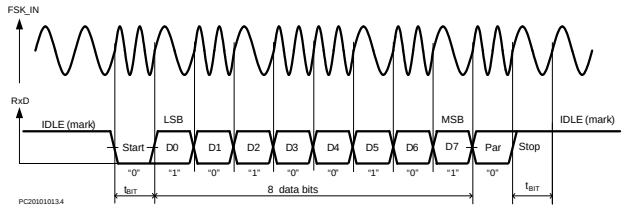


Figure 7. Modulation Timing

This HART bit stream follows a standard 11-bit UART frame with Start, Stop, 8 Data – and 1 Parity bit (odd). The communication speed is 1200 baud.

Receive Filter and Comparator

The received FSK signal first is filtered using a band-pass filter build around the low noise receiver operational amplifier. This filter blocks interferences outside the HART signal band.

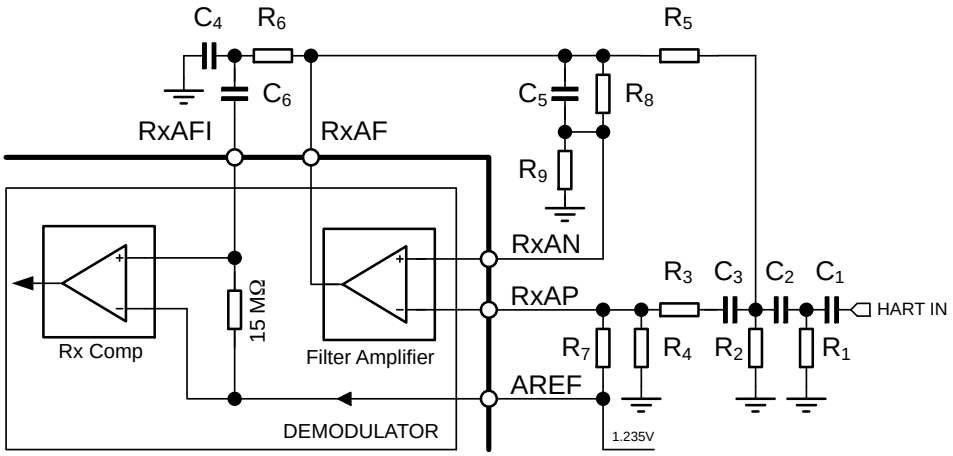


Figure 8. Demodulator Receive Filter and Signal Comparator

The filter output is fed into the Rx comparator. The threshold value equals the analog ground making the comparator to toggle on every zero crossing of the filtered FSK signal. The maximum demodulator jitter is 12% of one bit given the input frequencies are within the HART specifications, a clock frequency of 460.8 kHz (±1.0 %) and zero input (RxA) asymmetry.

Carrier Detect Circuitry

Low HART input signal levels increases the risk for the generation of bit errors. Therefore the minimum signal amplitude is set to 80−120 mVpp. If the received signal is below this level the demodulator is disabled.

This level detection is done in the Carrier Detector. The output of the demodulator is qualified with the carrier detect signal (CD), therefore, only RxA signals large enough to be detected (100 mV_{p-p} typically) by the carrier detect circuit produce received serial data at RxD.

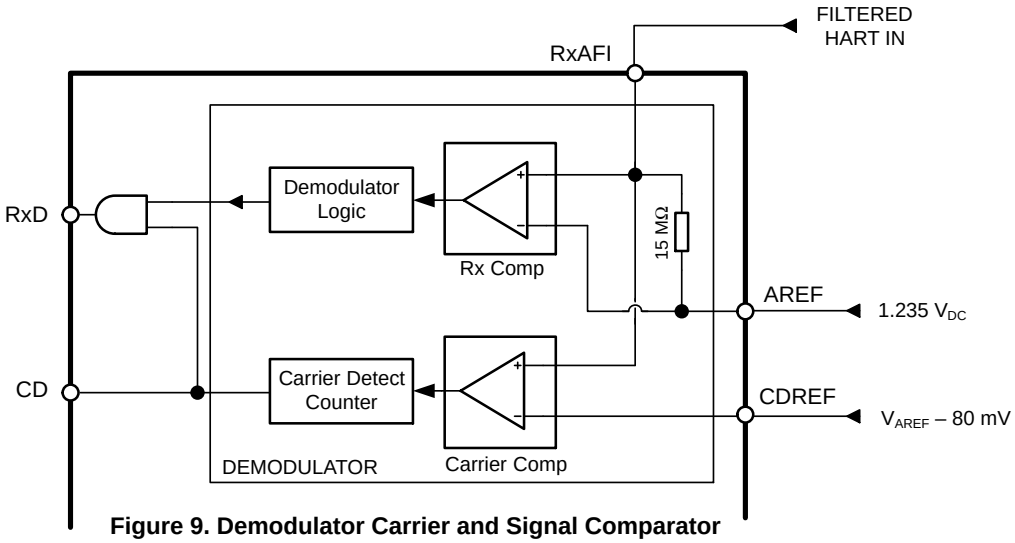


Figure 9. Demodulator Carrier and Signal Comparator

The carrier detect comparator shown in Figure 9 generates logic low output if the RxAFI voltage is below CDREF. The comparator output is fed into a carrier detect block. The carrier detect block drives the carrier detect output pin CD high if RTSB is high and four consecutive pulses out of the comparator have arrived. CD stays high as long as RTSB is high and the next comparator pulse is received in less than 2.5 ms. Once CD goes inactive, it takes four consecutive pulses out of the comparator to assert CD again. Four consecutive pulses amount to 3.33 ms when the received signal is 1200 Hz and to 1.82 ms when the received signal is 2200 HZ. The difference between RxD and RxD_ENH is evident when CD is low: RxD is then also low, while RxD_ENH is then high. When CD is high, RxD and RxD_ENH have the same output.

Miscellaneous Analog Circuitry

Voltage References

The NCN5193 requires two voltage references, AREF and CDREF. AREF sets the DC operating point of the internal operational amplifiers and is the reference for the

Rx comparator. The ON Semiconductor LM285D 1.235 V reference is recommended.

The level at which CD (Carrier Detect) becomes active is determined by the DC voltage difference (CDREF - AREF). Selecting a voltage difference of 80 mV will set the carrier detect to a nominal 100 mV_{p-p}.

Bias Current Resistor

The NCN5193 requires a bias current resistor R_{BIAS} to be connected between CBIAS and V_{SS}. The bias current controls the operating parameters of the internal operational amplifiers and comparators and should be set to 2.5 μA.

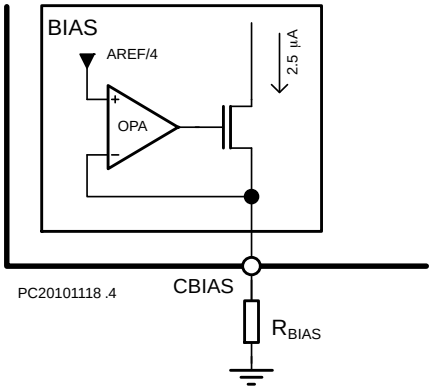


Figure 10. Bias Circuit

The value of the bias current resistor is determined by the reference voltage AREF and the following formula:

$$R_{BIAS} = \frac{VREF}{4 \times 2.5\ \mu A}$$

The recommended bias current resistor is 120 KΩ when AREF is equal to 1.235 V.

Oscillator

The clock signal used by NCN5193 can either be 460.8 kHz, 921.6 kHz, 1.8432 MHz or 3.6864 MHz. This can be provided by an external clock or a resonator or crystal connected to the internal oscillator. This is selected by connecting pin 27 to VDD (for external oscillator) or VSS (for internal oscillator). The correct divider value must be chosen so that the internal system clock is always 460.8 kHz. This divider value can be set in the Clock Configuration Register (CCR), bits 1−0. In the CCR, divider values can also be chosen for the CLK1 and CLK2 outputs. These values can be freely chosen and do not affect operation of the HART transceiver.

Internal Oscillator Option

The oscillator cell will function with a 460.8 kHz, 921.6 kHz, 1.8432 MHz or 3.6864 MHz crystal or ceramic resonator. A parallel resonant ceramic resonator can be connected between XIN and XOUT. Figure 11 illustrates the crystal option for clock generation using a 460.8 kHz (±1% tolerance) parallel resonant crystal and two tuning capacitors C_x. The actual values of the capacitors may depend on the recommendations of the manufacturer of the resonator. Typically, capacitors in the range of 10 pF to 470 pF are used. Additionally, a resistor may be required between XOUT and the crystal terminal, depending on manufacturer recommendation.

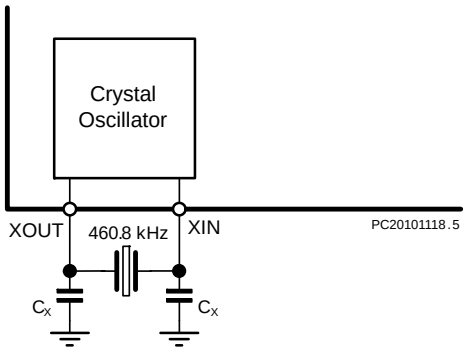


Figure 11. Crystal Oscillator

External Clock Option

It may be desirable to use an external clock as shown in Figure 12 rather than the internal oscillator. In addition, the NCN5193 consumes less current when an external clock is used. Minimum current consumption occurs with the clock connected to XOUT and XIN connected to V_{SS}.

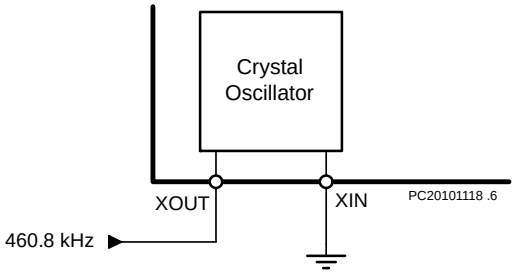


Figure 12. Oscillator with External Clock

Reset

The NCN5193 modem includes a Power on Reset block. An external resistor division of the supply voltage is required, and should be tied to pin VPOR. This pin is attached to an internal comparator, and is compared to the AREF voltage. When this comparator trips, the RESETB pin will be pulled low and the IC will reset. After VPOR returns to a valid level, the RESETB pin will be held low for at least an additional 35 ms (may be longer depending on clock frequency). The RESETB pin will also be pulled low when a failure is detected by the watchdog timer. When the microcontroller fails to provide a periodical kick signal, either by a pulse on the kick pin or by an update to the sigma−delta register (configurable in the GCR), the watchdog will pull down the RESETB pin for 140 μs. A kick signal should be provided to the IC at least every 53 ms. The watchdog timer can also guard against system clock failures if bit 2 of the GCR is set. In this case, the RESETB pin will also be pulled low when the system clock frequency is outside of 0.5x − 2x the nominal frequency (460.8 kHz).

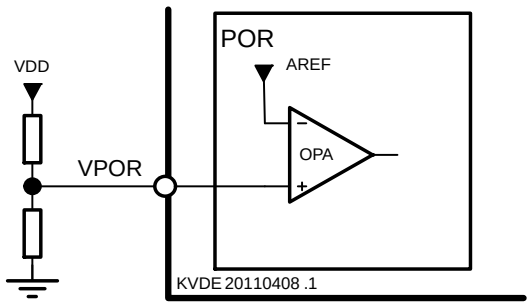


Figure 13. Power on Reset Block

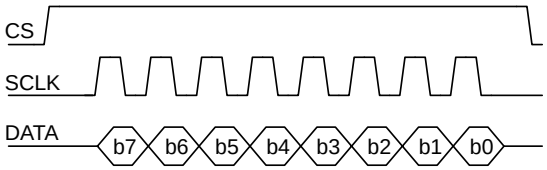


Figure 14. SPI Frame

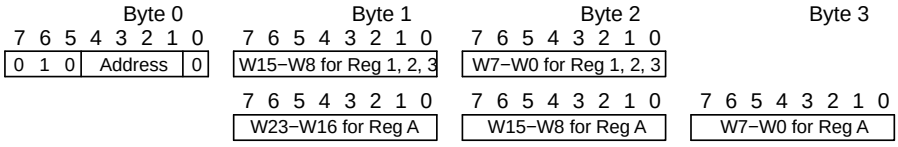


Figure 15. Register Write Format

SPI Communication

The SPI bus on the NCN5193 is made up of three signals; DATA, SCLK, and CS operating in SPI mode 1 (CPOL = 0, CPHA = 1, as shown in Figure 14).

CS should first go high at least one clock cycle before the other signals change. One clock cycle is 2.17 μs at a master clock frequency of 460.8 kHz.

SCLK can begin to clock in DATA serially to the chip on the falling edge of SCLK. SCLK should have a maximum frequency of 460.8 kHz. The format of the data should be most significant bit first.

DATA is shifted into the chip on the falling edge of SCLK, and thus for correct operation DATA should change only on the rising edge of SCLK. The first bit shifted in is the MSB. Once the data is shifted in, CS should go low no sooner than one clock cycle after the last rising edge of the last byte of SCLK. To write to a register, first a command byte must be sent which includes the register address (as shown in Figure 15), followed by 2 bytes (for GCR, CCR, and ACR) or 3 bytes (for SDR) of data. When writing data to the GCR, CCR, or ACR registers, the first byte must be the bitwise inverse of the configuration data in the second byte.

Internal Registers

The NCN5193 has four registers to setup its internal operation. In Tables 10 to 16 an explanation of their usage is given, together with their reset values.

Table 10. GENERAL CONFIGURATION REGISTER (GCR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01	**Reset**	1	0	0	0	0	1	0	1
	Data	-	-	-	RXD_IDLE	-	WDT_CLK	WDT_KICK	

The general configuration register is used to set the RxD idle state, enable or disable the monitoring of the system clock and setting the watchdog timer kick source. A write to this register should always be preceded with an inverted value to the shadow register.

Table 11. GENERAL CONFIGURATION REGISTER PARAMETERS

Parameter	Value		Description	Info
RXD_IDLE	0	Low	Sets the idle state for the RxD pin (when CD is low)	
	1	High		
WDT_CLK	0	Enable	Disable/Enable monitoring of the clock frequency by the watchdog timer.	
	1	Disable		
WDT_KICK	00	Disable	Kick signal to watchdog timer is disabled	
	01	External	Watchdog kick source is a pulse on the KICK pin	
	10	Sigma-Delta	Watchdog kick source is an write to the Sigma-Delta Data register (SDR)	
	11			

Table 12. CLOCK CONFIGURATION REGISTER (CCR)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x02	Reset	1	0	1	1	0	1	1	1
	Data	CLK2_DIV			CLK1_DIV			SYSCLK_DIV	

The clock configuration register is used to set the correct division ratios for both clock outputs and the system clock. A write to this register should always be preceded with an inverted value to the shadow register.

Table 13. CLOCK CONFIGURATION REGISTER PARAMETERS

Parameter	Value		Description	Info
CLK2_DIV	000	Divide by 1	Set the clock division value for clock output 2 (CLK2) with regard to the oscillator frequency.	
	001	Divide by 2		
	010	Divide by 3		
	011	Divide by 4		
	100	Divide by 5		
	101	Divide by 8		
	110	Divide by 16		
	111	Divide by 32		
CLK1_DIV	000	Divide by 1	Set the clock division value for clock output 1 (CLK1) with regard to the oscillator frequency.	
	001	Divide by 2		
	010	Divide by 3		
	011	Divide by 4		
	100	Divide by 5		
	101	Divide by 8		
	110	Divide by 16		
	111	Divide by 32		
SYSCLK_DIV	00	Divide by 1	Set the clock division value for the system clock with regard to the oscillator frequency. These bits must be set so the system clock is 460.8 kHz	
	01	Divide by 2		
	10	Divide by 4		
	11	Divide by 8		

Table 14. ANALOG CONFIGURATION REGISTER – ACR

General Configuration Register (GCR)									
Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x03	Reset	1	1	1	1	1	1	0	1
	Data	MOD_EN	RXAMP_EN	RXCMP_EN	CDCMP_EN	TXAMP_EN	MODDAC_EN	WDOSC_EN	SDDAC_EN

The analog configuration register is used to enable or disable various analog blocks. A write to this register should always be preceded with an inverted value to the shadow register.

Table 15. ANALOG CONFIGURATION REGISTER PARAMETERS

Parameter	Value		Description	Info
MOD_EN	0	Enable	Disable/Enable the modulator/demodulator	
	1	Disable		
RXAMP_EN	0	Enable	Disable/Enable the receive filter opamp	
	1	Disable		
RXCMP_EN	0	Enable	Disable/Enable the receive comparator	
	1	Disable		
CDCMP_EN	0	Enable	Disable/Enable the carrier detect comparator	
	1	Disable		
TXAMP_EN	0	Enable	Disable/Enable the transmit output amplifier	
	1	Disable		
MODDAC_EN	0	Enable	Disable/Enable the DAC used to provide the waveshaping to the modulator	
	1	Disable		
WDOSC_EN	0	Enable	Disable/Enable the watchdog timer oscillator	
	1	Disable		
SDDAC_EN	0	Enable	Disable/Enable the sigma-delta DAC	
	1	Disable		

Table 16. SIGMA-DELTA DAC REGISTER – SDR

General Configuration Register (GCR)					
Address		**Bit 23:16**	**Bit 15:8**	**Bit 7**	**Bit 6:0**
0x0A	**Reset**	0x00	0x00	0	0x00
	Data	Data 16:9	Data 8:1	Data 0	-

The sigma-delta register is used to update the output value of the 17-bit sigma delta modulator. The sigma-delta modulator is disabled at reset and must be enabled in the ACR first before the value in the SDR will appear at the sigma-delta output.

Sigma Delta DAC

The NCN5193 Modem has an integrated Sigma−Delta Modulator for use in a current loop slave transmitter. Through this DAC, an analog value can be set and transmitted across the current loop. For more information on how to create a current loop slave transmitter, see application notes on the ON Semiconductor website. The DAC output will switch between 0 V and the voltage provided to DACREF. To achieve maximum accuracy, the DACREF voltage should be kept stable, so that power supply variations are not visible in the DAC output. The Sigma−Delta modulator output can be set through the Sigma Delta Register (SDR). When a clock failure is detected, using an internal oscillator, the DAC output will jump to the level set by the JUMP pin, until the IC is reset or a rising flank is detected on KICK.

Ordering Information

The NCN5193 is available in a 32−pin no lead quad flat pack (NQFP). Use the following part numbers when ordering. Contact your local sales representative for more information: www.onsemi.com.

Table 17. ORDERING INFORMATION

Part Number	Temperature Range	Package	Shipping†
NCN5193MNTWG	−40°C to +85°C (Industrial)	32−pin NQFP Green/RoHS compliant	1000 / Tape & Reel

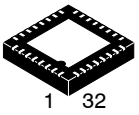
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

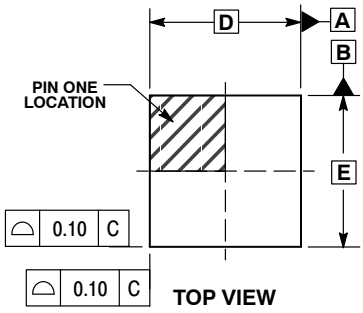
ON Semiconductor®

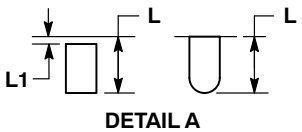
QFN32 5x5, 0.5P
CASE 485EK
ISSUE A

DATE 29 SEP 2015

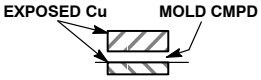


SCALE 2:1

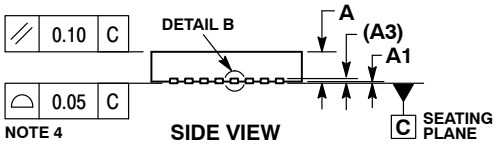


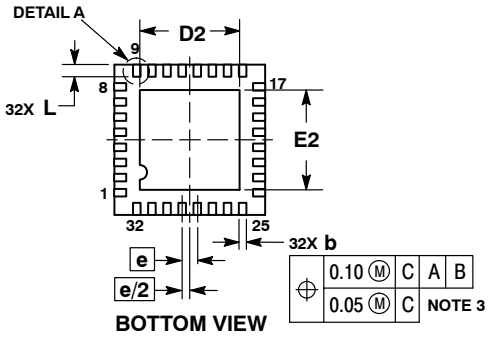


DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION

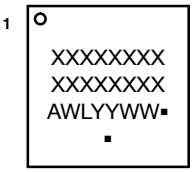




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	0.90
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	3.20	3.40
E	5.00 BSC	
E2	3.20	3.40
e	0.50 BSC	
L	0.35	0.45
L1	---	0.15

GENERIC MARKING DIAGRAM*

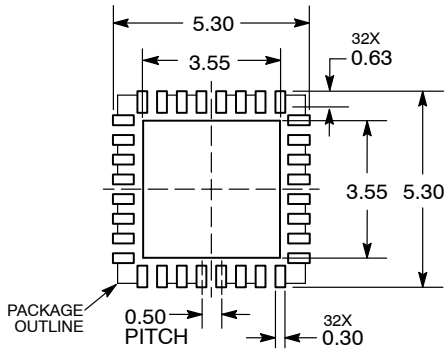


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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