

Voltage Regulator - Low Dropout

400 mA

NCV4274C

Description

The NCV4274C is a precision micro-power voltage regulator with an output current capability of 400 mA available in the DPAK, D2PAK and SOT-223 packages.

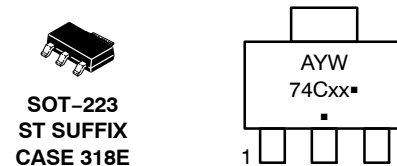
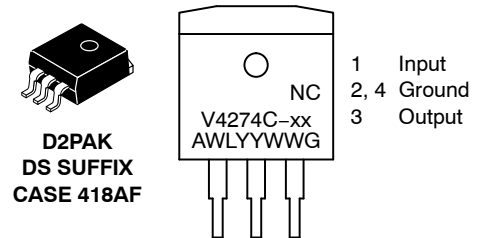
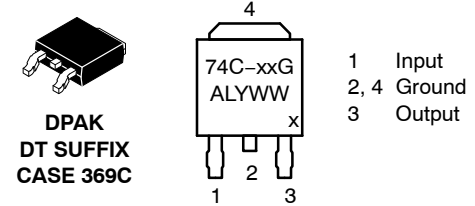
The output voltage is accurate within $\pm 2.0\%$ with a maximum dropout voltage of 0.5 V with an input up to 40 V. Low quiescent current is a feature drawing only 125 μA with a 1 mA load. This part is ideal for automotive and all battery operated microprocessor equipment.

The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments.

Features

- 3.3 V, 5.0 V, $\pm 2.0\%$ Output Options
- Low 125 μA Quiescent Current at 1 mA load current
- 400 mA Output Current Capability
- Fault Protection
- +60 V Peak Transient Voltage with Respect to GND
 - -42 V Reverse Voltage
 - Short Circuit
 - Thermal Overload
- Very Low Dropout Voltage
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices

MARKING DIAGRAMS



xx = 33 (3.3 V)
= 50 (5.0 V)
A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 12.

NCV4274C

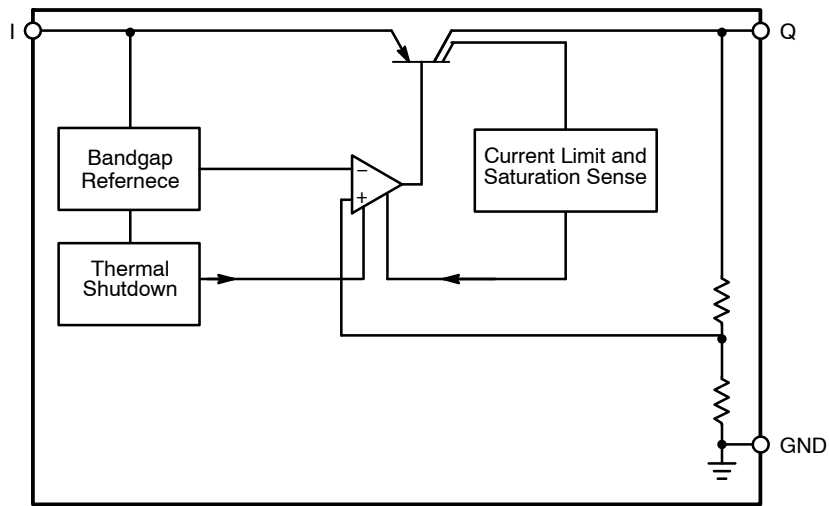


Figure 1. Block Diagram

Pin Definitions and Functions

| Pin No. | Symbol | Function |
|---------|--------|---|
| 1 | I | Input; Bypass directly at the IC with a ceramic capacitor to GND. |
| 2,4 | GND | Ground |
| 3 | Q | Output; Bypass with a capacitor to GND. |

ABSOLUTE MAXIMUM RATINGS

| Pin Symbol, Parameter | | Symbol | Condition | Min | Max | Unit |
|---|---------|--------------------|-------------|--------------------|--------------------|------|
| I, Input-to-Regulator | Voltage | V_I | | -42 | 45 | V |
| | Current | I_I | | Internally Limited | Internally Limited | |
| I, Input peak Transient Voltage to Regulator with Respect to GND (Note 1) | | V_I | | | 60 | V |
| Q, Regulated Output | Voltage | V_Q | $V_Q = V_I$ | -1.0 | 40 | V |
| | Current | I_Q | | Internally Limited | Internally Limited | |
| GND, Ground Current | | I_{GND} | | - | 100 | mA |
| Junction Temperature | | T_J | | -40 | 150 | °C |
| Storage Temperature | | T_{Stg} | | -50 | 150 | °C |
| ESD Capability, Human Body Model (Note 2) | | ESD _{HB} | | 4 | | kV |
| ESD Capability, Machine Model (Note 2) | | ESD _{MM} | | 200 | | V |
| ESD Capability, Charged Device Model (Note 2) | | ESD _{CDM} | | 1 | | kV |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Load Dump Test B (with centralized load dump suppression) according to ISO16750-2 standard. Guaranteed by design. Not tested in production. Passed Class C.
- This device series incorporates ESD protection and is tested by the following methods:
 ESD HBM tested per AEC-Q100-002 (EIA/JESD22-A114)
 ESD MM tested per AEC-Q100-003 (EIA/JESD22-A115)
 Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes <50mm² due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS-002-2014.

OPERATING RANGE

| Parameter | Symbol | Condition | Min | Max | Unit |
|-------------------------------|--------|-----------|-----|-----|------|
| Input Voltage (5.0 V Version) | V_I | | 5.5 | 40 | V |
| Input Voltage (3.3 V Version) | V_I | | 4.5 | 40 | V |
| Junction Temperature | T_J | | -40 | 150 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

THERMAL RESISTANCE

| Parameter | | Symbol | Condition | Min | Max | Unit |
|---------------------|---------|---------------------------------|-----------|-----|------------------|------|
| Junction-to-Ambient | DPAK | R_{thja} | | – | 72.5 (Note 3) | °C/W |
| Junction-to-Ambient | D2PAK | R_{thja} | | – | 56.7 (Note 3) | °C/W |
| Junction-to-Case | DPAK | R_{thjc} | | – | 5.8 | °C/W |
| Junction-to-Case | D2PAK | R_{thjc} | | – | 5.8 | °C/W |
| Junction-to-Tab | SOT-223 | Ψ_{JLX} , Ψ_{LX} | | – | 15.6 (Note 3) | °C/W |
| Junction-to-Ambient | SOT-223 | $R_{\theta JA}$, θ_{JA} | | – | 87 (Note 3) | °C/W |

3. 1 oz copper, 300 mm² copper area, single-sided FR4 PCB.

MOISTURE SENSITIVITY LEVEL (Note 4)

| Parameter | Symbol | Condition | Min | Max | Unit |
|----------------------------|--------|---------------------------|--------|--------|------|
| Moisture Sensitivity Level | MSL | DPAK and D2PAK SOT-223 | 1 3 | – – | |

4. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NCV4274C

ELECTRICAL CHARACTERISTICS

$-40^{\circ}\text{C} < T_J < 150^{\circ}\text{C}$; $V_I = 13.5\text{ V}$ unless otherwise noted.

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|--|-----------------|--|------|-----|------|--------------------|
| REGULATOR | | | | | | |
| Output Voltage (5.0 V Version) | V_Q | $5\text{ mA} < I_Q < 400\text{ mA}$ $6\text{ V} < V_I < 28\text{ V}$ | 4.9 | 5.0 | 5.1 | V |
| Output Voltage (5.0 V Version) | V_Q | $5\text{ mA} < I_Q < 200\text{ mA}$ $6\text{ V} < V_I < 40\text{ V}$ | 4.9 | 5.0 | 5.1 | V |
| Output Voltage (3.3 V Version) | V_Q | $5\text{ mA} < I_Q < 400\text{ mA}$ $4.5\text{ V} < V_I < 28\text{ V}$ | 3.23 | 3.3 | 3.37 | V |
| Output Voltage (3.3 V Version) | V_Q | $5\text{ mA} < I_Q < 200\text{ mA}$ $4.5\text{ V} < V_I < 40\text{ V}$ | 3.23 | 3.3 | 3.37 | V |
| Current Limit (All Versions) | I_Q | $V_Q = 90\% V_{Q\text{TYP}}$ | 400 | 600 | – | mA |
| Quiescent Current | I_q | $I_Q = 1\text{ mA}$ $V_Q = 5.0\text{ V}$ | – | 125 | 250 | μA |
| | | $V_Q = 3.3\text{ V}$ | – | 125 | 250 | μA |
| | | $I_Q = 250\text{ mA}$ $V_Q = 5.0\text{ V}$ | – | 5 | 15 | mA |
| | | $V_Q = 3.3\text{ V}$ | – | 5 | 15 | mA |
| | | $I_Q = 400\text{ mA}$ $V_Q = 5.0\text{ V}$ | – | 10 | 35 | mA |
| | | $V_Q = 3.3\text{ V}$ | – | 10 | 35 | mA |
| Dropout Voltage 5.0 V Version | V_{DR} | $I_Q = 250\text{ mA}$, $V_{\text{DR}} = V_I - V_Q$ $V_I = 5.0\text{ V}$ | – | 250 | 500 | mV |
| Load Regulation (3.3 V and 5 V Versions) | ΔV_Q | $I_Q = 5\text{ mA to } 400\text{ mA}$ | – | 3 | 20 | mV |
| Line Regulation (3.3 V and 5 V Versions) | ΔV_Q | $\Delta V_I = 12\text{ V to } 32\text{ V}$ $I_Q = 5\text{ mA}$ | – | 4 | 25 | mV |
| Power Supply Ripple Rejection | PSRR | $f_r = 100\text{ Hz}$, $V_r = 0.5\text{ V}_{\text{PP}}$ | – | 60 | – | dB |
| Thermal Shutdown Temperature* | T_{SD} | $I_Q = 5\text{ mA}$ | 150 | – | 210 | $^{\circ}\text{C}$ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Guaranteed by design, not tested in production

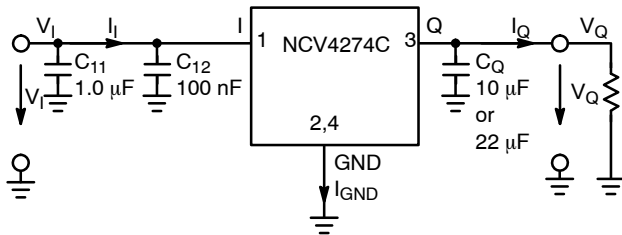


Figure 2. Measuring Circuit

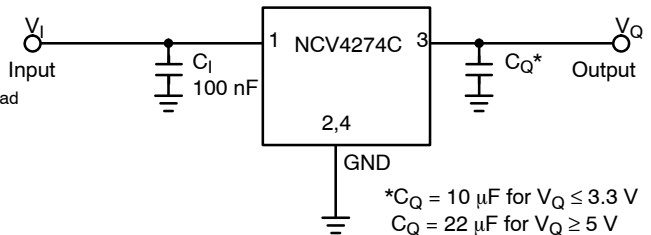


Figure 3. Application Circuit

TYPICAL CHARACTERISTIC CURVES – 5 V VERSION

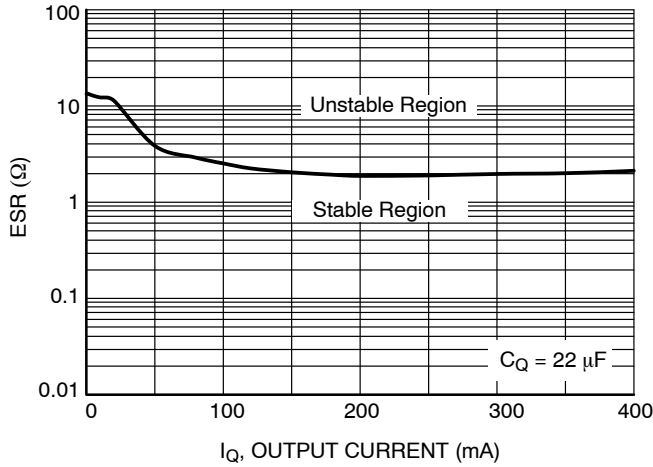


Figure 4. Output Stability with Output Capacitor ESR

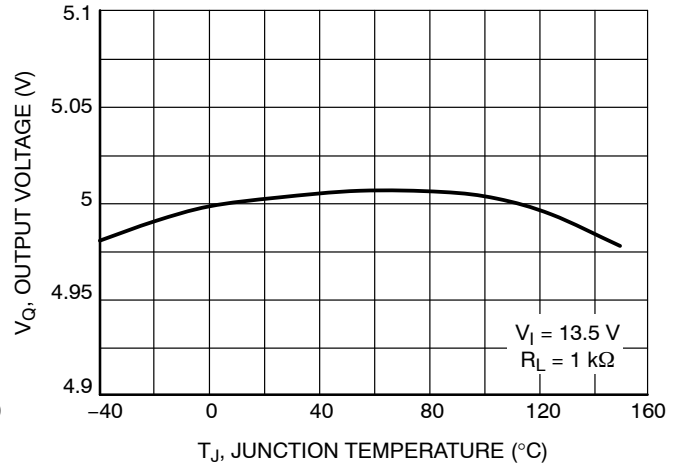


Figure 5. Output Voltage vs. Junction Temperature

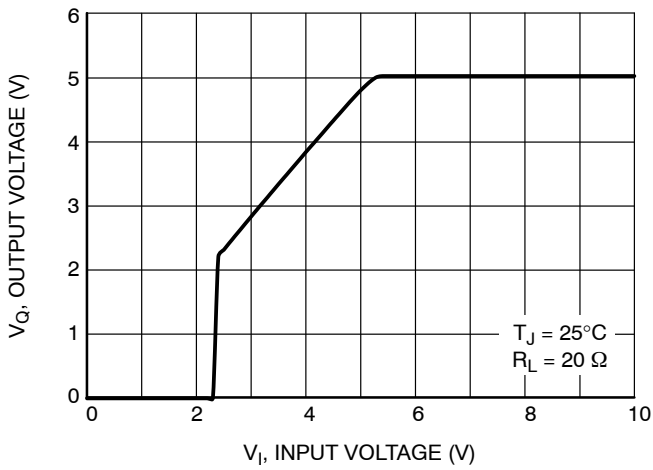


Figure 6. Output Voltage vs. Input Voltage

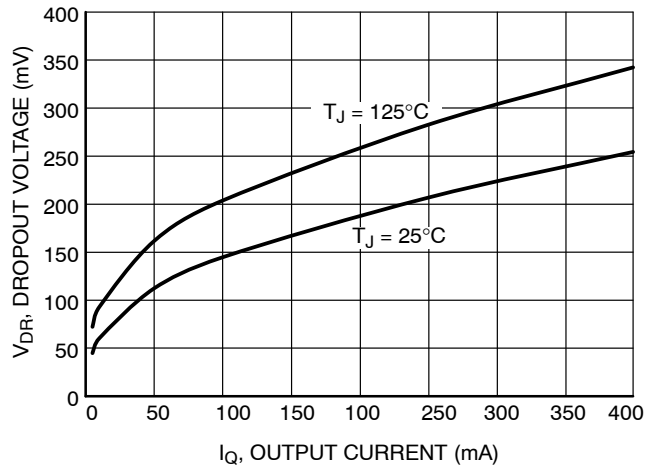


Figure 7. Dropout Voltage vs. Output Current

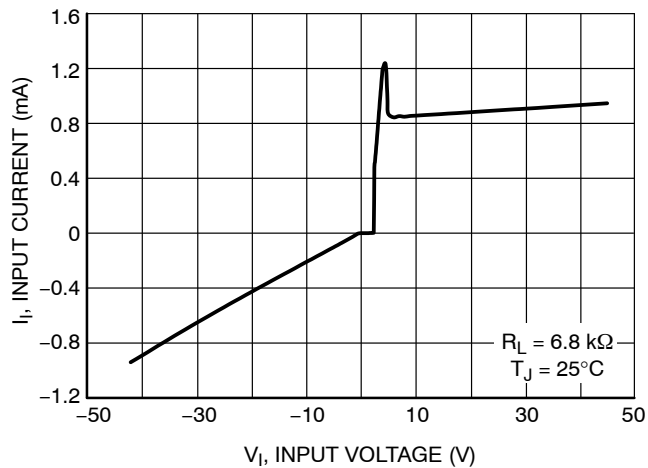


Figure 8. Input Current vs. Input Voltage

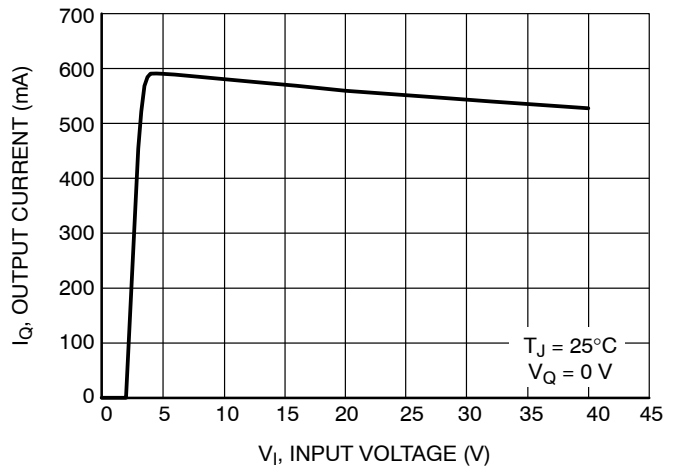


Figure 9. Maximum Output Current vs. Input Voltage

TYPICAL CHARACTERISTIC CURVES – 5 V VERSION

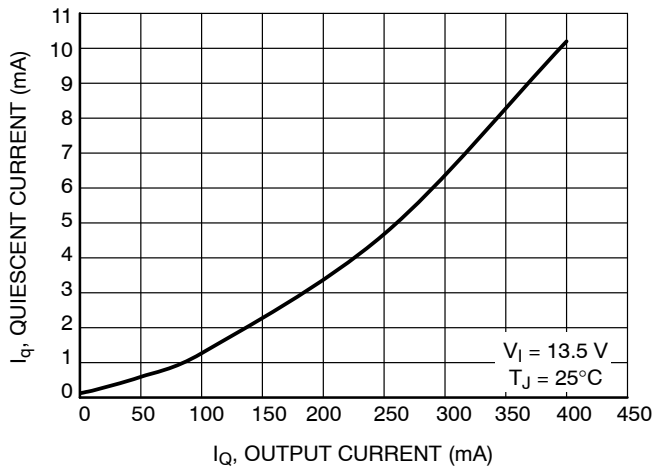


Figure 10. Quiescent Current vs. Output Current (High Load)

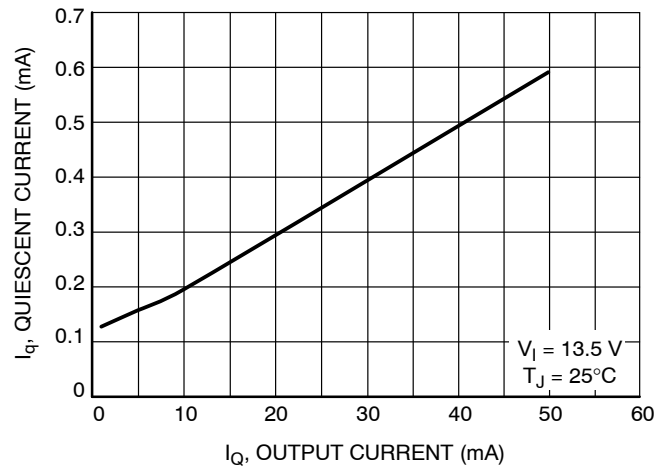


Figure 11. Quiescent Current vs. Output Current (Low Load)

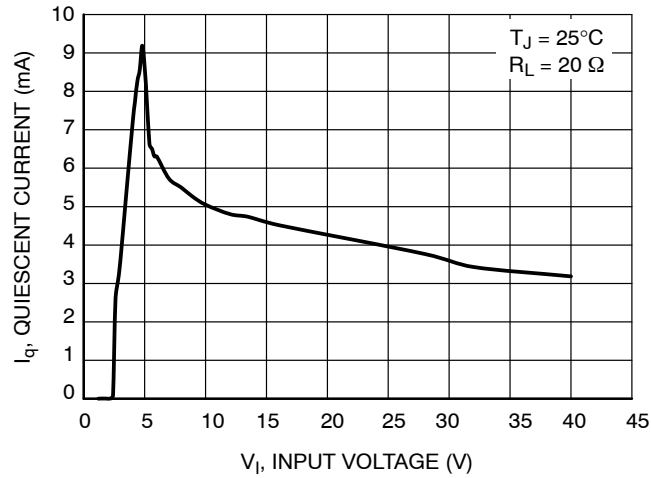


Figure 12. Quiescent Current vs. Input Voltage

TYPICAL CHARACTERISTIC CURVES – 3.3 V VERSION

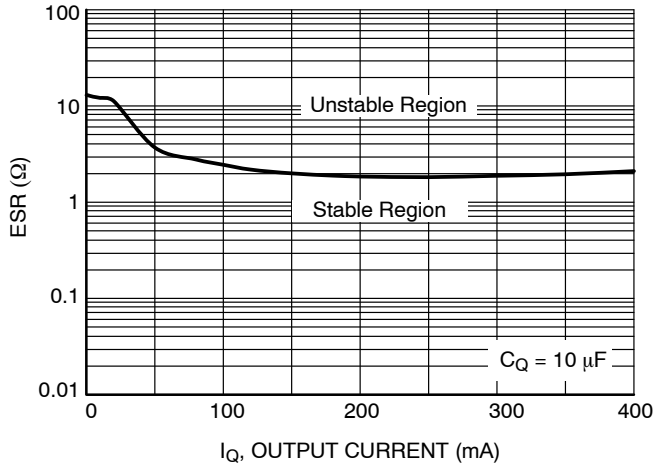


Figure 13. Output Stability with Output Capacitor ESR

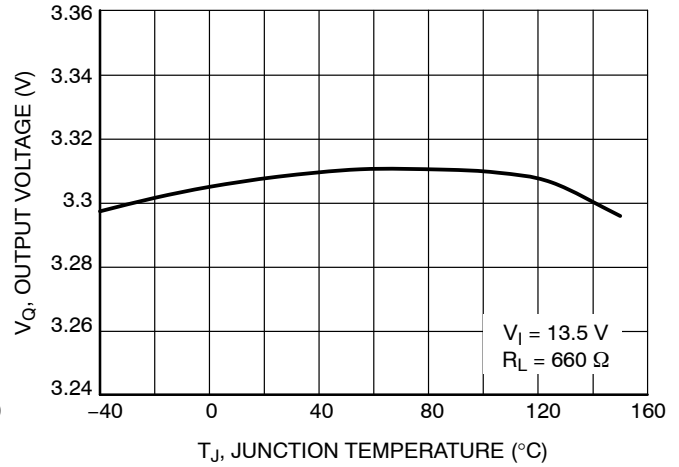


Figure 14. Output Voltage vs. Junction Temperature

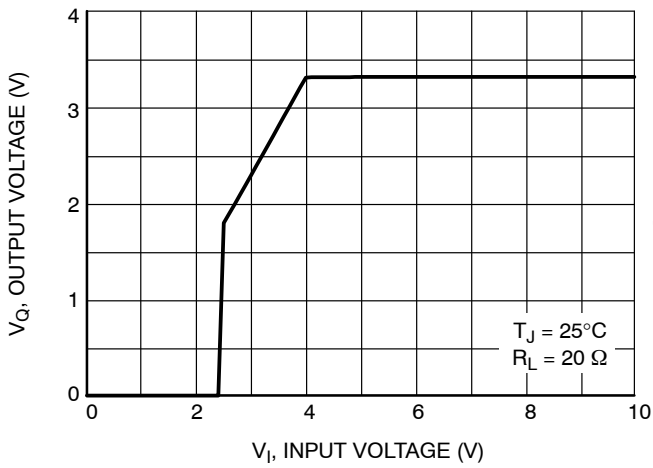


Figure 15. Output Voltage vs. Input Voltage

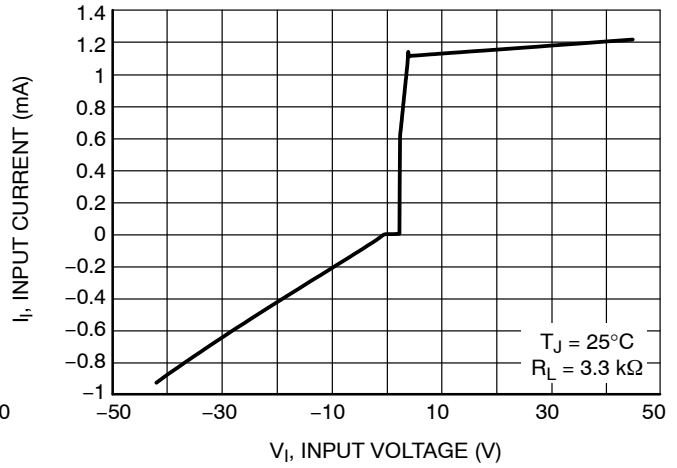


Figure 16. Input Current vs. Input Voltage

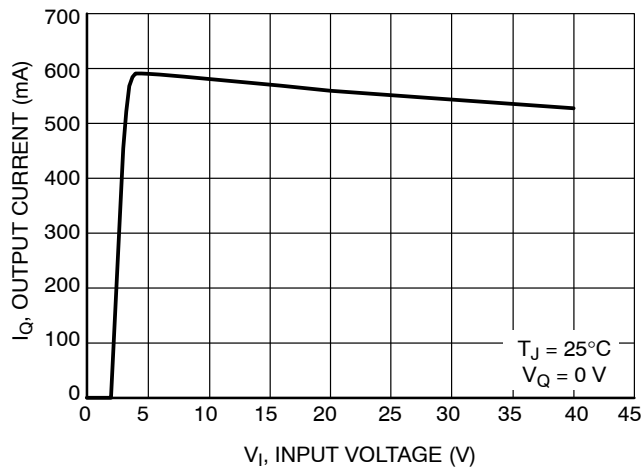


Figure 17. Maximum Output Current vs. Input Voltage

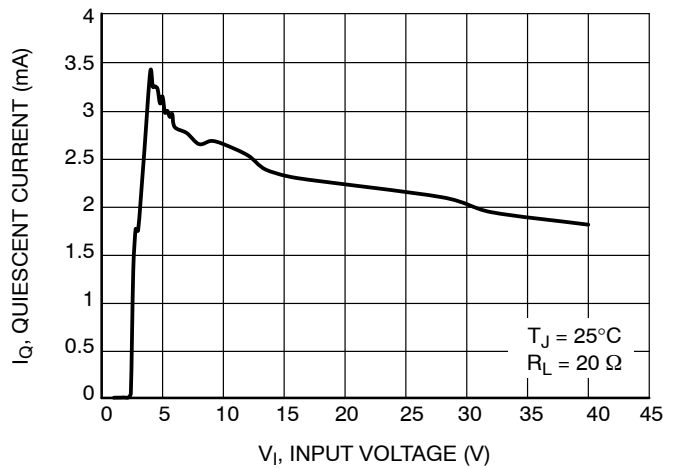


Figure 18. Quiescent Current vs. Input Voltage

TYPICAL CHARACTERISTIC CURVES – 3.3 V VERSION

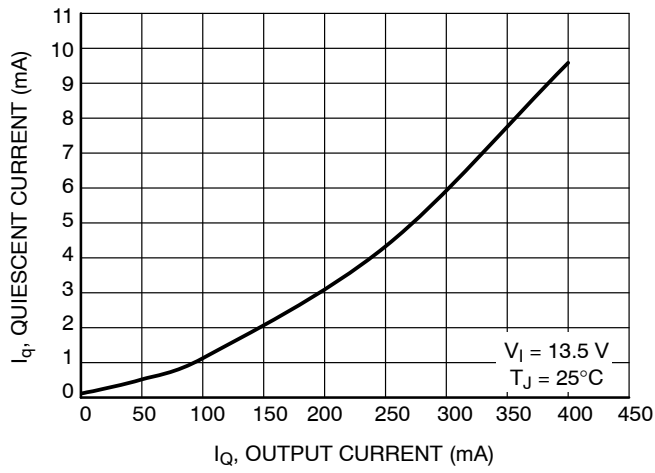


Figure 19. Quiescent Current vs. Output Current (High Load)

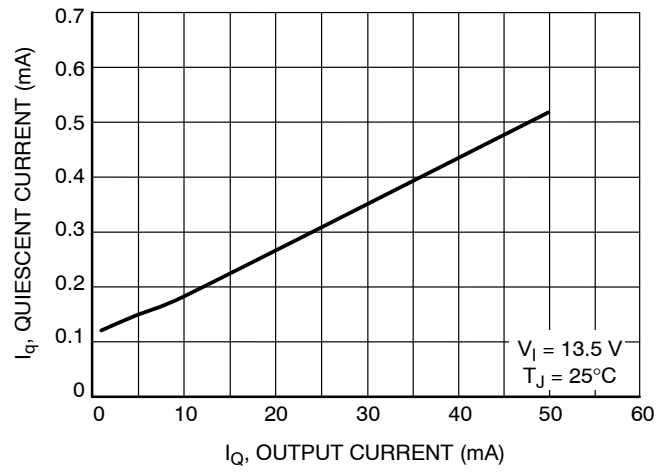


Figure 20. Quiescent Current vs. Output Current (Low Load)

APPLICATION DESCRIPTION

Output Regulator

The output is controlled by a precision trimmed reference and error amplifier. The PNP output has saturation control for regulation while the input voltage is low, preventing over saturation. Current limit and voltage monitors complement the regulator design to give safe operating signals to the processor and control circuits.

Stability Considerations

The input capacitor C_{I1} in Figure 2 is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately $1\ \Omega$ in series with C_{I2} .

The output or compensation capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (-25°C to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The value for the output capacitor C_O shown in Figure 2 should work for most applications; however, it is not necessarily the optimized solution. Actual Stability Regions are shown in a graphs in the Typical Performance Characteristics section.

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 3) is:

$$P_{D(\max)} = [V_{I(\max)} - V_{Q(\min)}]I_{Q(\max)} + V_{I(\max)}I_q \quad (\text{eq. 1})$$

Where:

$V_{I(\max)}$ is the maximum input voltage,

$V_{Q(\min)}$ is the minimum output voltage,

$I_{Q(\max)}$ is the maximum output current for the application, and

I_q is the quiescent current the regulator consumes at $I_{Q(\max)}$.

Once the value of $P_{D(\max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$P_{\theta JA} = \frac{(150^{\circ}\text{C} - T_A)}{P_D} \quad (\text{eq. 2})$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C . In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (\text{eq. 3})$$

Where:

$R_{\theta JC}$ = the junction-to-case thermal resistance,

$R_{\theta CS}$ = the case-to-heat sink thermal resistance, and

$R_{\theta SA}$ = the heat sink-to-ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heat sink and the interface between them. These values appear in data sheets of heat sink manufacturers.

Thermal, mounting, and heat sinking are discussed in the onsemi application note AN1040/D, available on the [onsemi Website](http://www.onsemi.com).

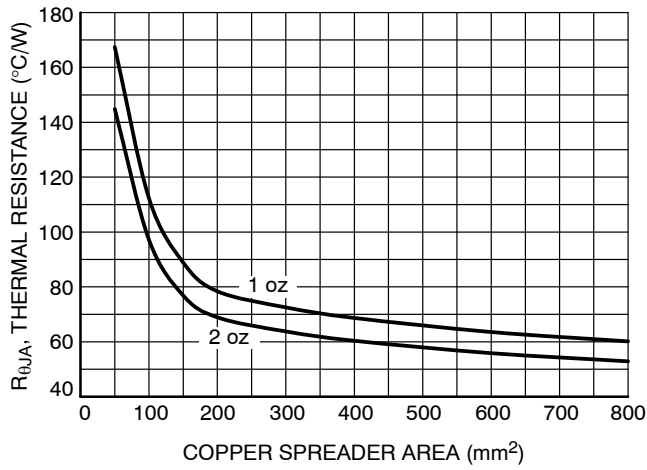


Figure 21. $R_{\theta JA}$ vs. Copper Spreader Area, DPAK 3-Lead

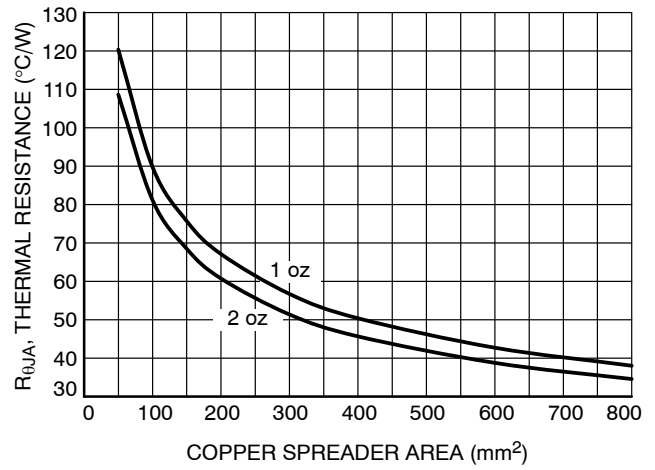


Figure 22. $R_{\theta JA}$ vs. Copper Spreader Area, D²PAK 3-Lead

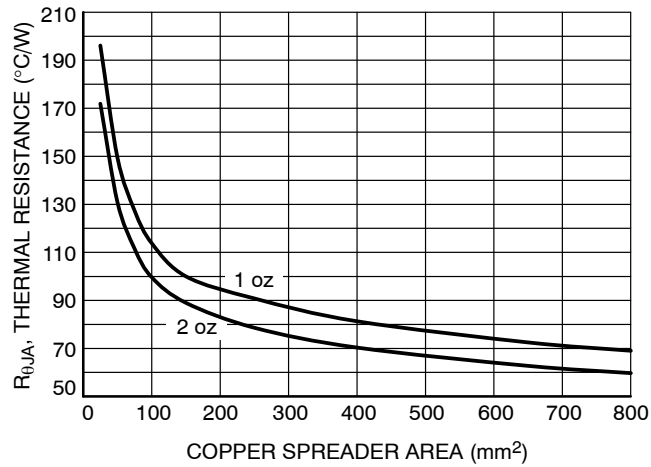


Figure 23. $R_{\theta JA}$ vs. Copper Spreader Area, SOT 223-Lead

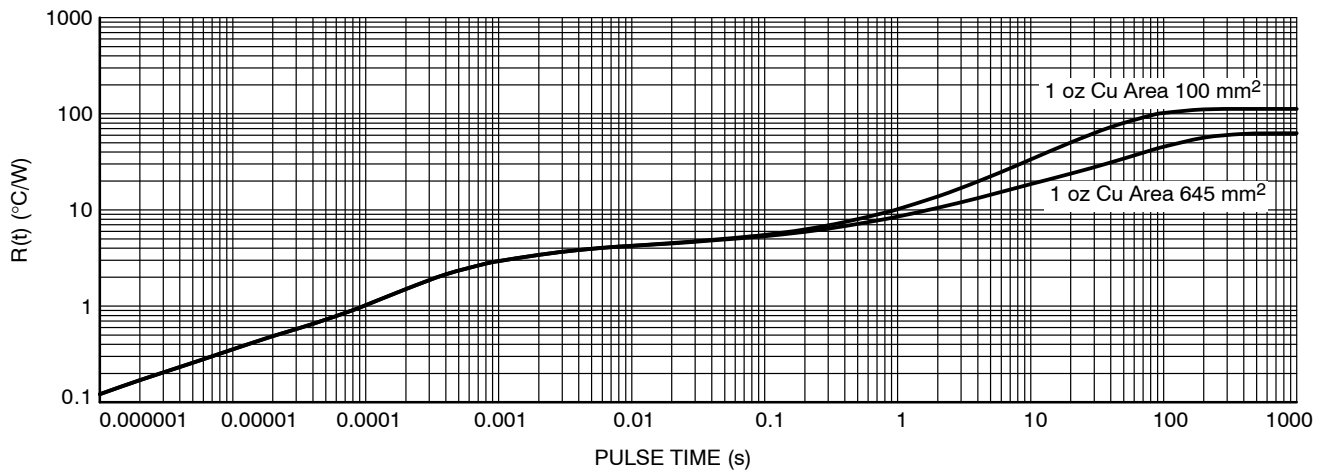


Figure 24. Single-Pulse Heating Curves, DPAK 3-Lead

NCV4274C

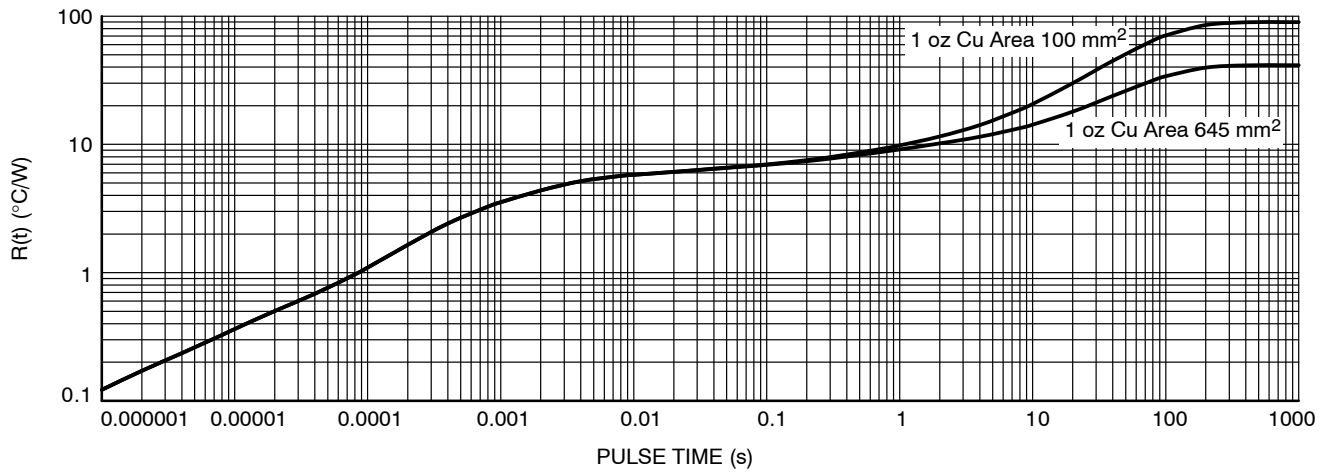


Figure 25. Single-Pulse Heating Curves, D²PAK 3-Lead

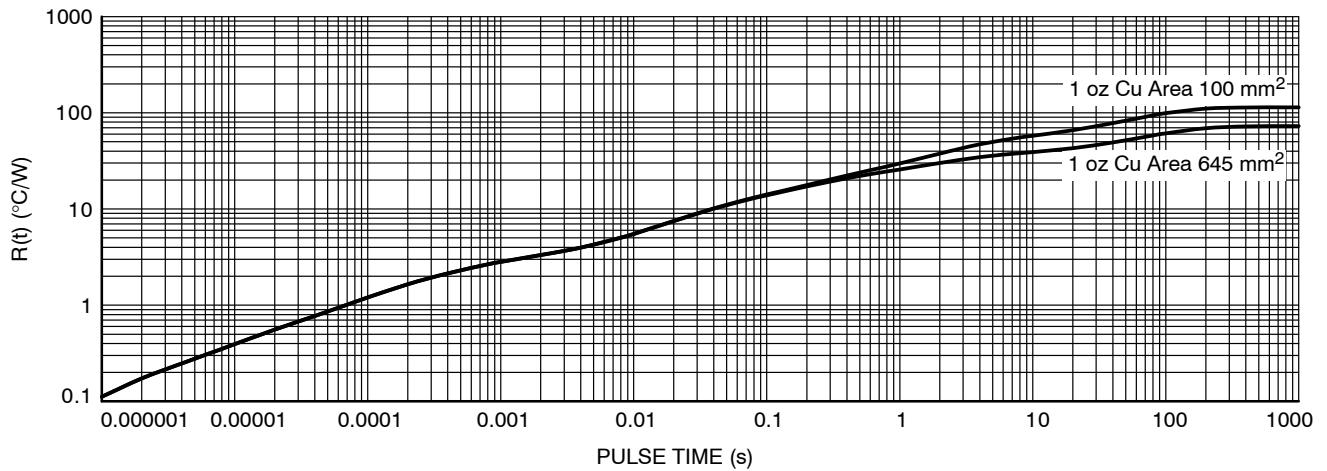


Figure 26. Single-Pulse Heating Curves, SOT 223-Lead

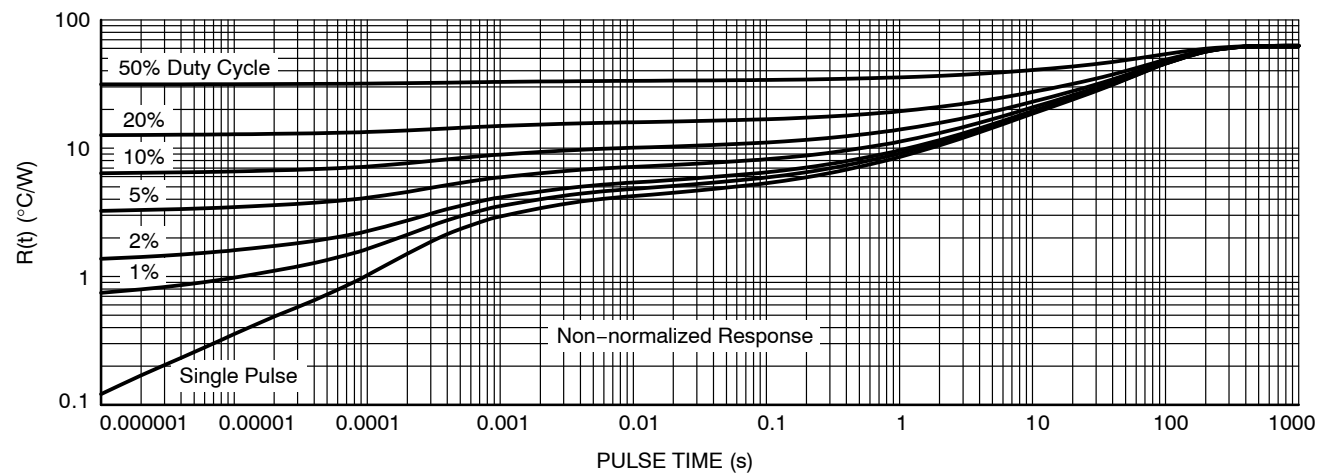


Figure 27. Duty Cycle for 1 inch² (645 mm²) Spreader Board, DPAK 3-Lead

NCV4274C

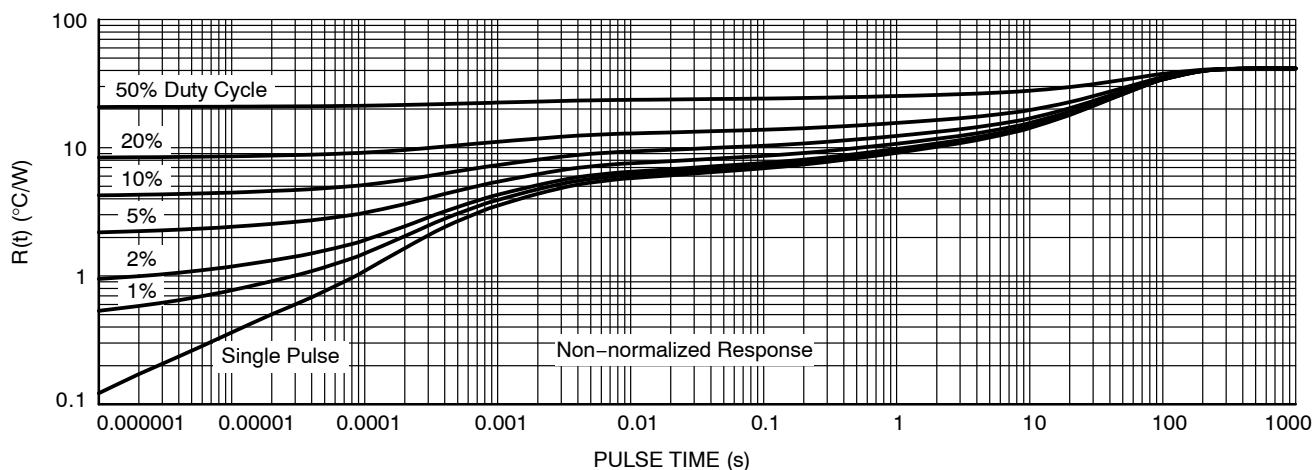


Figure 28. Duty Cycle for 1 inch² (645 mm²) Spreader Board, D²PAK 3-Lead

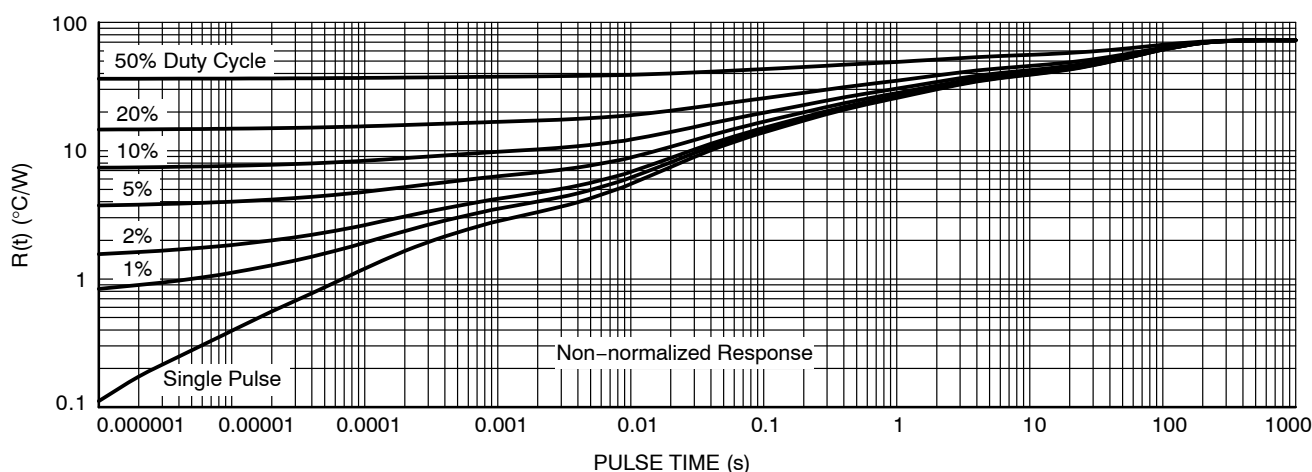


Figure 29. Duty Cycle for 1 inch² (645 mm²) Spreader Board, SOT 223-Lead

ORDERING INFORMATION

| Device* | Output Voltage Accuracy | Output Voltage | Package | Shipping† |
|-----------------|-------------------------|----------------|-------------------|--------------------|
| NCV4274CDT33RKG | 2% | 3.3 V | DPAK (Pb-Free) | 2500 / Tape & Reel |
| NCV4274CDT50RKG | 2% | 5.0 V | DPAK (Pb-Free) | 2500 / Tape & Reel |
| NCV4274CST33T3G | 2% | 3.3 V | SOT-223 (Pb-Free) | 4000 / Tape & Reel |
| NCV4274CST50T3G | 2% | 5.0 V | SOT-223 (Pb-Free) | 4000 / Tape & Reel |

DISCONTINUED (Note 5)

| | | | | |
|-----------------|----|-------|-----------------|-------------------|
| NCV4274CDS33R4G | 2% | 3.3 V | D2PAK (Pb-Free) | 800 / Tape & Reel |
| NCV4274CDS50R4G | 2% | 5.0 V | D2PAK (Pb-Free) | 800 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

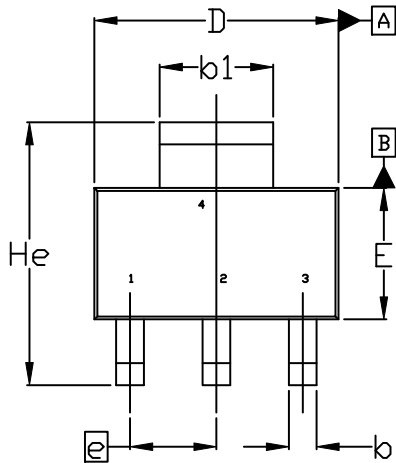
5. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.



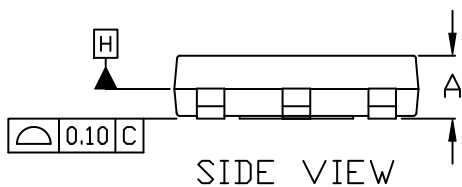
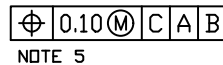
SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

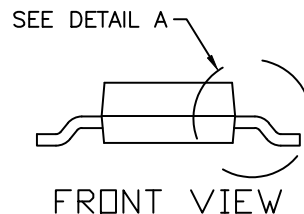
DATE 02 OCT 2018



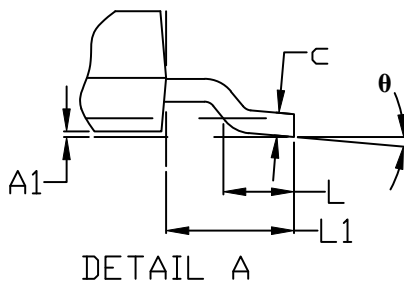
TOP VIEW



SIDE VIEW



FRONT VIEW

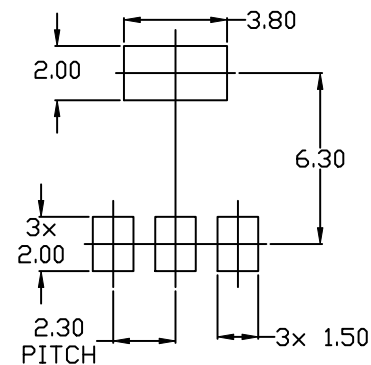


DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

| MILLIMETERS | | | |
|-------------|----------|------|------|
| DIM | MIN. | NOM. | MAX. |
| A | 1.50 | 1.63 | 1.75 |
| A1 | 0.02 | 0.06 | 0.10 |
| b | 0.60 | 0.75 | 0.89 |
| b1 | 2.90 | 3.06 | 3.20 |
| c | 0.24 | 0.29 | 0.35 |
| D | 6.30 | 6.50 | 6.70 |
| E | 3.30 | 3.50 | 3.70 |
| e | 2.30 BSC | | |
| L | 0.20 | --- | --- |
| L1 | 1.50 | 1.75 | 2.00 |
| He | 6.70 | 7.00 | 7.30 |
| θ | 0° | --- | 10° |



RECOMMENDED MOUNTING
FOOTPRINT

| | | |
|------------------|------------------|---|
| DOCUMENT NUMBER: | 98ASB42680B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOT-223 (TO-261) | PAGE 1 OF 2 |

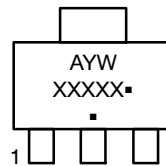
onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

| | | | | |
|--|---|---|---|---|
| STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR | STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE | STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN | STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN | STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE |
| STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT | STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE | STYLE 8: CANCELLED | STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND | STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE |
| STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2 | STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT | STYLE 13: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR | | |

**GENERIC
MARKING DIAGRAM***

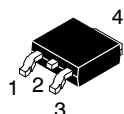


A = Assembly Location
 Y = Year
 W = Work Week
 XXXXX = Specific Device Code
 ■ = Pb-Free Package

(Note: Microdot may be in either location)
 *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|-------------------------|-------------------------|---|
| DOCUMENT NUMBER: | 98ASB42680B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | SOT-223 (TO-261) | PAGE 2 OF 2 |

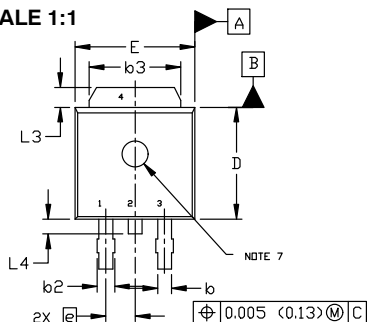
onsemi and **Onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.



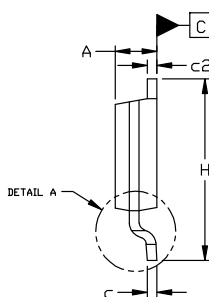
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE G

DATE 31 MAY 2023

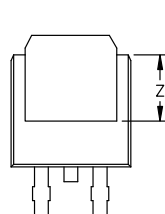
SCALE 1:1



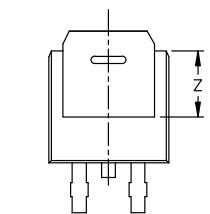
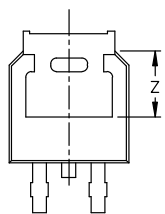
TOP VIEW



SIDE VIEW

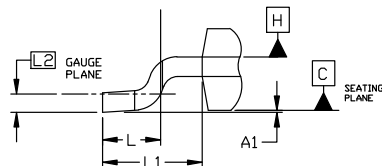
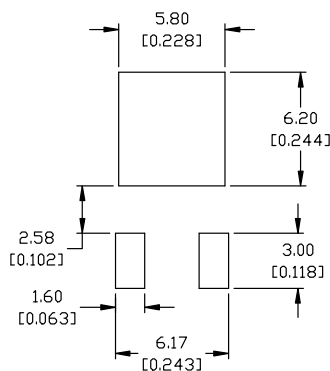


BOTTOM VIEW



BOTTOM VIEW

ALTERNATE
CONSTRUCTIONS



DETAIL A
ROTATED 90° CW

NOTES:

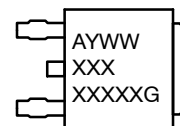
1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-------|-------------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.028 | 0.045 | 0.72 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 | BSC | 2.29 | BSC |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.114 | REF | 2.90 | REF |
| L2 | 0.020 | BSC | 0.51 | BSC |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | ---- | 0.040 | --- | 1.01 |
| Z | 0.155 | ---- | 3.93 | --- |

GENERIC
MARKING DIAGRAM*



IC



Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

RECOMMENDED MOUNTING FOOTPRINT*

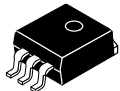
*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

| | | | | |
|---|---|--|--|---|
| STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR | STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN | STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE | STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE | STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE |
| STYLE 6: PIN 1. MT1 2. MT2 3. GATE 4. MT2 | STYLE 7: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR | STYLE 8: PIN 1. N/C 2. CATHODE 3. ANODE 4. CATHODE | STYLE 9: PIN 1. ANODE 2. CATHODE 3. RESISTOR ADJUST 4. CATHODE | STYLE 10: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. ANODE |

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|------------------|---------------------|--|
| DOCUMENT NUMBER: | 98AON10527D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | DPAK (SINGLE GAUGE) | PAGE 1 OF 1 |

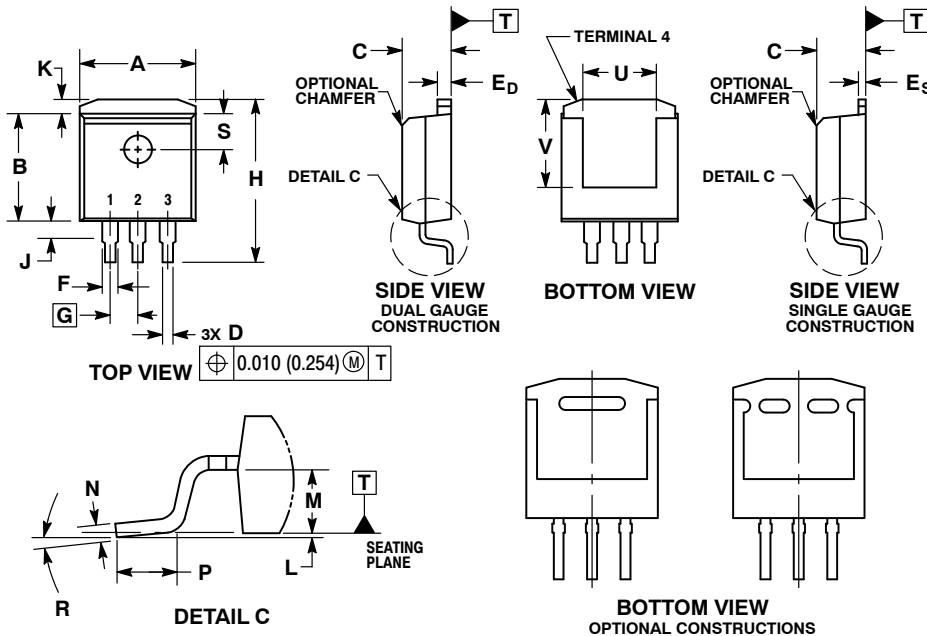
onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



SCALE 1:1

D2PAK
CASE 418AF
ISSUE E

DATE 15 SEP 2015

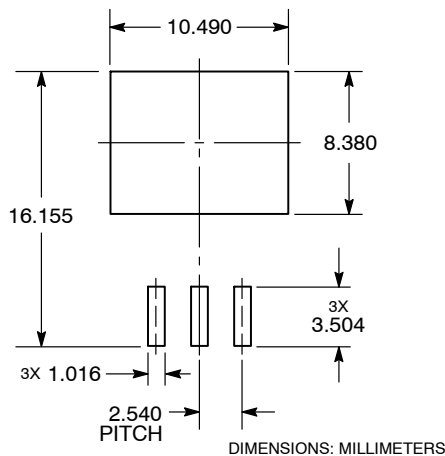


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.
6. SINGLE GAUGE DESIGN WILL BE SHIPPED AFTER FPCN EXPIRATION IN OCTOBER 2011.

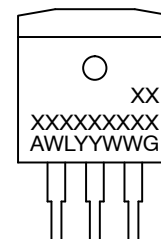
| DIM | INCHES | | MILLIMETERS | |
|----------------|-----------|-------|-------------|--------|
| | MIN | MAX | MIN | MAX |
| A | 0.386 | 0.403 | 9.804 | 10.236 |
| B | 0.356 | 0.368 | 9.042 | 9.347 |
| C | 0.170 | 0.180 | 4.318 | 4.572 |
| D | 0.026 | 0.036 | 0.660 | 0.914 |
| E _D | 0.045 | 0.055 | 1.143 | 1.397 |
| E _S | 0.018 | 0.026 | 0.457 | 0.660 |
| F | 0.051 REF | | 1.295 REF | |
| G | 0.100 BSC | | 2.540 BSC | |
| H | 0.539 | 0.579 | 13.691 | 14.707 |
| J | 0.125 MAX | | 3.175 MAX | |
| K | 0.050 REF | | 1.270 REF | |
| L | 0.000 | 0.010 | 0.000 | 0.254 |
| M | 0.088 | 0.102 | 2.235 | 2.591 |
| N | 0.018 | 0.026 | 0.457 | 0.660 |
| P | 0.058 | 0.078 | 1.473 | 1.981 |
| R | 0° | 8° | 0° | 8° |
| S | 0.116 REF | | 2.946 REF | |
| U | 0.200 MIN | | 5.080 MIN | |
| V | 0.250 MIN | | 6.350 MIN | |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

| | | |
|------------------|-------------|---|
| DOCUMENT NUMBER: | 98AON21981D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | D2PAK | PAGE 1 OF 1 |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales