NCV8871

Small-Signal PSPICE Model

The NCV8871xx-SMS model is a small-signal implementation of the NCV8871xx non-synchronous SEPIC/Boost controller (for product options xx = 00, 01, 02, 03 and 04) intended for AC analysis (cannot be used for large-signal transient analysis). The model is intended for feedback loop stability analysis of an NCV8871 controller using a Boost, Flyback or SEPIC topology.

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The example PSPICE file demonstrates the model implementation used for the NCV887100SEPGEVB discrete inductor SEPIC evaluation demo board (Fig. 1). Example files for Boost and coupled-inductor SEPIC converters are also included.
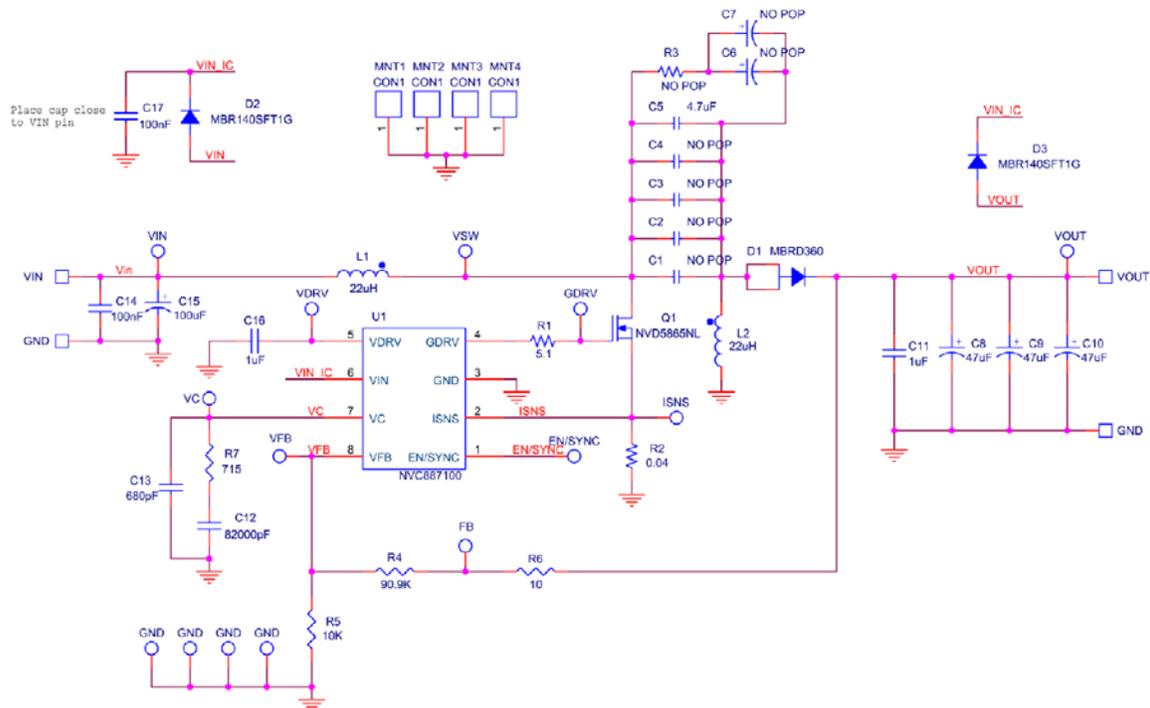
Figure 1 NCV887100SEPGEVB Evaluation Board Schematic

Modeled Elements

This NCV8871xx-SMS.LIB model is a modification of the public domain current-mode lossy switch PWMCM_L.LIB model created by Christophe Basso [1]. The corresponding NCV8871xx-SMS.OLB symbol representation is shown in Figure 2.

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Implementation = NCV8871xx-SMS
FS = 340kHz
RI = 100m
L = 10u
U?
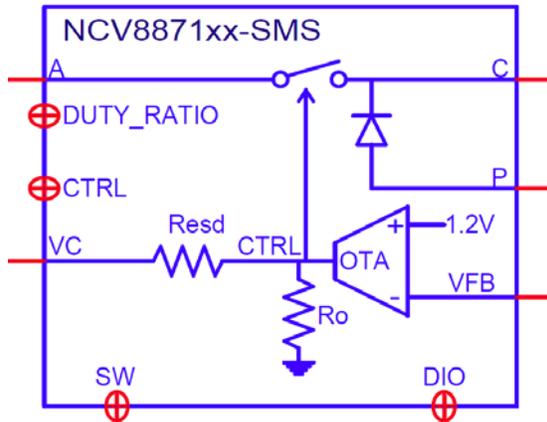
Figure 2 NCV8871xx Library Symbol

The following elements have been added to the PWMCM_L.LIB model to create the NCV8871-SMS.LIB small-signal mode.

- The op amp characteristics

- IC specific controller slope compensation

- IC specific duty cycle limitation

- All NCV8871 ordering options (replace 'xx' by either '00', '01', '02', '03' or '04' ordering options).

A stability analysis of the SEPIC converter design may be performed by passing the following parameters to the NCV8871-SMS model:

- SW: operating losses from the series combination of MOSFET rDS(ON) and current sense resistor (Ω)

- DIO – Connect the boost diode model for diode loss contribution. Anode to DIO and cathode to GND.

- L – Equivalent boost inductor (parallel value of L1//L2 for the discrete inductor SEPIC topology, L1 for the coupled-inductor SEPIC and boost topologies) (H)

- RI – Current sense resistor (value must be negative for boost topology) (Ω)

Modeling Example

A PSPICE small-signal analysis implementation of the NCV887100SEPGEVB demo board is shown in Fig. 3. Simulation results are shown in Fig. 4. Node definitions are provided in Table 1. The NCV8871 feedback amplifier is an operational transconductance amplifier (OTA). A 542 Ω resistor between the OTA output and the IC-VC compensation pin is implemented in silicon for ESD protection. To permit an accurate OTA gain analysis when selecting compensation feedback components, the internal OTA output node ("CTRL") is made available and strictly intended for analysis.
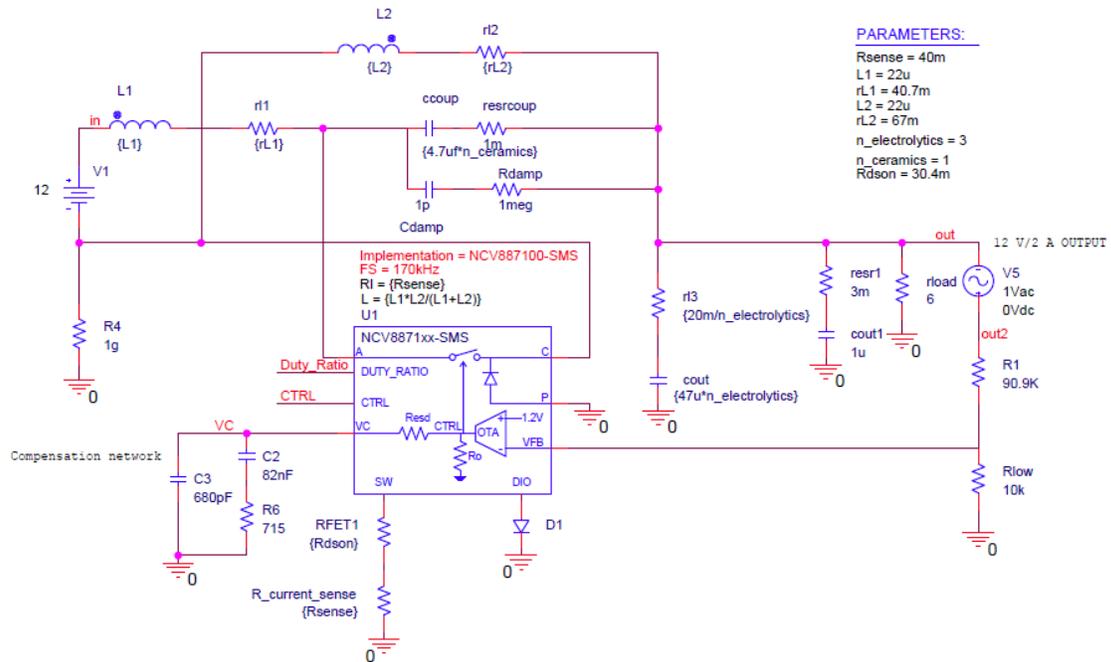
SMALL SIGNAL SIMULATION FOR THE DISCRETE INDUCTOR SEPIC
NCV887100SEPGEVB DEMO BOARD

Duty_Ratio, CTRL, VFB are NCV8871 internal nodes for feedback loop analysis. This is a lossy small-signal model adapted from Chris Basso's published PWMCM_L lossy PWM switch model. DIO introduces losses from the boost diode. MOSFET rDS(on) and current sense resistor (Rsense) losses are included.

Figure 3 NCV887100SEPGEVB Evaluation Board Small-Signal Simulation
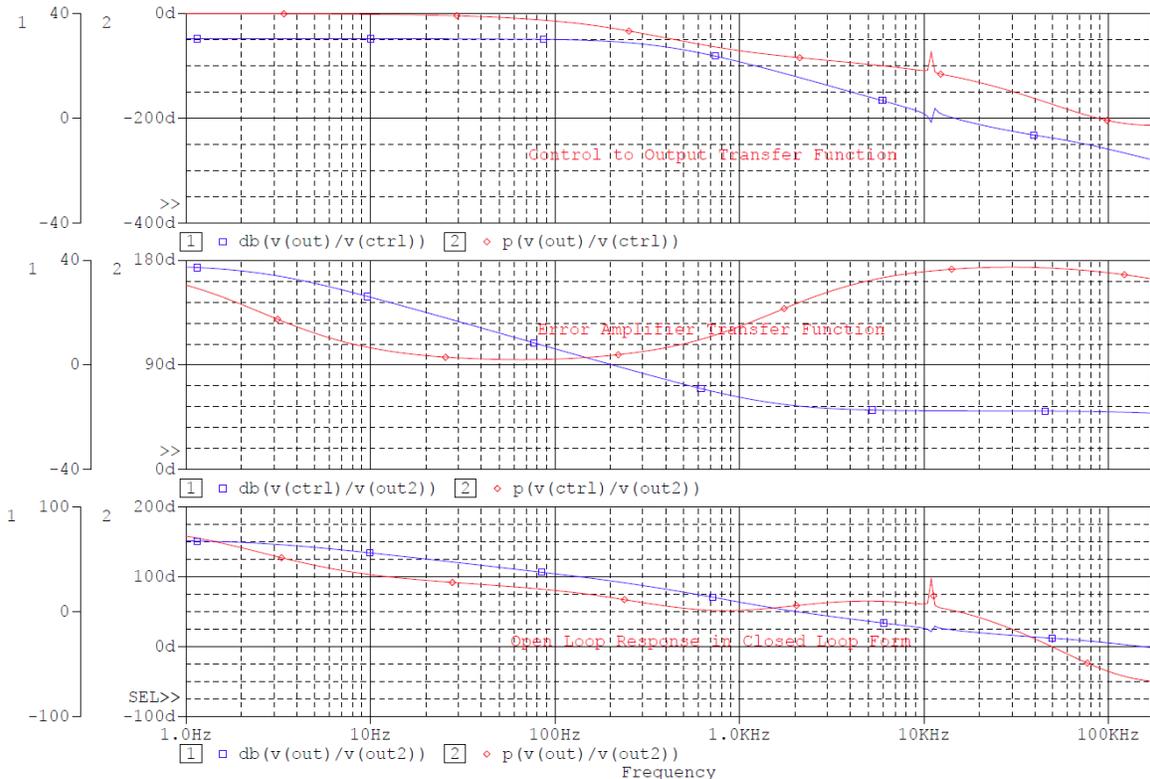
Figure 4 NCV887100SEPGEVB Evaluation Board Small-Signal Simulation Feedback Loop Response

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An ESD protection resistor is present between the OTA output and the VC package pin on the die (this is not documented in the datasheet). A virtual output (CTRL) is provided to access the controller's internal feedback node to permit a more accurate analysis for instances where the compensation resistor approaches the value of Resd (set to 542Ω within the model).

Table 1 NCV8871xx Model – Node Definitions

Parameter	Monitoring Purposes Only?	Unit	Range	Comment
A	No	V		Active Node (ref 1)
C	No	V		Common Node (ref 1)
P	No	V		Passive Node (ref 1)
CTRL	Yes	V	N/A	INTERNAL NODE FOR SIMULATION ANALYSIS
Duty_Ratio	Yes	V	0-D_{max} (see datasheet)	INTERNAL NODE FOR SIMULATION ANALYSIS
VC	No	V	N/A	IC Compensation Pin
VFB	No	V	V_{ref} = 1.2 V	Voltage feedback node
DIO	No	-	Boost Diode Loss	Connection point of boost diode's anode, only used for a more accurate duty ratio calculation in the simulation. Cathode MUST be connected to ground.
SW	No	-	rDS(on) and current sense losses	Connection point to include the influence of rDS(on) and current sense resistor losses, only used for a more accurate duty ratio calculation in the simulation.

Table 2 NCV8871xx Model – Parameters Table Definition

Parameter	Unit	Comment
RI	Ω	Current Sense Resistor
L	H	Boost Inductor

Feedback Loop Analysis Methodology

Simulations should be run at worst case parameter conditions (e.g.: Minimum input voltage, worst case output capacitor parasitic ESR values, etc). Additional simulations under less stringent conditions (e.g. nominal ESR, different input voltage conditions) are recommended as well for verification. The disturbance injection point is introduced by inserting and AC source between nodes OUT and OUT2.

1- Control-Output (Modulator Plot) Response

This is the response of the power supply as seen by the IC's internal CTRL node (V(OUT)/V(CTRL)). This information is required to select OTA compensation components (R6, C2, C3).

2- OTA Compensation

From the modulator plot data, the OTA compensation network is determined (V(CTRL)/V(OUT2)) by selecting the desired zero gain and frequency values (R6/C2) and pole frequency (C3). CTRL is the OTA output (before Resd) and is a node internal to the IC and is strictly intended for analysis.

3- Loop Response (Open-Loop Response in Closed-Loop Form)

The power supply feedback loop response is obtained by plotting V(OUT/V(OUT2). The resulting design cross-over frequency, phase-margin and gain-margin are now obtained.

References

[1] C. Basso, "Switch-Mode Power Supplies – SPICE Simulations and Practical Designs", McGraw Hill, 2008.

[2] NCV8871: Non-Synchronous Boost Controller datasheet:
http://onsemi.com/PowerSolutions/product.do?id=NCV8871

 [3] NCV8871: Automotive Grade High-Frequency SEPIC Controller Evaluation Board User's Manual:
http://www.onsemi.com/pub_link/Collateral/EVBUM2080-D.PDF

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