

# NCV8878

## Small-Signal PSPICE Model

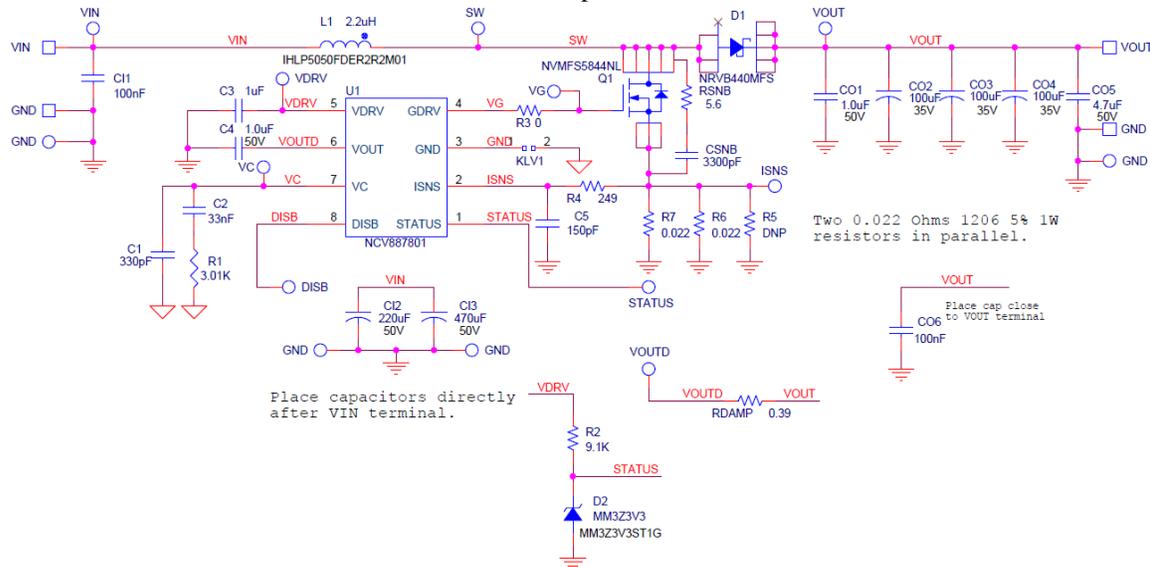
The NCV8878-SMS\_revX.ZIP is a PSPICE small-signal implementation of the NCV8878 Start-Stop boost controller (NCV887801) for AC small-signal feedback loop analysis (cannot be used for large-signal transient analysis).

The example PSPICE files demonstrate a modeling implementation for the NCV887801BSTGEVB (Fig. 1) evaluation demo board. This note will describe the NCV887801BSTGEVB evaluation board simulation implementation.



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**Figure 1 NCV887801BSTGEVB Evaluation Board Schematic**

### Modeled Elements

This model incorporates a discrete element implementation of the public domain current-mode lossy switch PWMCM\_LX.LIB model created by Christophe Basso [1]. The current mode lossy model configuration is shown in Figure 2.

The following elements are user defined:

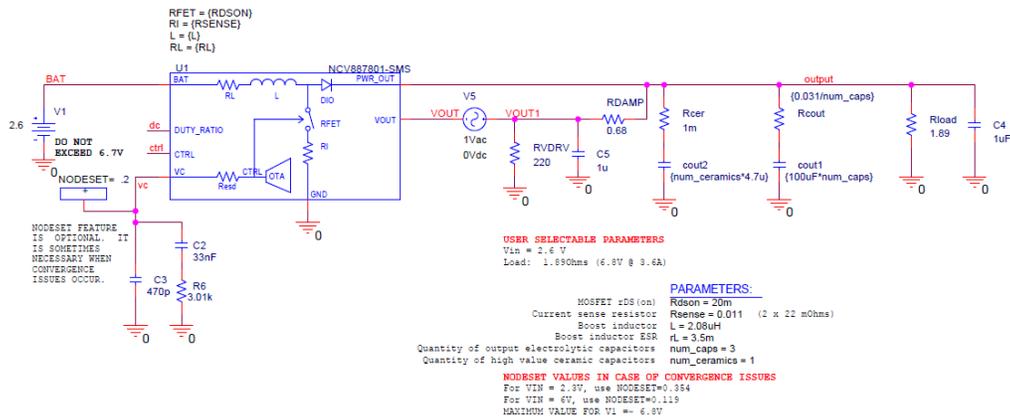
- Boost inductor value
- Inductor ESR
- Boost MOSFET transistor RDS(ON)
- Current sense resistor
- The op amp characteristics and internal feedback voltage divider.
- IC-VOUT input terminal (Note VDRV load must be added externally. Refer to RDRV location in the simulation schematic)
- IC specific controller slope compensation

A stability analysis of the boost converter design is performed by injecting an AC source between the power supply output (Figure 2 node labelled as *VOUT1*) and node *VOUT*.

This model is valid for both CCM and DCM operating modes. The discontinuous mode off-time term referenced as  $D2$  in literature [1] is generated within the IC modeling block.

### Modeling Example

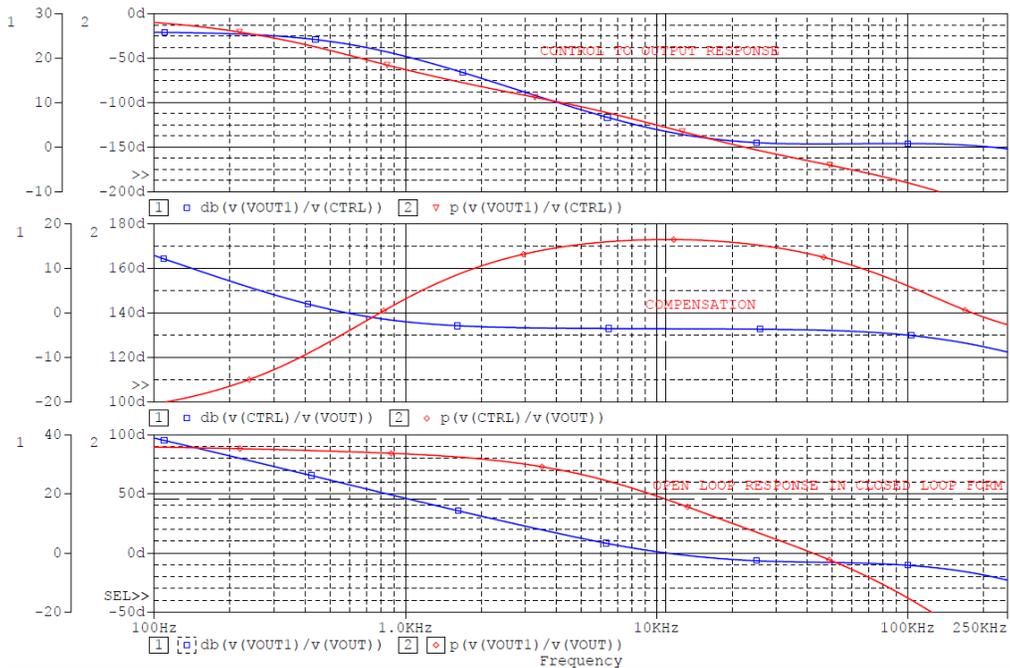
A PSPICE small-signal analysis implementation of the NCV887801BSTGEVB demo board is shown in Fig. 2. Simulation results are shown in Fig. 3. Node definitions are provided in Table 1. The NCV887801 feedback amplifier is an operational transconductance amplifier (OTA). A  $542\ \Omega$  resistor between the OTA output and the IC-VC compensation pin is implemented in silicon for ESD protection. To permit an accurate OTA gain analysis when selecting compensation feedback components, the internal OTA output node (“CTRL”) is made available and strictly intended for analysis.



SMALL SIGNAL SIMULATION FOR THE NCV887801BSTGEVB DEMO BOARD

Duty Ratio, CTRL are NCV887801 internal nodes for feedback loop analysis. This is a lossy small-signal model adapted from Chris Basso's published PFMCM\_LX lossy PWM switch model. DIO introduces losses from the current boost diode. MOSFET rDS(on) and current

**Figure 2 NCV887801BSTGEVB Evaluation Board Small-Signal Simulation Schematic**



**Figure 3 NCV887801BSTGEVB Evaluation Board Small-Signal Feedback Loop Response**

The IC-VOUT pin serves a dual function:

- (1) Feedback control
- (2) IC-power source.

As a result of this dual function, the actual PCB physical IC-VOUT node may not be used to perform lab feedback loop measurements. The feedback loop may only be analyzed by simulation and verified in a lab environment by input line and output transient tests.

**Table 1 NCV887801 Model – Node Definitions**

Parameter	Monitoring Purposes Only?	Unit	Range	Comment
BAT	No	V	< 6.7 V	Power Supply Input Voltage
DC	Yes	N/A	0 – 0.83	Duty cycle information. INTERNAL NODE FOR SIMULATION ANALYSIS
CTRL	Yes	V	N/A	INTERNAL NODE FOR SIMULATION ANALYSIS
VC	No	V	N/A	IC Compensation Pin
OUTPUT	No	V	Fixed 6.8 V	IC Specific Fixed Regulation Output Voltage
VOUT	No	V	Fixed 6.8 V	IC Feedback Input Voltage
GND	No	V	0 V	Connect to Schematic Ground Reference

**Table 2 NCV887801 Model – Parameters Table Definition**

Parameter	Unit	Comment
Rdson	$\Omega$	MOSFET RDS(ON) (Default Value = 25 m $\Omega$ )
Rsense	$\Omega$	Current Sense Resistor (Default Value = 10 m $\Omega$ )
L	H	Boost Inductor (Default Value = 10 $\mu$ H)
rL	$\Omega$	Boost Inductor ESR (Default Value = 3 m $\Omega$ )

### Feedback Loop Analysis Methodology

Simulations should be run at worst case parameter conditions (e.g.: Minimum input voltage, worst case output capacitor parasitic ESR values, etc). Additional simulations under less stringent conditions (e.g. nominal ESR, different input voltage conditions) are recommended as well for verification.

#### 1- Control-Output (Modulator Plot) Response

This is the response of the power supply as seen by the IC’s internal CTRL node ( $V(VOUT1)/V(CTRL)$ ). This information is required to select OTA compensation components (R6, C2, C3).

#### 2- OTA Compensation

From the modulator plot data, the OTA compensation network is determined ( $V(CTRL)/V(VOUT)$ ) by selecting the desired zero gain and frequency values ( $R6/C2$ ) and pole frequency (C3). CTRL is the OTA output (before Resd) and is a node internal to the IC and is strictly intended for analysis.

#### 3- Loop Response (Open-Loop Response in Closed-Loop Form)

The power supply feedback loop response is obtained by plotting  $V(OUT1)/V(VOUT)$ . The resulting design cross-over frequency, phase-margin and gain-margin are now obtained.

## References

[1] C. Basso, “Switch-Mode Power Supplies – SPICE Simulations and Practical Designs”, McGraw Hill, 2008.

[2] NCV8878: Automotive Grade Start-Stop Non-Synchronous Boost Controller datasheet:  
<http://onsemi.com/PowerSolutions/product.do?id=NCV8878>

[3] NCV887801: Automotive Start Stop Grade Boost Controller Evaluation Board:  
<http://onsemi.com/PowerSolutions/evalBoard.do?id=NCV887801BSTGEVB>