Electronic Fuse, +3.3/+5 Volt

NIS6432, NIS6452

The NIS64x2 is a cost effective, resettable fuse which can greatly enhance the reliability of a hard drive or other circuit from both catastrophic and shutdown failures.

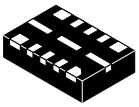
It is designed to buffer the load device from excessive input voltage which can damage sensitive circuits and to protect the input side circuitry from reverse currents. It includes an overvoltage clamp circuit that limits the output voltage during transients but does not shut the unit down, thereby allowing the load circuit to continue its operation.

Features

- 42 mΩ Typical
- Digital and Tristate Enable
- Integrated Reverse Current Protection
- Thermally Protected
- Integrated Soft−Start Circuit
- Fast Response Overvoltage Clamp Circuit
- Internal Undervoltage Lockout Circuit
- Internal Charge Pump
- Load Current Monitor Pin
- ESD Ratings: Human Body Model (HBM); 2000 V
  Charged Device Model (CDM); 2000 V
  Latch−Up; Class 1
- These Devices are Pb−Free and are RoHS Compliant

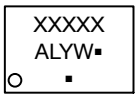
Typical Applications

- Hard Drives
- Solid State Drives
- Mother Boards



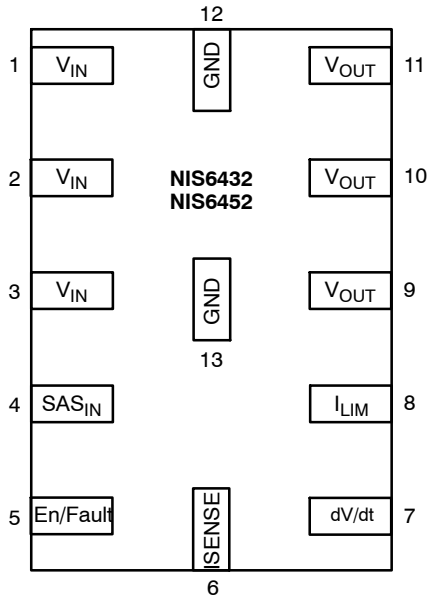
WQFN12
CASE 510BM

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

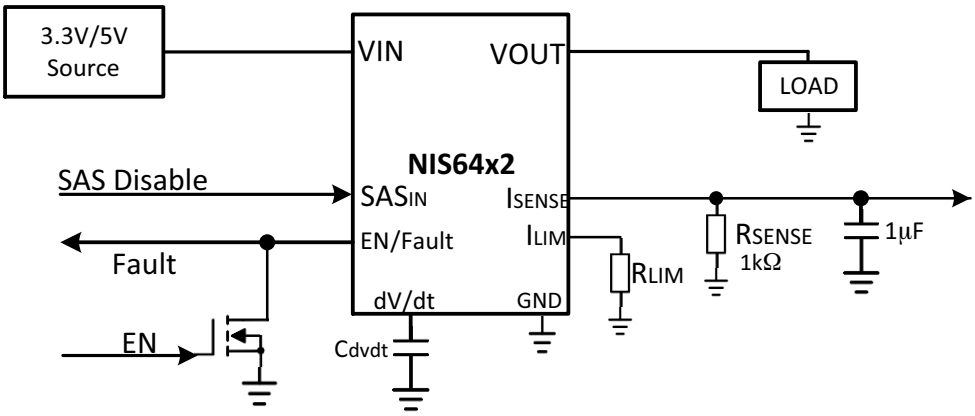


Figure 1. Typical Application Circuit

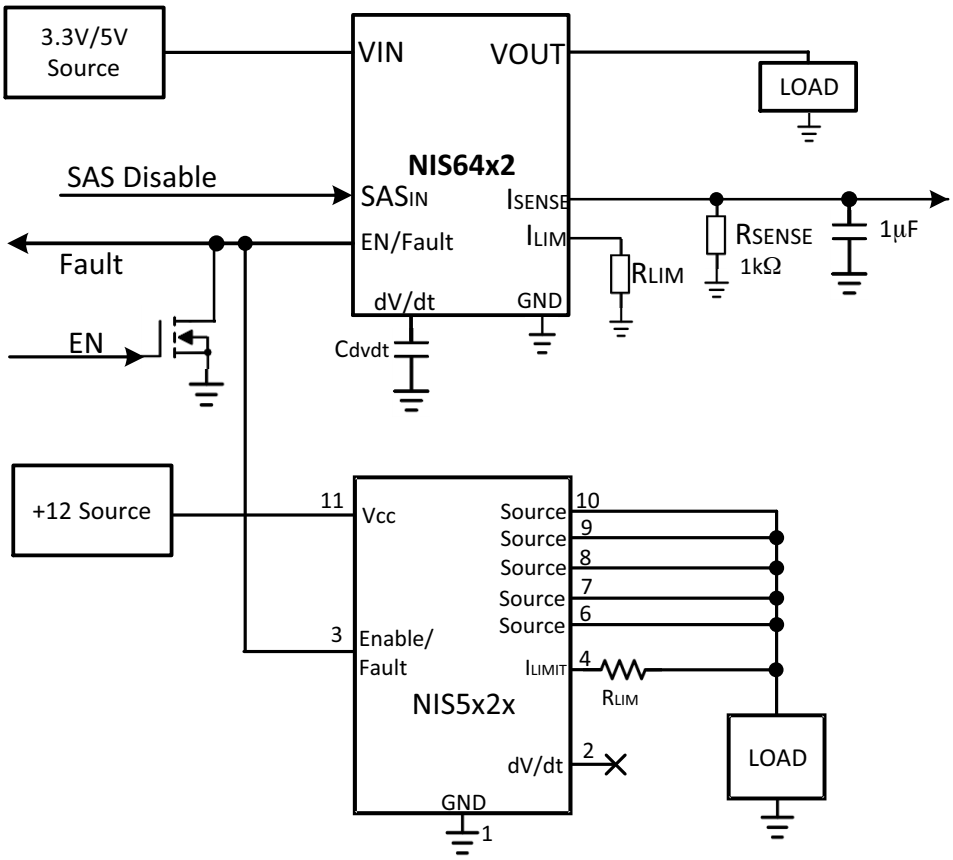


Figure 2. Common Thermal Shutdown with another eFuse

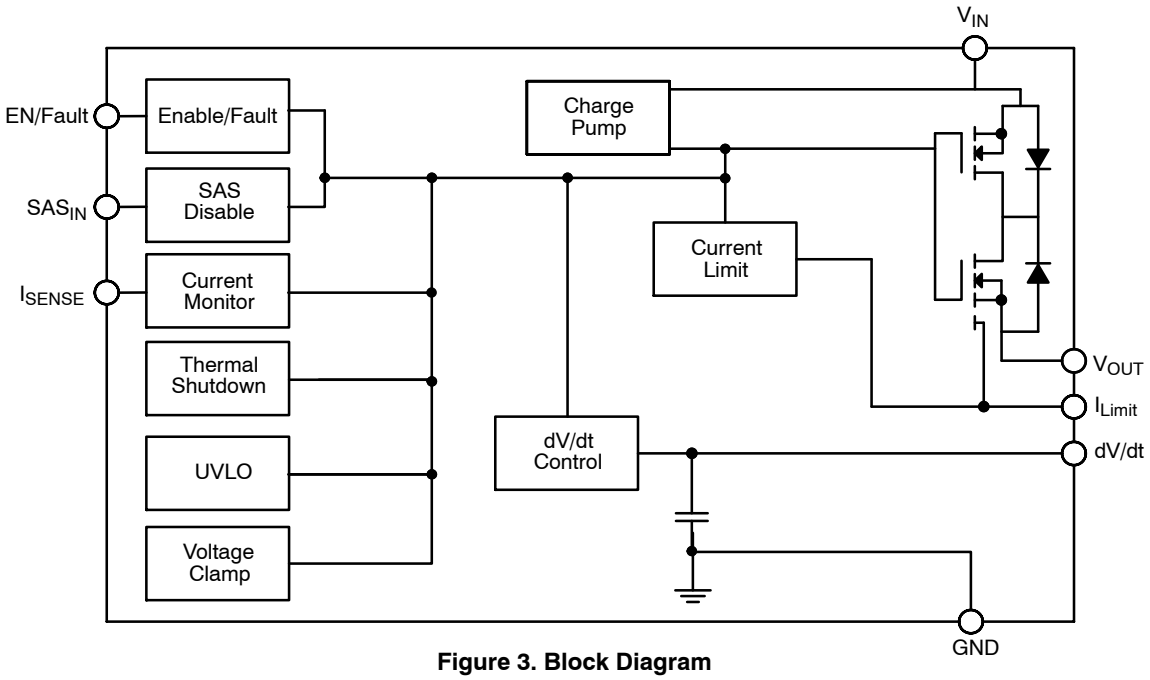


Figure 3. Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1,2,3	V_{IN}	Positive input voltage to the device.
4	SAS_{IN}	When this pin is pulled high the eFuse is turned off.
5	EN/Fault	This pin is a tri−state, bidirectional interface. It can be pulled to ground with an external open−drain or open collector device to shut down the eFuse. It can also be used as a status indicator; if the voltage level is intermediate (around 1.4 V), the eFuse is in thermal shutdown. If the voltage level is high (around 3 V) the eFuse is operating normally. Do not actively drive this pin to any voltage. Do not connect a capacitor to this pin.
6	I_{SENSE}	Current Sense Pin. Connect a 1 kΩ 1% resistor and a 1 μF capacitor to ground.
7	dV/dt	The internal dV/dt circuit controls the slew rate of the output voltage at turn on.
8	I_{LIM}	A resistor between this pin and ground pin sets the overload and short circuit current limit levels.
9,10,11	V_{OUT}	Source of the internal power FET and the output terminal of the fuse
12,13	GND	Negative input voltage to the device. This is used as the internal reference for the IC.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage, operating, steady−state (V_{IN} to GND) Transient (100 ms)	V_{IN}	−0.3 to +14 −0.3 to +15	V
Voltage range on EN/Fault pin		−0.3 to 6	V
Voltage range on SAS_{IN} pin		−0.3 to 6	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. THERMAL RATINGS

Thermal Resistance, Junction to Air (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu)	θ_{JA}	75	°C/W
Thermal Resistance, Junction−to−Lead (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu)	Ψ_{J-L}	12	°C/W
Thermal Resistance, Junction−to−Board (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu)	Ψ_{J-B}	12	°C/W
Thermal Resistance, Junction−to−Case Top (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu)	Ψ_{J-T}	5	°C/W
Total Power Dissipation @ T_A = 25°C (4 layer High−K JEDEC JESD51−7 PCB, 100 mm^2, 2 oz. Cu) Derate above 25°C	P_{max}	1.67 13.4	W mW/°C
Operating Ambient Temperature Range	T_A	−40 to 125	°C
Operating Junction Temperature Range	T_J	−40 to 150	°C
Non−operating Storage Temperature Range	T_{STG}	−55 to 155	°C
Lead Temperature, Soldering (10 Sec)	T_L	260	°C

Table 4. ELECTRICAL CHARACTERISTICS
(Unless otherwise noted: V_{IN} = 5 V, dV/dt pin open, R_{LIM} = 10 kΩ, T_A = 25°C)

Characteristics	Symbol	Min	Typ	Max	Unit
POWER FET					
ON Resistance (Note 4) T_J = 140°C (Note 5)	$R_{DS(on)}$		42 62	60	mΩ
Continuous Current (Ta = 25°C, 0.5 sq in pad) (Note 4) (Ta = 80°C, minimum copper)	I_d		5 3.8		A
Off State Leakage (Vin = 5 V, EN = 0 V)	I_{leak}			1	μA
THERMAL LATCH					
Shutdown Temperature (Note 1)	T_{SD}	150	175	200	°C
UNDER/OVERVOLTAGE PROTECTION					
V_{OUT} Maximum (V_{CC} = 10 V) NIS6432 NIS6452	$V_{out-clamp}$	3.6 6.3	3.9 6.5	4.4 7.0	V
Undervoltage Lockout (Turn on, Voltage Going High)	V_{UVLO}	2.3		2.8	V
UVLO Hysteresis	V_{Hyst}		0.4		V
CURRENT LIMIT					
Overload Current Limit (overload/trigger), R_{LIM} = 10 kΩ	I_{OL}		4.3		A
Short Circuit Current Limit, R_{LIM} = 10 kΩ	I_{SC}	2.34	2.7	3.06	A
Current Limit Response Time	T_{ilim}	5.5		40	μs
LOAD CURRENT MONITORING					
Load Monitor Sense Current, R_{SENSE} = 1 kΩ	I_{SENSE}		1		mA/A
REVERSE CURRENT LIMIT					
Reverse Current Limit (Note 5)	$I_{REVERSE}$		1.2	1.78	A
Reverse Current Limit Response Time (dVin/dt = −5 V/1 ms, 20 μF Load)	$T_{IREVERSE}$	5		10	μs
SLEW RATE CONTROL					
Slew Rate (No dV/dt capacitor)	SR		1.0		ms
ENABLE/FAULT					
Output Logic Level Low (Output Disabled)	$EN_{(VOL)}$			0.8	V
Output Logic Level Mid (Thermal Fault, Output Disabled)	$EN_{(MID)}$	0.9	1.4	1.95	V
Output Logic Level High (Output Enabled)	$EN_{(VOH)}$	2.1			V
Logic Low Sink Current (Venable = 0 V)	$EN_{(ISink)}$		12	20.24	μA
Logic High Leakage Current for External Switch (Venable = 3.3 V)	$EN_{(ILeak)}$			1	μA
Maximum Fanout for Fault Signal (Total number of chips that can be connected to this pin for simultaneous shutdown)	$EN_{(Fanout)}$			3	Units
SAS DISABLE					
Logic Level Low (Output Enabled)	$SAS_{IN(VIL)}$	0.3			V
Logic Level High (Output Disabled)	$SAS_{IN(VIH)}$			1.2	V
De−glitch Filter Delay	SAS_{Tdly}	2		50	μs

Table 4. ELECTRICAL CHARACTERISTICS
(Unless otherwise noted: V_{IN} = 5 V, dV/dt pin open, R_{LIM} = 10 kΩ, T_A = 25°C)

Characteristics	Symbol	Min	Typ	Max	Unit
TOTAL DEVICE					
Bias Current	I_{Bias}				μA
Operational (I_{Load} = 0 A)			300		
Shutdown (EN = 0), (Note 2)			160		
Fault			100	120	
FAULT EVENTS					
		EN/Fault Level	V_{OUT} State	Latch	
Under Voltage Lock Out	UVLO	$EN_{(VOL)}$	off	no	
Thermal Shutdown	TSD	$EN_{(MID)}$	off	yes, (Note 1)	
Reverse Current Protection	Ireverse	$EN_{(MID)}$	off	no, (Note 5)	
No Fault (Vin > UVLO)		$EN_{(VOH)}$	on	N/A	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. eFuse is latched off until the En/Fault pin is pulled low and then released, the SAS Disable pin is pulled high and then released or a power on reset is applied to the device.
2. Does not include fan out of Enable/Fault function.
3. Pulse test: Pulse width 300 s, duty cycle 2%
4. Verified by design.
5. Once the device has entered shutdown mode due to a reverse current event, it will re−enable its output when $V_{IN} > V_{OUT}$ for at least 100 μs. The slew rate SR will be applied when the output is re−enabled.

TYPICAL CHARACTERISTICS

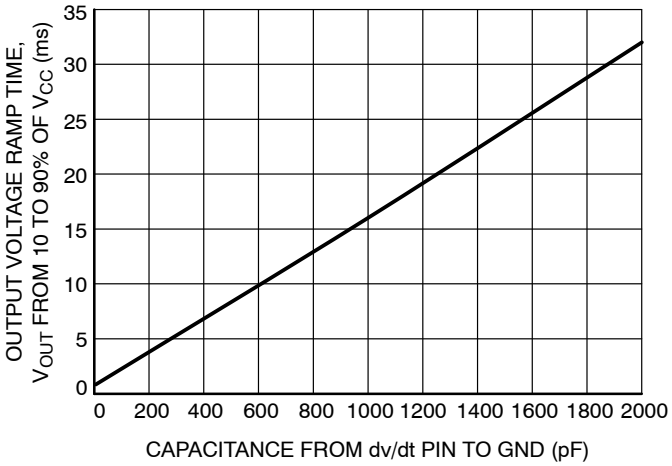


Figure 4. Slew Rate vs Cdvdt capacitance for 3.3V and 5V

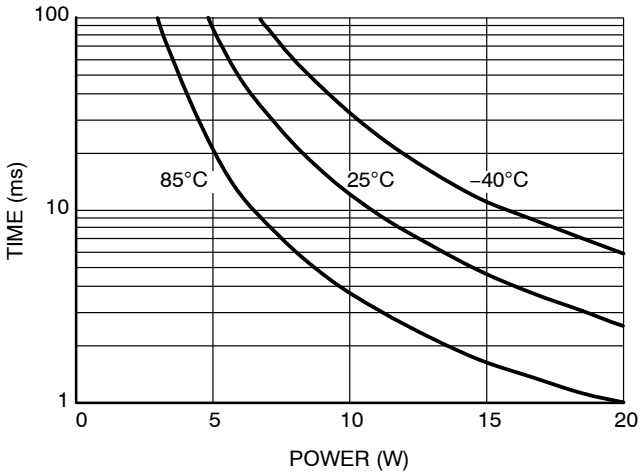


Figure 5. Thermal Trip Time vs Power Dissipation

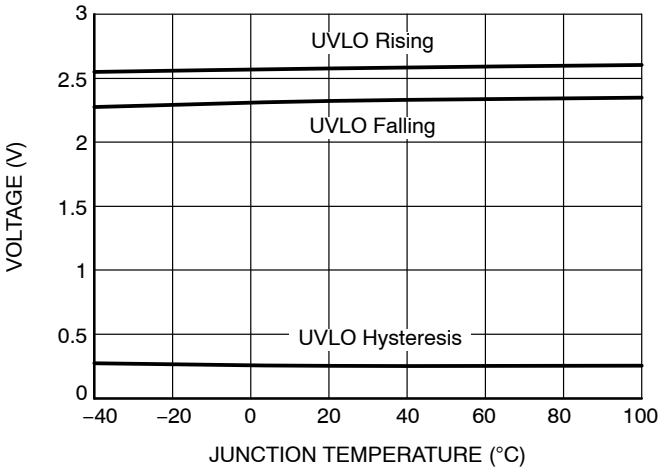


Figure 6. UVLO vs Junction Temperature

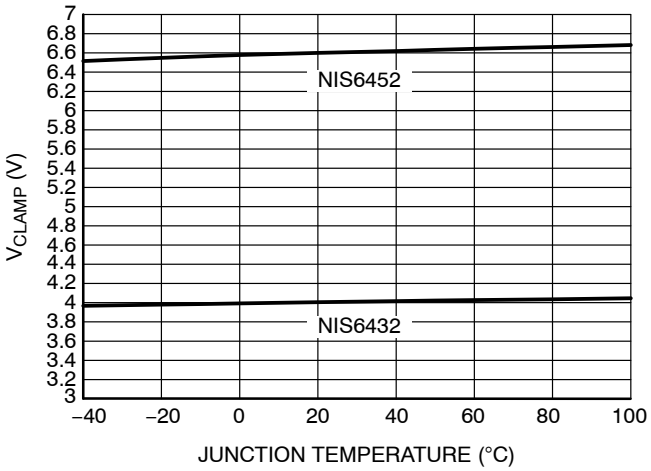


Figure 7. V_{clamp} vs Junction Temperature

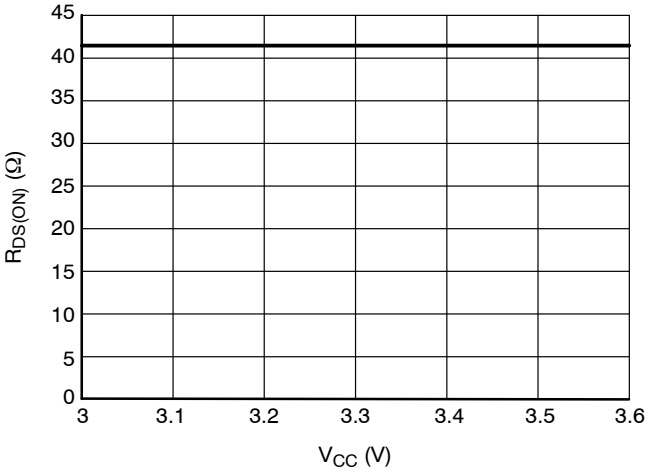


Figure 8. $R_{DS(on)}$ vs V_{CC} for NIS6432

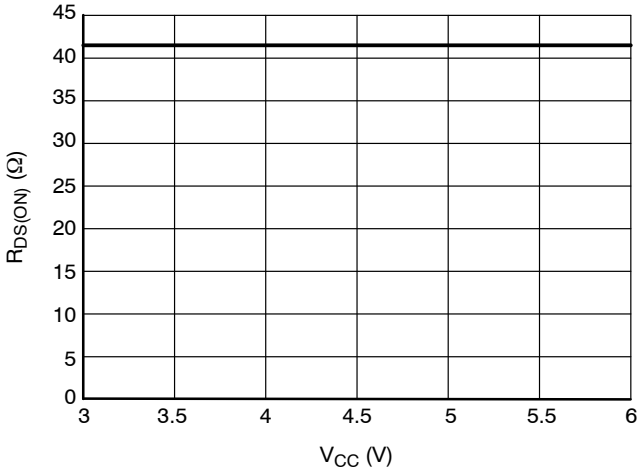


Figure 9. $R_{DS(on)}$ vs V_{CC} for NIS6452

TYPICAL CHARACTERISTICS

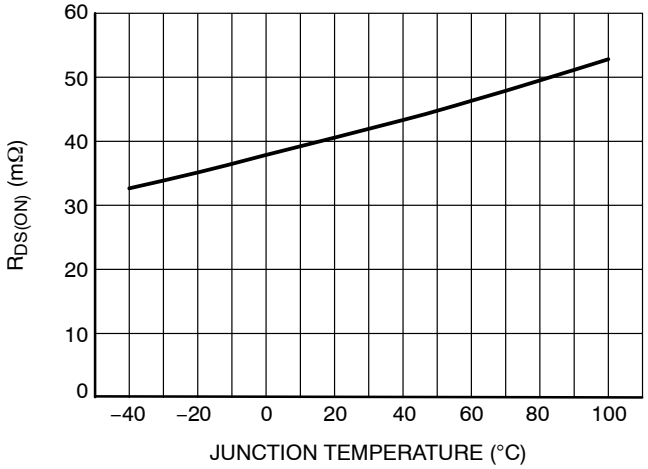


Figure 10. $R_{DS(on)}$ vs Junction Temperature

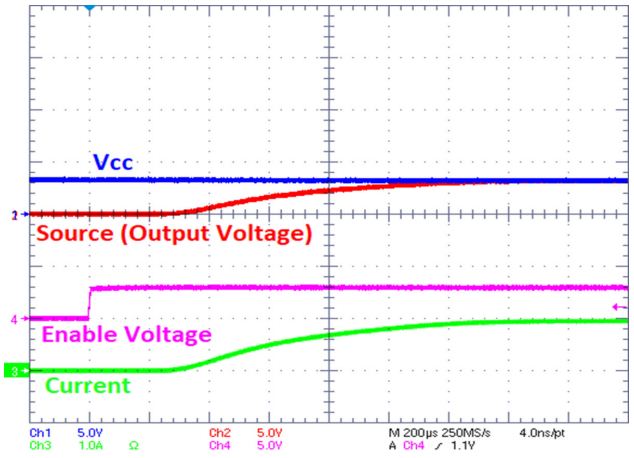


Figure 11. Slew Rate Control for NIS6432

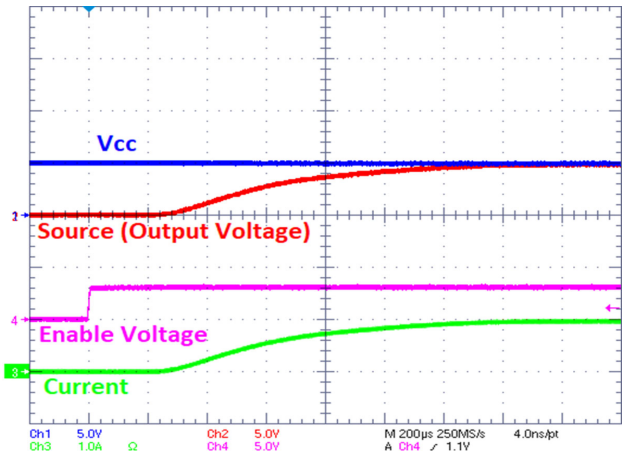


Figure 12. Slew Rate Control for NIS6452

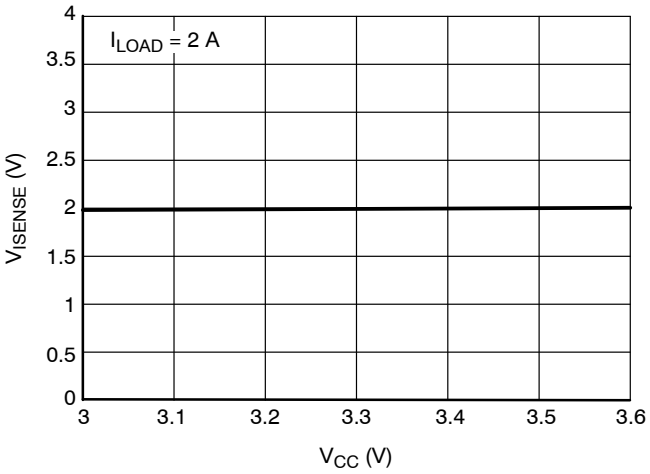


Figure 13. V_{ISENSE} vs V_{CC} for NIS6432

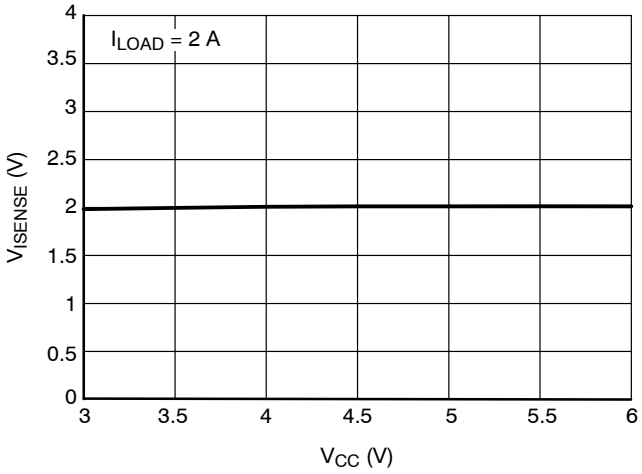


Figure 14. V_{ISENSE} vs V_{CC} for NIS6452

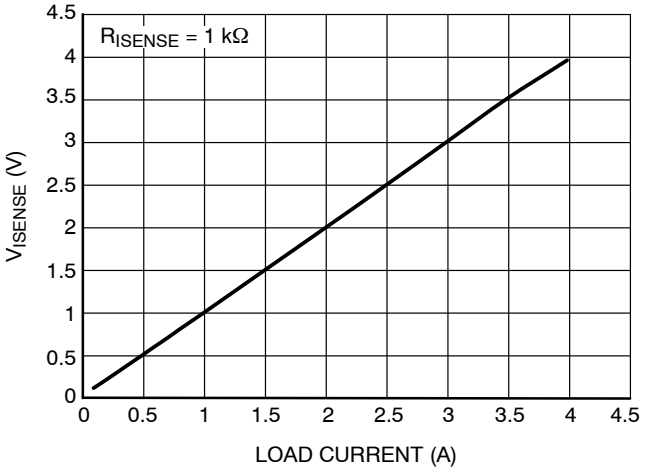


Figure 15. V_{ISENSE} vs Load Current

TYPICAL CHARACTERISTICS

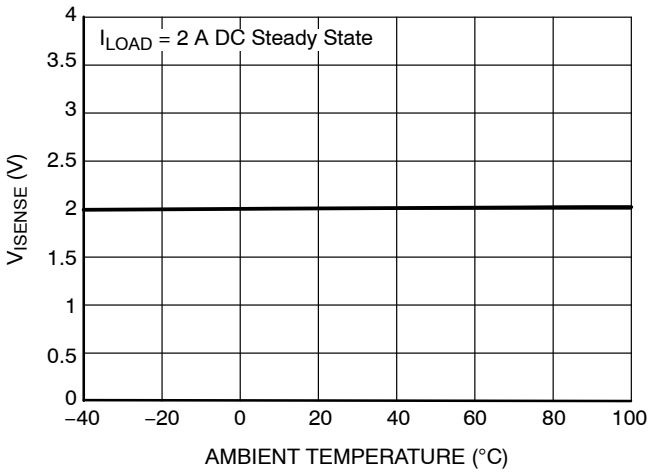


Figure 16. V_{ISENSE} vs Ambient Temperature

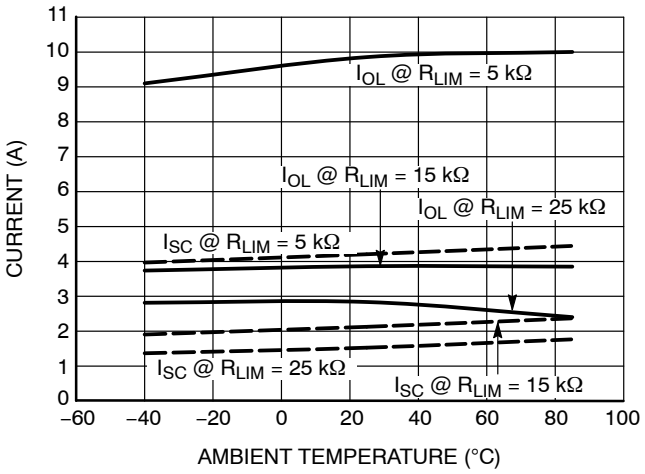


Figure 17. I_{LIM} vs R_{LIM} over Ambient Temperature

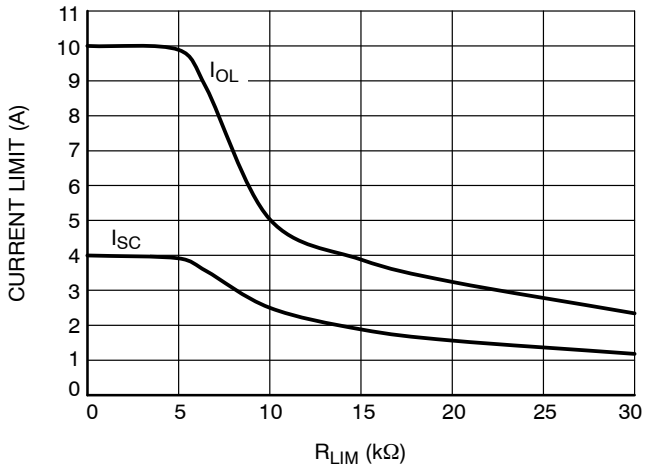


Figure 18. Overload and Short Circuit Current Limit vs R_{LIM}

APPLICATIONS INFORMATION

Basic Operation

This device is a self−protected, resettable, electronic fuse.

It contains circuits to monitor the input voltage, output voltage, output current and die temperature.

On application of the input voltage, the device will apply the input voltage to the load based on the restrictions of the controlling circuits. The output voltage, which is controlled by an internal dv/dt circuit, will slew from 0 V to the rated output voltage in 1.0 ms.

The device will remain on as long as the temperature does not exceed the 175°C limit that is programmed into the chip.

The internal current limit circuit does not shut down the part but will reduce the conductivity of the FET to maintain a constant current at the internally set current limit level. The input overvoltage clamp also does not shutdown the part, but will limit the output voltage in the event that the input exceeds the Vclamp level.

An internal charge pump provides bias for the gate voltage of the internal n−channel power FET and also for the current limit circuit. The remainder of the control circuitry operates between the input voltage (V_{CC}) and ground.

Overvoltage Clamp

The overvoltage clamp consists of an amplifier and reference. It monitors the output voltage and if the input voltage exceeds $V_{out-clamp}$, the gate drive of the main FET is reduced to limit the output. This is intended to allow operation through transients while protecting the load. If an overvoltage condition exists for many seconds, the device may overheat due to the voltage drop across the FET combined with the load current. In this event, the thermal protection circuit would shut down the device.

Enable/Fault

The Enable/Fault Pin is a multi−function, bidirectional pin that can control the output of the chip as well as send information to other devices regarding the state of the chip. When this pin is low, the output of the fuse will be turned off. When this pin is high the output of the fuse will be turned−on. If a thermal fault occurs, this pin will be pulled low to an intermediate level by an internal circuit. To use as a simple enable pin, an open drain or open collector device should be connected to this pin. Due to its tri−state operation, it should not be connected to any type of logic with an internal pull−up device.

If the chip shuts down due to the die temperature reaching its thermal limit, this pin will be pulled down to an intermediate level. This signal can be monitored by an external circuit to communicate that a thermal shutdown has occurred. If this pin is tied to another device in this family, a thermal shutdown of one device will cause both devices to disable their outputs. Both devices will turn on once the fault is removed for the auto−retry devices.

Since this is a latching thermal device, the outputs will be enabled after the enable pin has been pulled to ground with an external switch and then allowed to go high or after the input power has been recycled.

Thermal Protection

The NIS64x2 includes an internal temperature sensing circuit that senses the temperature on the die of the power FET. If the temperature reaches 175°C, the device will shut down, and remove power from the load. Output power can be restored by either recycling the input power or toggling the enable pin.

The thermal limit has been set high intentionally, to increase the trip time during high power transient events. It is not recommended to operate this device above 150°C for extended periods of time.

SAS Disable

The SAS Disable feature provides a digital interface to control the output of the eFuse. When the SAS_{IN} pin is pulled high by any external digital control circuitry the eFuse switches to its off state. When the SAS_{IN} pin is pulled low the eFuse output is turned on. All fault conditions will be cleared when the eFuse is reset through the SAS pin.

Reverse Current Protection

The NIS64x2 monitors and protects against reverse current events, which can be the result of a malfunction in the power supply or noise induced in the input voltage rail under certain load characteristics (for example, when the load is largely capacitive).

The protection mechanism disables the eFuse's output and triggers when the reverse current exceeds the preset magnitude and this condition remains for at least 7.5 μs.

The NIS64x2 automatically re−enables its output once the input voltage exceeds the output voltage for at least 100 μs.

Current Limit

The current limit circuit uses a SENSEFET along with a reference and amplifier to control the peak current in the device. The SENSEFET allows for a small fraction of the load current to be measured, which has the advantage of reducing the losses in the sense resistor. The current limit circuit has two limiting values, one for short circuit hold current − I_{SC}, another is overload current limit I_{OL}. Refer to Figure 4. for dependence of I_{OL} and I_{SC} vs current limit resistor R_{LIM}.

Load Current Monitoring

The current monitor I_{SENSE} pin provides a small current proportional to the main device current which is flowing through the device. This pin should have a decoupling capacitor to filter out internal sampling noise. A resistor connected between the I_{SENSE} pin and GND converts the I_{SENSE} current into a GND referenced voltage. This pin can be floated if the feature is not required by application. Connect this pin to ground through 1 kOhm 1% resistor and

a 1 μF capacitor to ground to read the voltage corresponding to a load current.

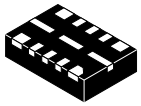
Slew Rate Control

The dV/dt circuit brings the output voltage up under a linear, controlled rate regardless of the load impedance characteristics. An internal ramp generator creates a linear ramp, and a control circuit forces the output voltage to follow that ramp, scaled by a factor. The default ramp time is approximately 1.0 ms. This pin includes an internal current source of approximately 1 μA. Since the current level is very low, it is important to use a ceramic cap or other low leakage capacitor. Aluminum electrolytic capacitors are not recommended for this circuit. Refer to Figure 5. for the typical ramp time vs Cdvdt capacitor. Anytime that the unit shuts down due to a fault, enable shut−down, or recycling of input power, the timing capacitor will be discharged and the output voltage will ramp from 0 at turn on.

ORDERING INFORMATION

Device	Input Voltage	Marking	Auto−Retry/Latch	Package	Shipping†
NIS6432MT1TWG	3.3 V	63L	Latch	WQFN 2x3 (Pb−Free)	3000 / Tape & Reel
NIS6432MT2TWG	3.3 V	63A	Auto−Retry		3000 / Tape & Reel
NIS6452MT1TWG	5.0 V	65L	Latch		3000 / Tape & Reel
NIS6452MT2TWG	5.0 V	65A	Auto−Retry		3000 / Tape & Reel

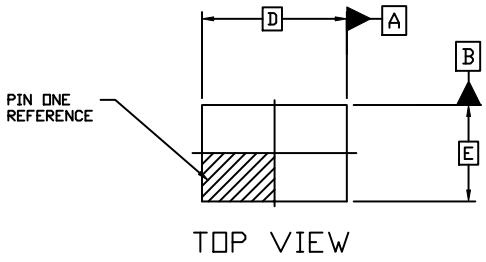
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



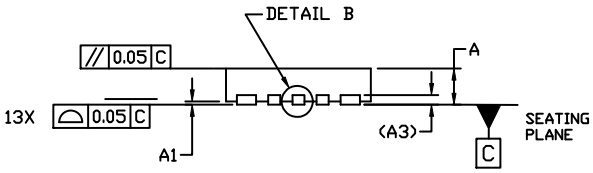
SCALE 4:1

WQFN12 3.0x2.0, 0.5P
CASE 510BM
ISSUE C

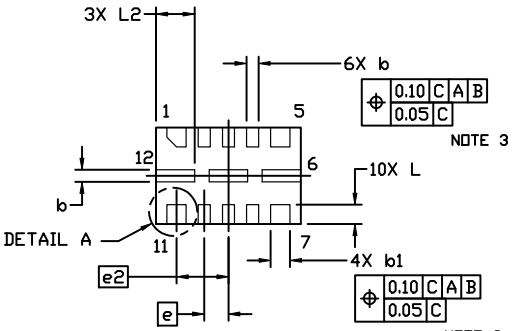
DATE 09 DEC 2019



TOP VIEW



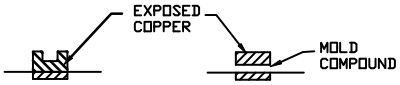
SIDE VIEW



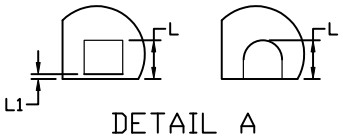
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b AND b1 APPLY TO THE PLATED TERMINALS AND ARE MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

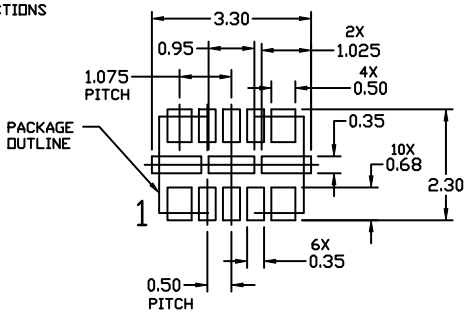


DETAIL B
OPTIONAL CONSTRUCTIONS



DETAIL A
OPTIONAL CONSTRUCTIONS

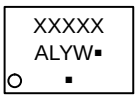
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
b1	0.35	0.40	0.45
D	2.90	3.00	3.10
E	1.90	2.00	2.10
e	0.50 BSC		
e2	1.075 BSC		
L	0.30	0.40	0.50
L1	0.00	---	0.15
L2	0.70	0.80	0.90



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON93408F**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**WQFN12 3.0X2.0, 0.5P**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales