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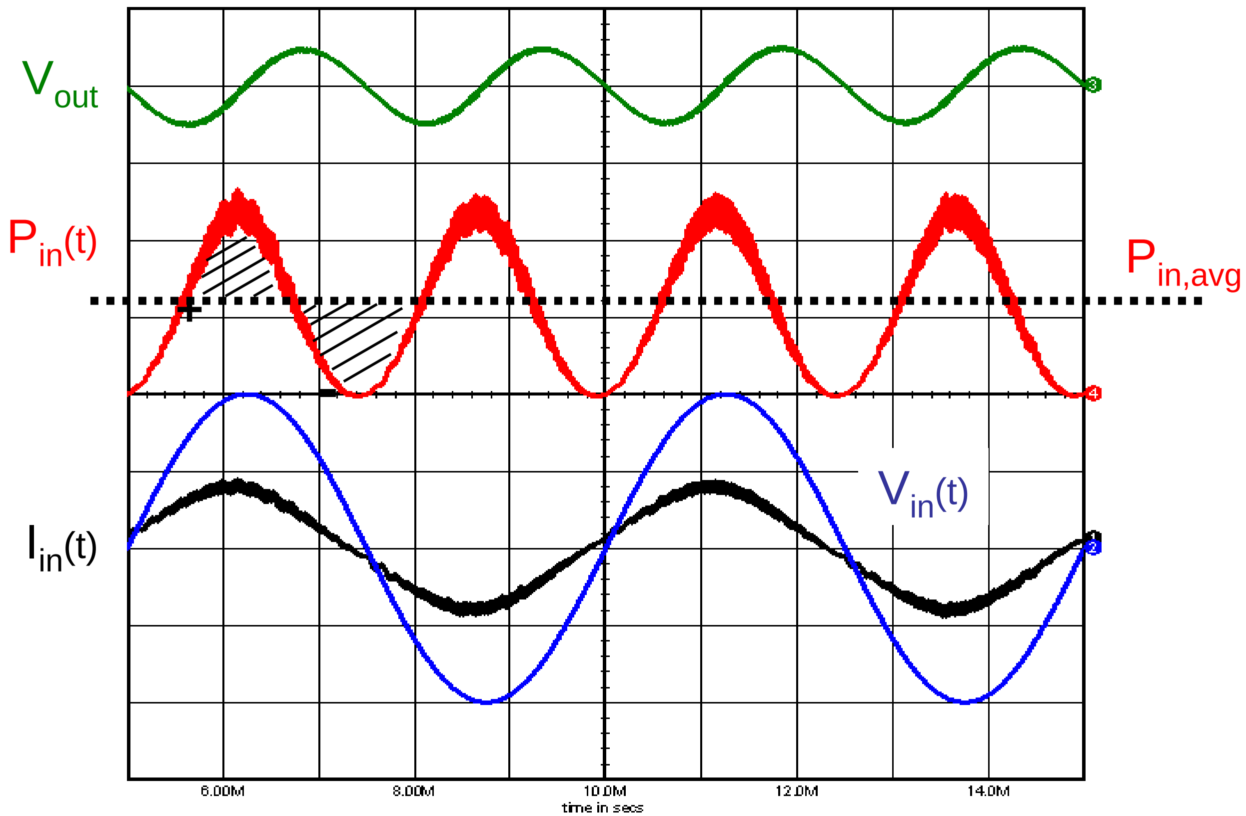
ON Semiconductor®

补偿PFC段
Compensating PFC Stages

议程 Agenda

- ❑ 简介 Introduction
- ❑ 导出小信号模型 Deriving a small-signal model
  - – 一般方法 General method
  - – 实际案例：NCP1605驱动的PFC段 Practical example: NCP1605-driven PFC stages
- ❑ 补偿环路 Compensating the loop
  - – 第2类补偿 Type-2 compensation
  - – 交流线路及功率电平影响 Influence of the line and power level
  - – 计算补偿 Computing the compensation
  - – 实际案例 Practical example
- ❑ 总结 Summary

输出电压低频纹波 Output Voltage Low Frequency Ripple



- 负载功率需求仅匹配平均值 The load power demand is matched in average only
- PFC功能本质上会有**低频纹波** A **low frequency ripple** is inherent to the PFC function

PFC段是低频工作系统
PFC Stages are Slow Systems…

- 必须滤除输出纹波，防止电流失真
  The output ripple must be filtered to avoid current distortion.

- 在实际工作,环路频率会选择在20 Hz范围, 这是非常低
  In practice, the loop frequency is selected in the range of 20 Hz, which is very low.

- 即使带宽低，环路也必须作补偿!
  Even if the bandwidth is low, the loop must be compensated!

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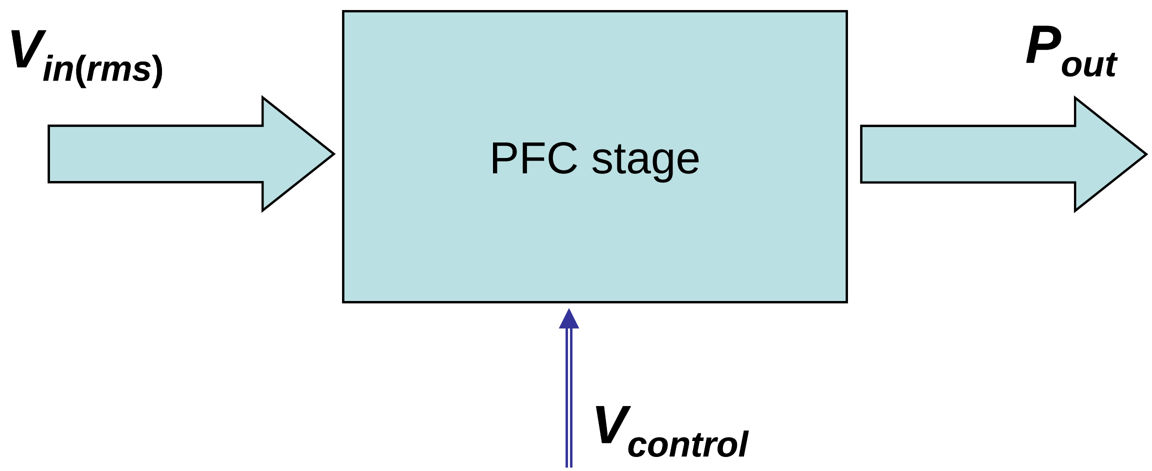
PFC段简化表现 A Simple Representation

- 将PFC段视作一个系统，在输入均方根(rms)电压及控制信号的条件下提供功率 We will consider the PFC stage as a system delivering a power under an input rms voltage and a control signal

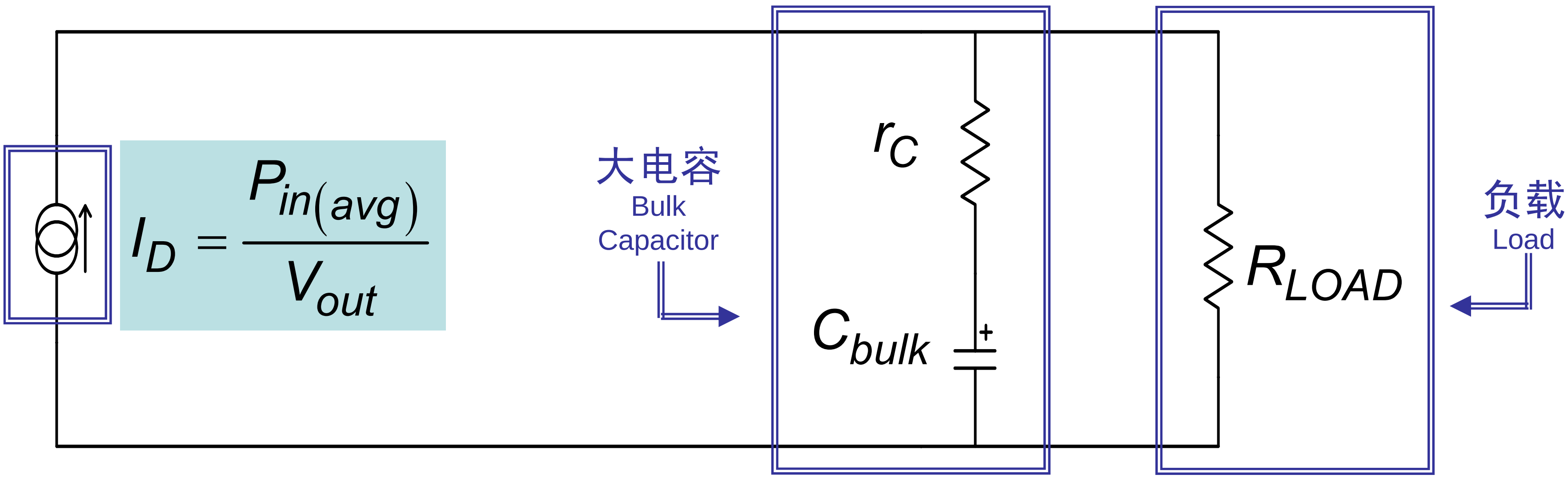


- 忽略具体的功率处理问题 Details of the power processing are ignored:
  - 工作模式(CrM，CCM，电压或电流模式…) Operation mode (CrM, CCM, Voltage or Current mode…)
  - 能效100%，仅考虑正弦信号的平均功率部分 100% efficiency, only the average power contribution of the sinusoidal signals is considered

PFC段简化大信号模型 A Simple Large Signal Model

- 将PFC段表现为电流源，传送能量到大电容及负载

  Let's represent the PFC stage as a current source delivering the power to the bulk capacitor and the load



- $P_{in(avg)}$取决于$V_{control}$（永远）、$V_{in(rms)}$（缺少前馈时）及V_{out}（有时）

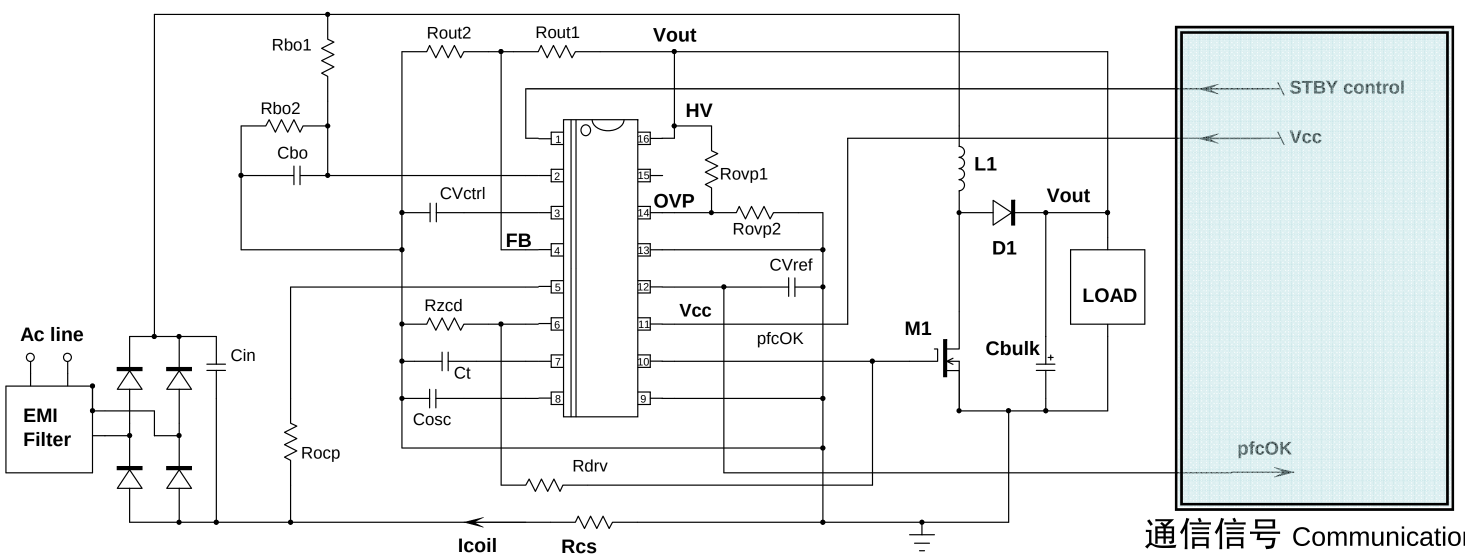
  $P_{in(avg)}$ depends on $V_{control}$ (always), on $V_{in(rms)}$ (in the absence of feedforward) and sometimes on V_{out}

- 3种可能的干扰源：$V_{control}$、V_{out}及$V_{in(rms)}$.

  3 possible sources of perturbations: $V_{control}$, V_{out} and $V_{in(rms)}$.

NCP1605

- ❑ 频率钳位临界导电模式(FCCrM) Frequency Clamped Critical Conduction Mode (FCCrM)
- ❑ 主PFC关键特性 Key features for a master PFC:
  - 高压电流源，待机模式软跳周期 High voltage current source, Soft-Skip™ during standby mode
  - 提供“pfcOK”信号，动态响应增强器 “pfcOK” signal, dynamic response enhancer
  - 多种保护特性，便于设计强固的PFC段 Bunch of protections for rugged PFC stages
- ❑ 市场：大功率交流适配器、液晶电视 Markets: high power ac adapters, LCD TVs



通信信号 Communication signals

NCP1605-跟随升压 NCP1605 – Follower Boost

- 电压模式工作：电路藉调制MOSFET导通时间来调节功率电平
  Voltage mode operation: the circuit adjusts the power level by modulating the MOSFET conduction time
- 时序电容的充电电流与反馈方波、并因此与(V_{out})^{2}成正比 The charge current of the timing capacitor is proportional to the FB square and hence to (V_{out})^2:

$$I_{charge} = I_t \cdot \left(\frac{V_{out}}{V_{out,nom}} \right)^2$$

其中 where：

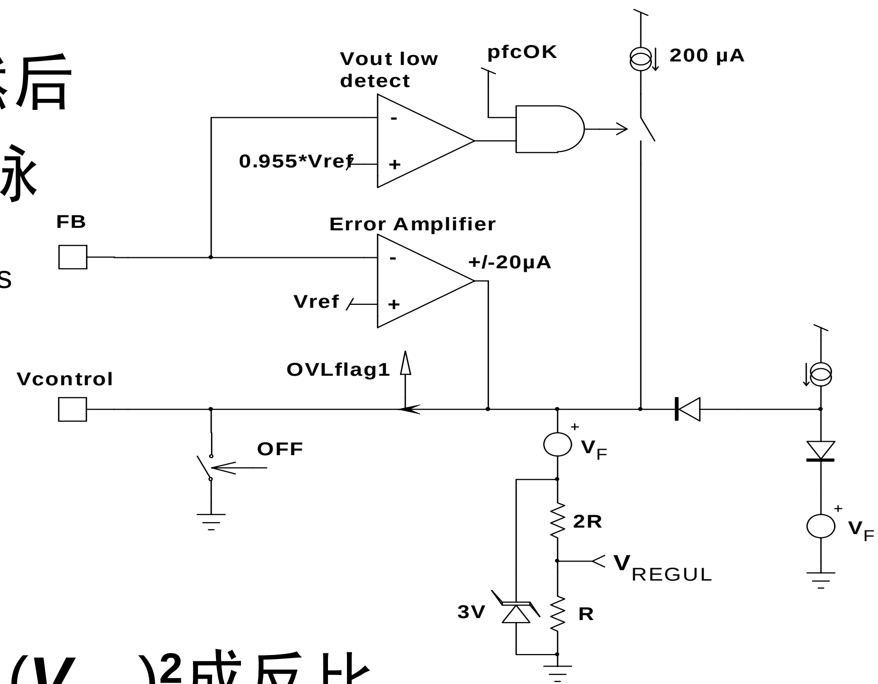
- $V_{out,nom}$是输出稳压电压 $V_{out,nom}$ is the V_{out} regulation voltage
- I_t**是**370 µA**电流源** I_t is a 370-µA current source

- 导通时间与(V_{out})^{2}成反比，支持跟随升压功能 The on-time is inversely proportional to (V_{out})^2 allowing the Follower boost function:

$$t_{on} = \frac{C_t \cdot V_{ton}}{I_t} \cdot \left(\frac{V_{out,nom}}{V_{out}} \right)^2$$

NCP1605-功率表达式 NCP1605 - Power Expression

- 控制信号是V_F先向下偏置、然后除以3所得到的V_{REGUL}，用于脉宽调制(PWM) 部分 The control signal is V_F offset down and divided by 3 to form V_{REGUL} used in the PWM section



- 故由于跟随升压功能，功率与$(V_{out})^2$成反比 Hence due to the follower boost function, the power is inversely dependent on $(V_{out})^2$:

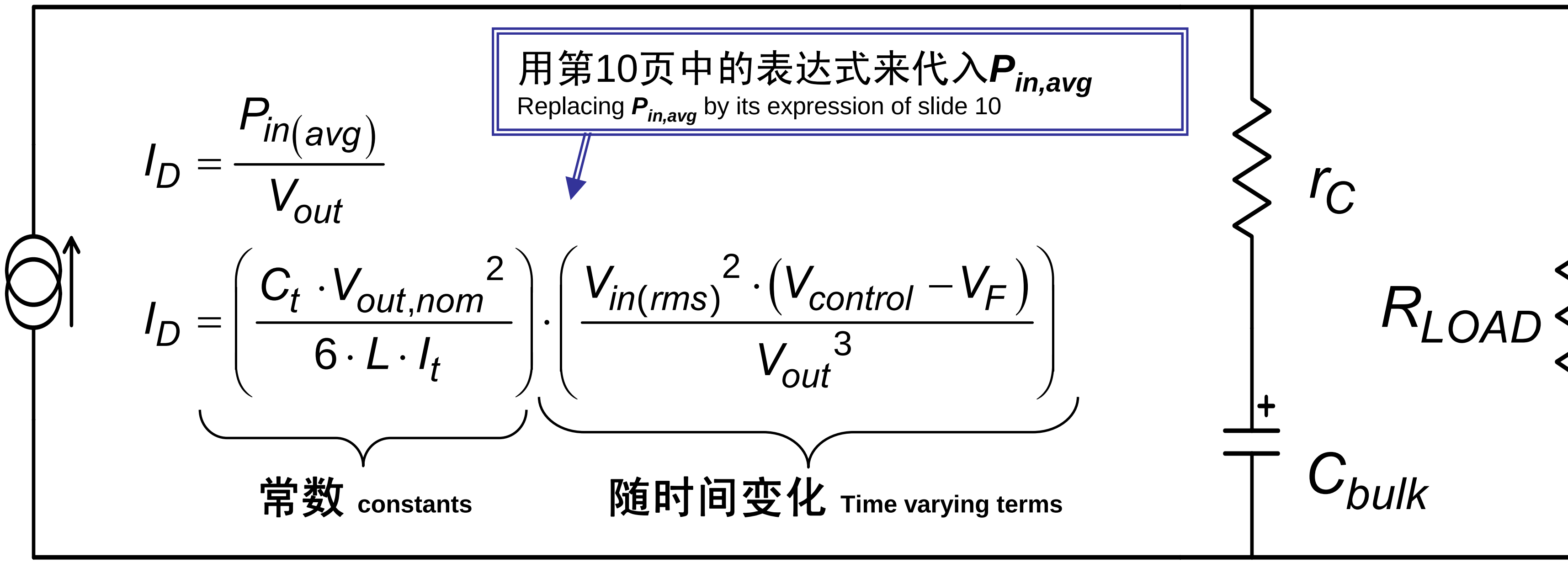
$$P_{in(avg)} = \frac{C_t \cdot V_{in(rms)}^2}{2 \cdot L \cdot I_t} \cdot \left(\frac{V_{out,nom}}{V_{out}}\right)^2 \cdot \frac{(V_{control} - V_F)}{3}$$

NCP1605-大信号模型

NCP1605 - Large Signal Model

❑ 将PFC段表现为电流源，传送能量到大电容及负载

Let’s represent the PFC stage as a current source delivering the power to the bulk capacitor and the load:



用第10页中的表达式来代入$P_{in,avg}$

Replacing $P_{in,avg}$ by its expression of slide 10

$$I_D = \frac{P_{in(avg)}}{V_{out}}$$

$$I_D = \underbrace{\left(\frac{C_t \cdot V_{out,nom}{}^2}{6 \cdot L \cdot I_t}\right)}_{\text{常数 constants}} \cdot \underbrace{\left(\frac{V_{in(rms)}{}^2 \cdot (V_{control} - V_F)}{V_{out}{}^3}\right)}_{\text{随时间变化 Time varying terms}}$$

❑ 3种干扰源：$V_{CONTROL}$、V_{out}及$V_{in(rms)}$

3 sources of perturbations: $V_{CONTROL}$, V_{out} and $V_{in(rms)}$.

小信号模型 Small Signal Model

- 大信号模型是非线性，因为I_D由$V_{control}$、$V_{in,rms}$及V_{out}的乘法及除法运算而构成

  A large signal model is nonlinear because I_D is formed of the multiplication and division of $V_{control}$, $V_{in,rms}$ and V_{out}.

- 这个模型需要线性化，评估每个变量的交流成分

  This model needs to be linearized to assess the ac contribution of each variable

- 这模型在静态工作点(直流点)附近扰动及线性化

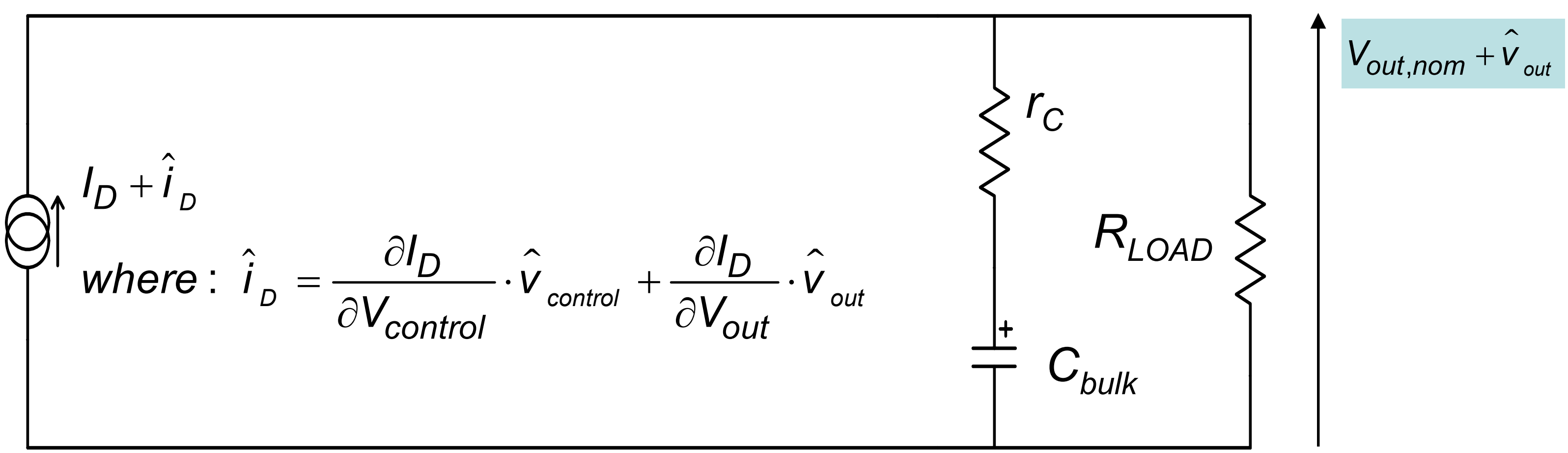
  The model is perturbed and linearized around a quiescent operating point (dc point)

考虑直流值附近的变量

Considering Variations Around the Dc Value…

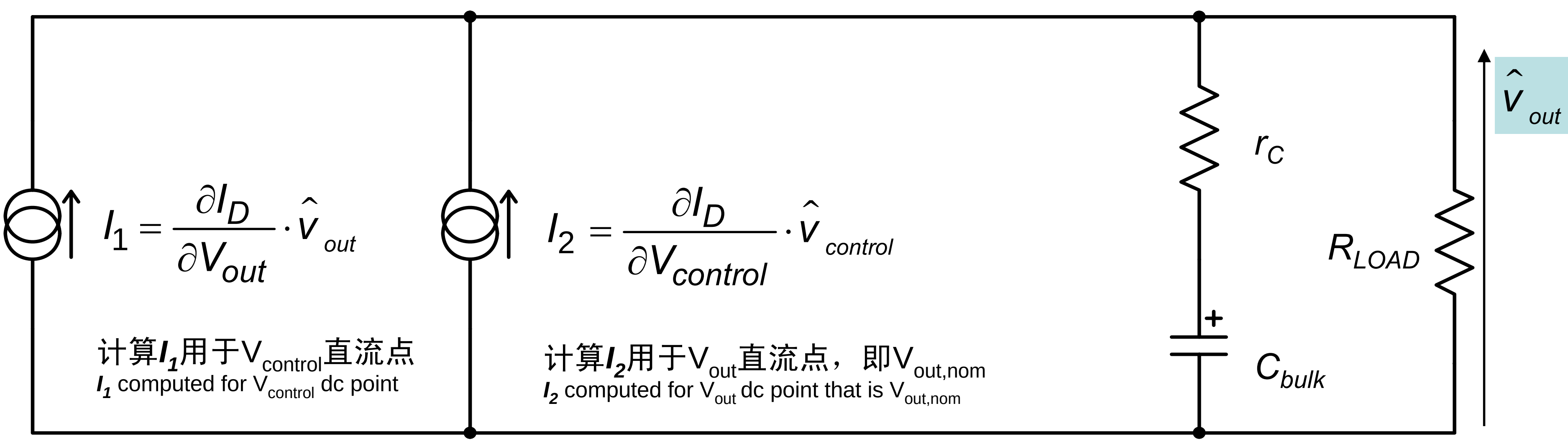
- 忽略交流线的微扰(假定为常量) Let's omit the perturbations of the line magnitude (assumed constant)
- 考虑V_{out}及$V_{control}$直流值附近的小变量 Let's consider small variations around the dc values for V_{out} and $V_{control}$:
- 然后我们获得 We then obtain:

$$\hat{i}_D = \frac{\partial I_D}{\partial V_{control}} \cdot \hat{v}_{CONTROL} + \frac{\partial I_D}{\partial V_{out}} \cdot \hat{v}_{out}$$



导出小信号模型 Deriving a Small Signal Model…

- 直流部分可以去除The dc portion can be eliminated
- 在直流点计算偏导数，即 The partial derivatives are to be computed at the dc point that is for:
  - $V_{control}$ 是控制信号直流值，用于所考虑的工作点 that is the control signal dc value for the considered working point
  - $V_{out,nom}$是额定(直流)输出电压 that is the nominal (dc) output voltage
- 用等式替代导数，我们就获得 Replacing the derivations by their expression, we obtain:



输出电压干扰成分 Contribution of the V_{out} Perturbations

❑ 取决于控制器原理 Depending on the controller scheme

$$I_D = \frac{P_{in,avg}}{V_{out}} = \frac{f\left(V_{in(rms)}, V_{control}\right)}{\left(V_{out}\right)^{n+1}} \quad where\ n = 0,1\ or\ 2$$

- n=0 对应NCP1607 for NCP1607
- n=1 对应NCP1654(预测型CCM PFC, 当 $P_{in,avg} \propto \frac{V_{control} \cdot V_{in,rms}}{V_{out}}$)
  n=1 for NCP1654 (predictive CCM PFC for which)
- n=2 对应NCP1605(跟随升压-见第10页)
  n=2 for NCP1605 (follower boost – see slide 10)

❑ 在直流点 At the dc point

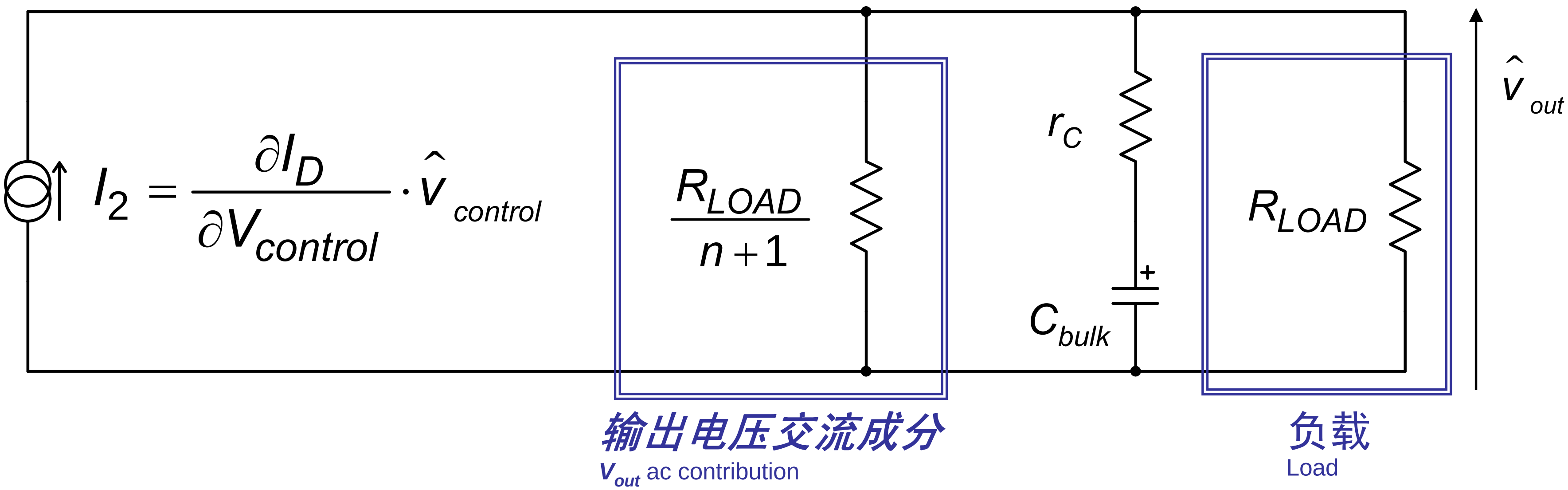
$$V_{out} = V_{out,nom} \quad and \quad \frac{P_{in(avg)}}{\left(V_{out,nom}\right)^2} = \frac{1}{R_{LOAD}}$$

❑ 最后得到 Finally:

$$I_1 = \frac{\partial I_D}{\partial V_{out}} \cdot \hat{v}_{out} = -\left.\frac{(n+1) \cdot f\left(V_{in(rms)}, V_{control}\right)}{\left(V_{out}\right)^{n+2}}\right|_{V_{out}=V_{out,nom}} \cdot \hat{v}_{out} = -\frac{(n+1) \cdot P_{in(avg)}}{\left(V_{out,nom}\right)^2} \cdot \hat{v}_{out} = -\frac{(n+1)}{R_{LOAD}} \cdot \hat{v}_{out}$$

简化为2个电阻型负载 2 Resistors…

- 因此，能简化小信号模型，如下图所示 Hence, the small signal model can be simplified as follows:



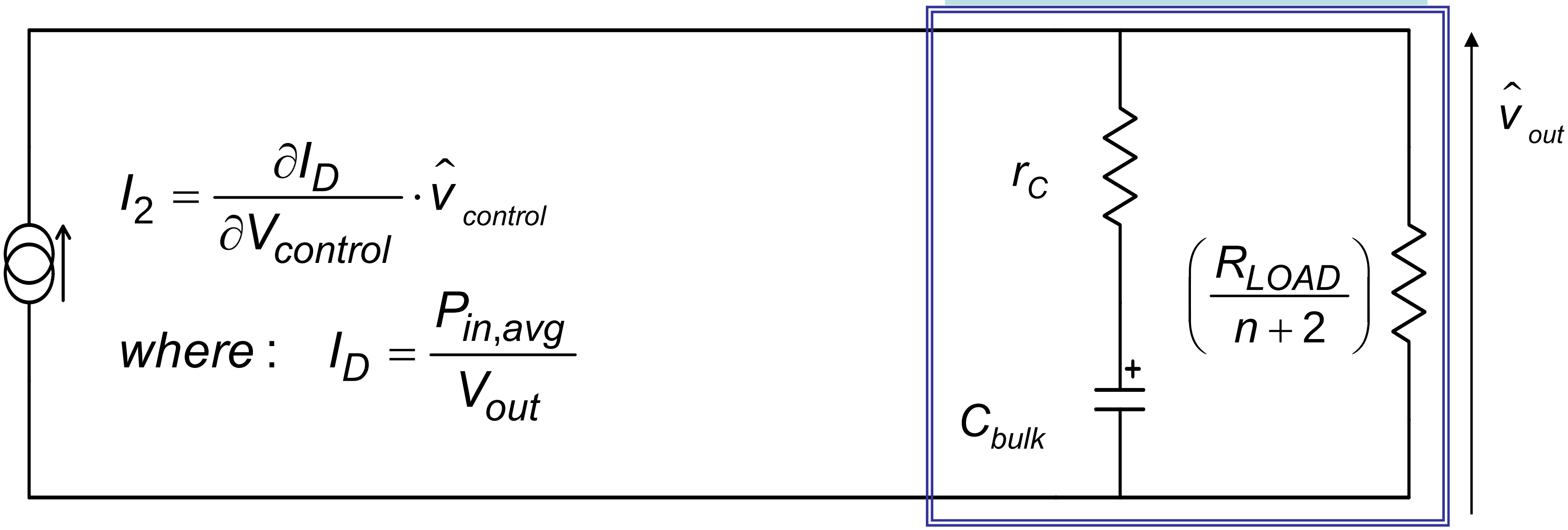
- 注意： Noting that: $\frac{R_{LOAD}}{n+1} \parallel R_{LOAD} = \frac{R_{LOAD}}{n+2}$

这模型还能进一步简化 the model can be further simplified

最终获得 Finally…

❑ 小信号模型 The small signal model is:

$$Z(s) = \frac{R_{LOAD}}{n+2} \cdot \frac{1 + s \cdot r_C \cdot C_{bulk}}{1 + s\left(\frac{R_{LOAD} \cdot C_{bulk}}{n+2}\right)}$$



$$I_2 = \frac{\partial I_D}{\partial V_{control}} \cdot \hat{v}_{control}$$

$$where: \quad I_D = \frac{P_{in,avg}}{V_{out}}$$

❑ 传递函数 The transfer function is:

$$\frac{\hat{v}_{out}}{\hat{v}_{control}} = \frac{R_{LOAD}}{n+2} \cdot \left(\frac{\partial I_D}{\partial V_{control}}\right) \cdot \frac{1 + s \cdot r_C \cdot C_{bulk}}{1 + s\left(\frac{R_{LOAD} \cdot C_{bulk}}{n+2}\right)}$$

NCP1605示例 NCP1605 Example

- 大信号模型表示为 The large signal model instructed that:

$$I_D = \frac{P_{in(avg)}}{V_{out}} = \left(\frac{C_t \cdot V_{out,nom}{}^2}{6 \cdot L \cdot I_t}\right) \cdot \left(\frac{V_{in(rms)}{}^2 \cdot (V_{control} - V_F)}{\boxed{V_{out}{}^3}}\right)$$

$\boxed{(V_{out})^{n+1} \text{ term}}$

- 因此 Hence:

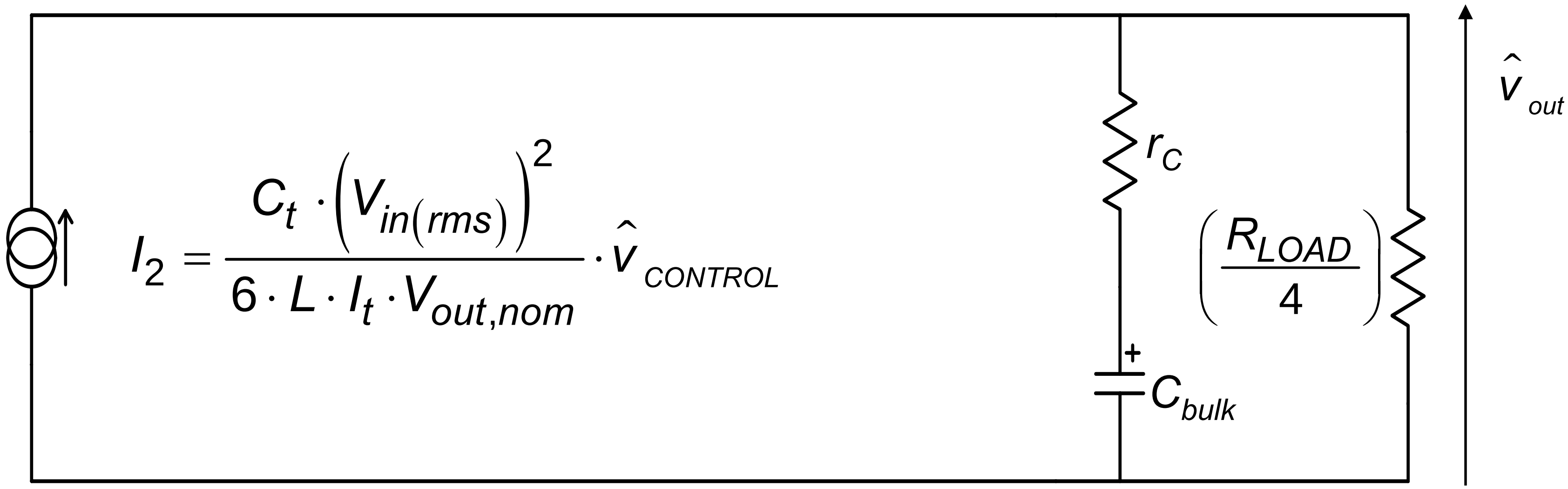
$$n = 2$$

$$\frac{\partial I_D}{\partial V_{control}} = \frac{C_t \cdot \left(V_{in(rms)}\right)^2}{6 \cdot L \cdot I_t \cdot V_{out,nom}}$$

NCP1605-小信号模型

NCP1605 - Small Signal Model

- 最终获得 Finally:



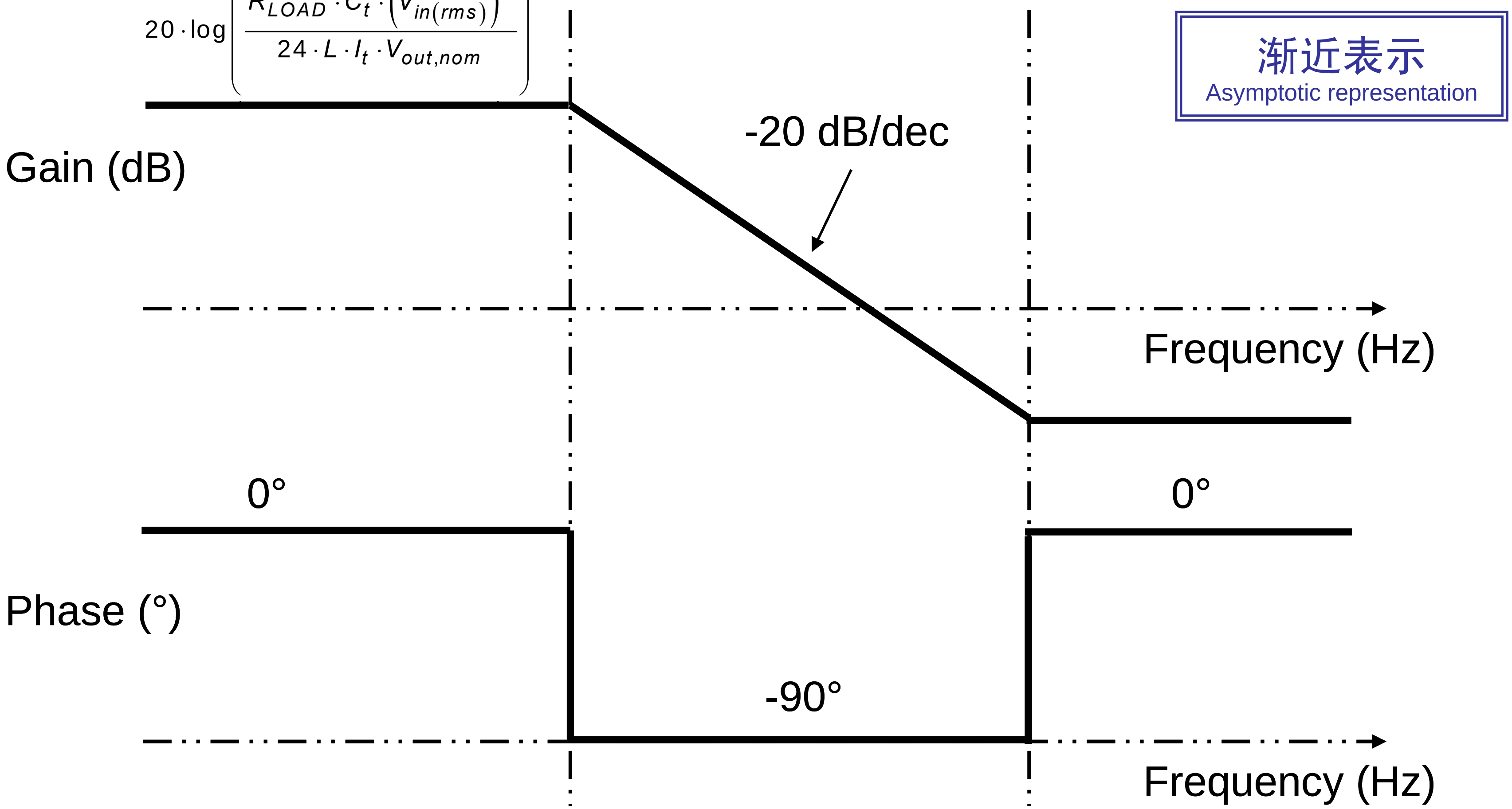
$$I_2 = \frac{C_t \cdot \left(V_{in(rms)}\right)^2}{6 \cdot L \cdot I_t \cdot V_{out,nom}} \cdot \hat{v}_{CONTROL}$$

- 传递函数是 The transfer function is:

$$\frac{\hat{v}_{out}}{\hat{v}_{CONTROL}} = \frac{R_{LOAD} \cdot C_t \cdot \left(V_{in(rms)}\right)^2}{24 \cdot L \cdot I_t \cdot V_{out,nom}} \cdot \frac{1 + s \cdot r_C \cdot C_{bulk}}{1 + s \cdot \left(\frac{R_{LOAD} \cdot C_{bulk}}{4}\right)}$$

电源段特性描述-波特图
Power stage characteristic – Bode Plots

$$20 \cdot \log\left(\frac{R_{LOAD} \cdot C_t \cdot \left(V_{in(rms)}\right)^2}{24 \cdot L \cdot I_t \cdot V_{out,nom}}\right)$$



$$f_{p0} = \frac{2}{\pi \cdot R_{LOAD} \cdot C_{bulk}} \qquad f_{z0} = \frac{1}{2\pi \cdot r_C \cdot C_{bulk}}$$

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补偿相位提升 Compensation Phase Boost

- 由大电容等效串联电阻(ESR)导致的零点太高，难以提供一些相位余量。忽略不计。 The zero brought by the bulk capacitor ESR is too high to bring some phase margin. It is ignored.

- PFC环路开路本质上会导致-360° 的相移 The PFC open loop inherently causes a -360° phase shift:
  - 电源段极点 Power stage pole ➔ -90°
  - 倒置误差放大器 Error amplifier inversion ➔ -180°
  - 补偿原极点 Compensation origin pole ➔ -90°

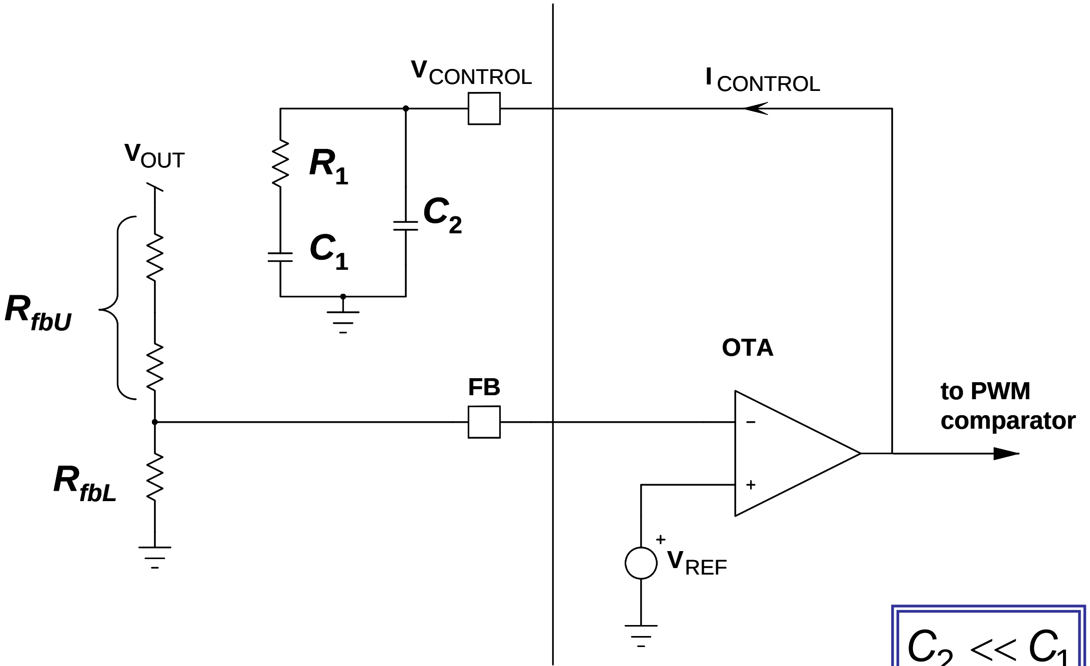
- 补偿必须提供一些相位提升 The compensation must then provide some phase boost

- **推荐第2类补偿 A type-2 compensation is recommended**

第2类补偿 Type-2 Compensation

❑NCP1605集成了传导误差变压器(OTA)

The NCP1605 embeds a transconductance error amplifier (OTA)



$$C_2 << C_1$$

$$f_{z1} = \frac{1}{2\pi \cdot R_1 \cdot C_1}$$

$$f_{p2} = \frac{1}{2\pi \cdot R_1 \cdot C_2}$$

$$f_{p1} = \frac{1}{2\pi \cdot R_0 \cdot C_1}$$

pole at the origin

$$R_0 = \frac{V_{out,nom}}{V_{ref} \cdot G_{EA}}$$

- V_{ref} is the reference voltage (generally 2.5 V in ON semi devices)
- G_{EA} is the OTA (200-µS transconductance gain for NCP1605, NCP1654 and NCP1631)

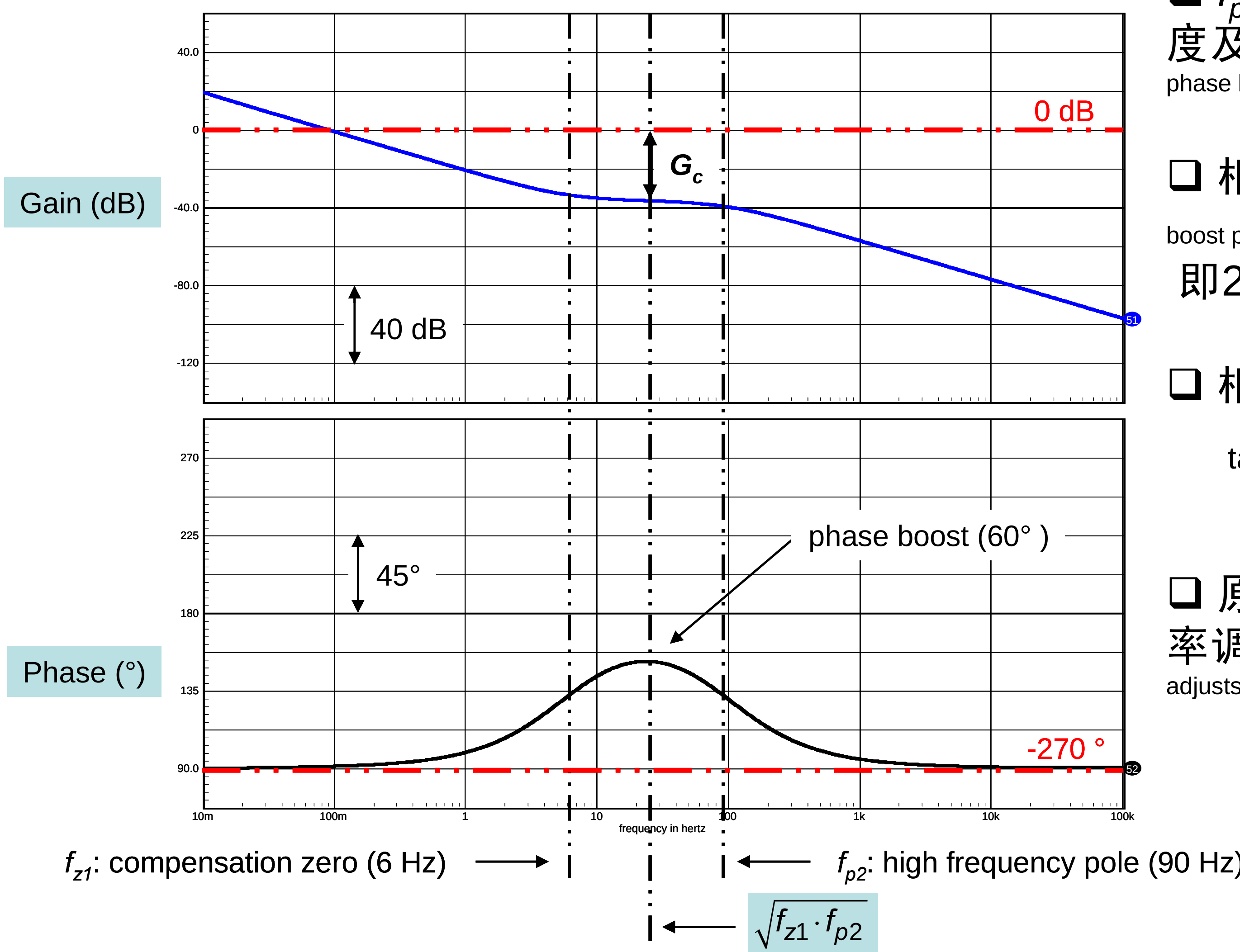
–R_{fbU}阻抗对补偿没有直接影响

No direct influence of the R_{fbU} impedance on the compensation

–仅反馈比例因数有影响

Only the feedback scale factor interferes

第2类补偿特性示例 Type-2 Characteristic - Example



- f_{p2}和f_{z1}确定相位提升幅度及位置(频率) f_{p2} and f_{z1} set the phase boost magnitude and location (frequency)

- 相位提升峰值为： The phase boost peaks at: $\left(f_{PhB} = \sqrt{f_{z1} \cdot f_{p2}}\right)$

  即27 Hz that is 27 Hz

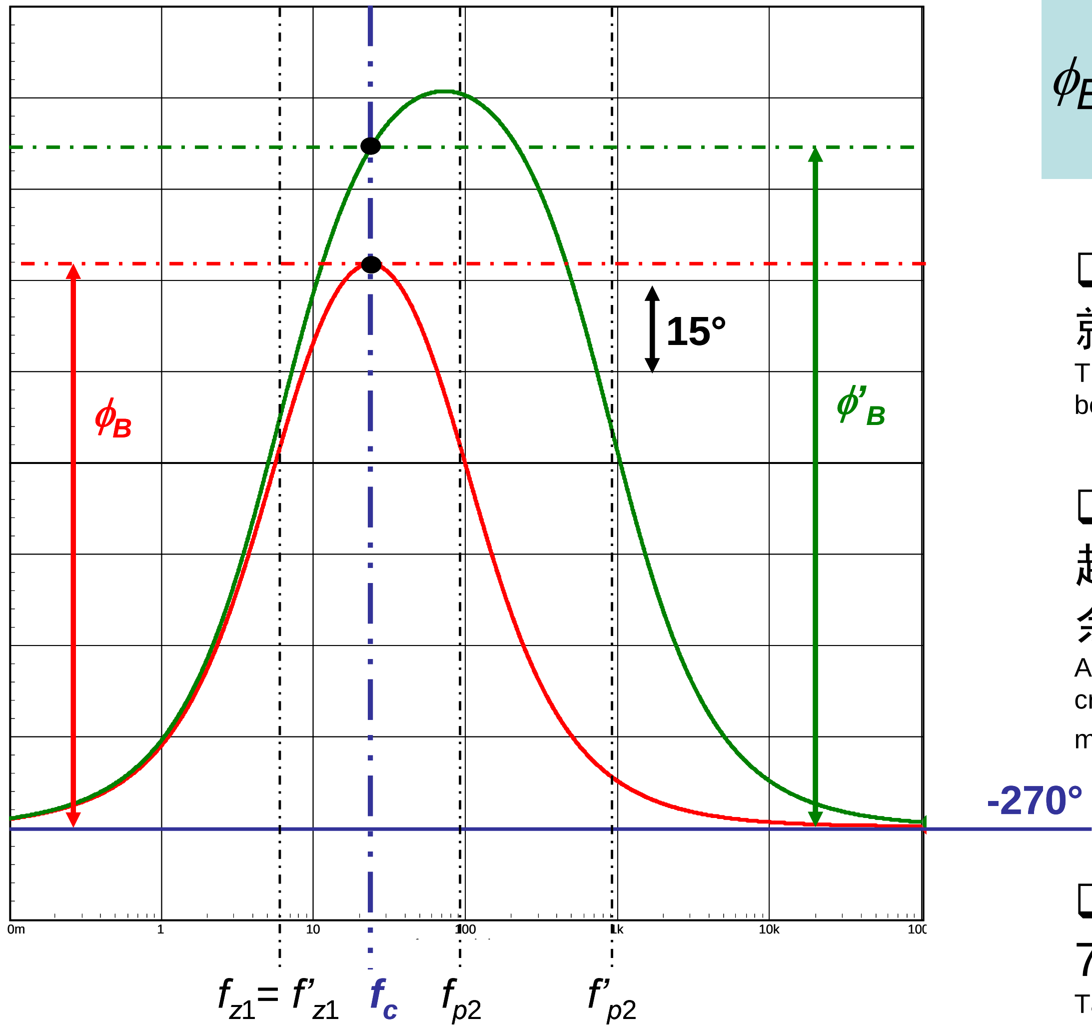
- 相位提升为 The phase boost is:

$$\tan^{-1}\left(\frac{f_{phB}}{f_z}\right) - \tan^{-1}\left(\frac{f_{phB}}{f_p}\right)$$

- 原极点f_{p1}以相位提升频率调节增益G_c The origin pole f_{p1} adjusts the gain G_c at the phase boost frequency

在交越频率相位提升

Phase Boost at the Crossover Frequency



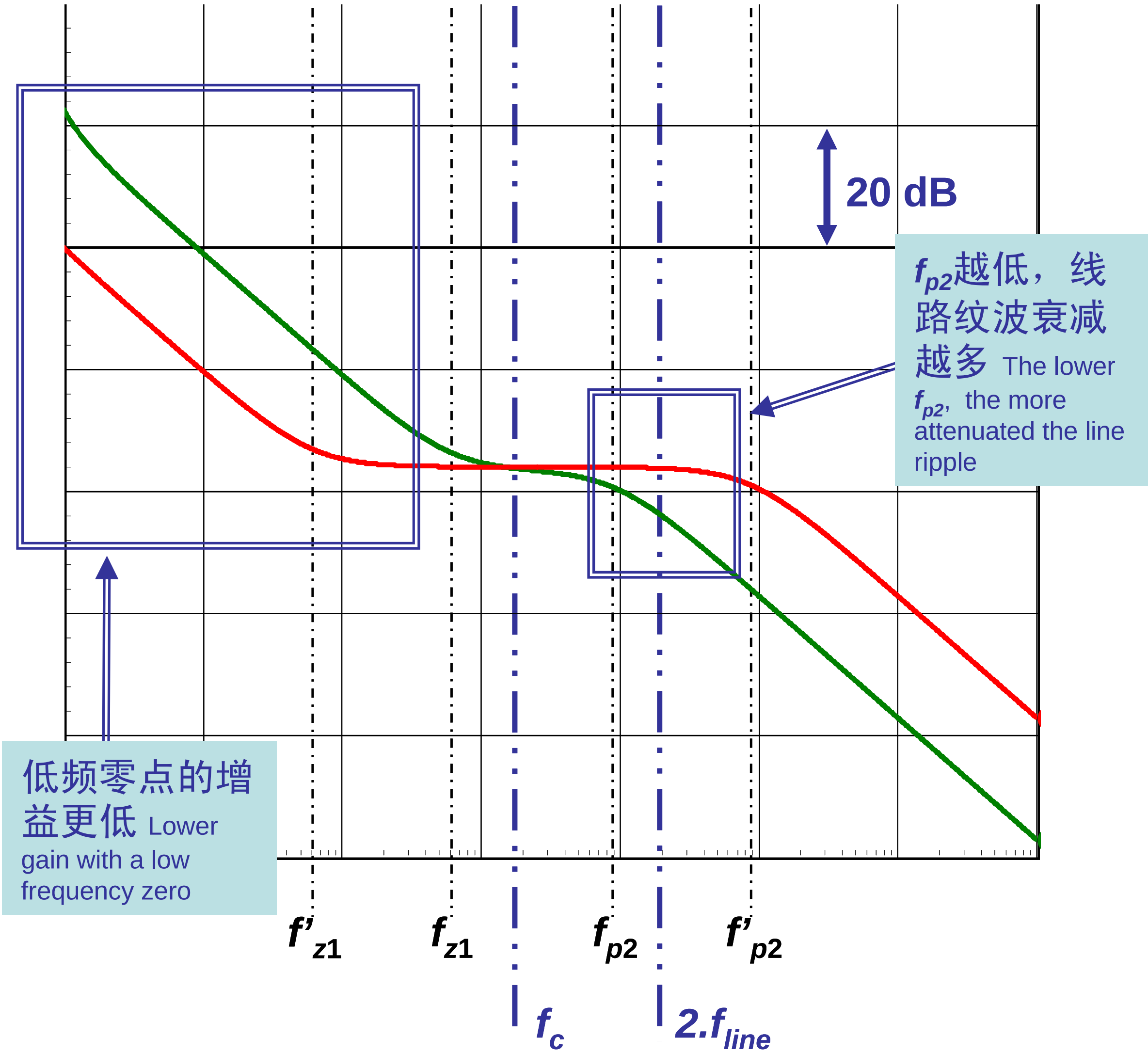
$$\phi_B = \tan^{-1}\left(\frac{f_c}{f_{z1}}\right) - \tan^{-1}\left(\frac{f_c}{f_{p2}}\right)$$

- ❑ f_{z1}越低和/或f_{p2}越高，相位提升就越高(最大值为90°)
  The lower f_{z1} and/or the higher f_{p2}, the higher the phase boost (max. value: 90°)

- ❑ 假定PFC电源段极点远低于交越频率(f_c)，相位提升就等于相位余量($\Phi_m = \Phi_B$)
  Assuming the PFC power stage pole is well below the crossover frequency (f_c), the phase boost equates the phase margin ($\phi_m = \varphi_B$)

- ❑ 将相位增益目标定在45 ° 与75° 之间
  Target a phase boost between 45 ° and 75°

增益考虑因素 Gain Considerations



- 红色迹线中，零点与极点频率之间的距离增加 In the red trace, the distance between the zero and the pole frequencies is increased
- 两种特性迹线在交越频率处产生的衰减相同 Both characteristics generate the same attenuation at the crossover frequency
- f_{z1}频率越低，低频区域中的增益就越低 The lower the f_{z1} frequency, the lower the gain in the low frequency region
- f_{p2}越高，($2.f_{line}$)纹波抑制就越低 The higher f_{p2}, the lower the ($2.f_{line}$) ripple rejection

第2类补偿器小结

Type-2 Compensator - Summary

- 零点不应置于太低的频率(不损及低频增益)
  The zero should not be placed at a too low frequency (not to penalize the low-frequency gain)
- 高频极点必须置于低至足以使交流线路纹波衰减的频率
  The high frequency pole must be placed at a frequency low enough to attenuate the line ripple
- 相位提升(及相位余量)取决于零点及高频极点位置
  The phase boost (and phase margin) depends on the zero and high-frequency pole locations
- 原极点设为在目标交越频率迫使开环增益为零
  The origin pole is set to force the open loop gain to zero at the targeted crossover frequency

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是否要全范围补偿？
Compensating for the Full Range?...

- 静态增益取决于负载，而如果没有前馈，取决于交流线路幅度 The static gain depends on the load and if there is no feedforward, on the line magnitude

$$G_{static(dB)} = 20 \cdot \log\left(\frac{R_{LOAD}}{n+2} \cdot \left(\frac{\partial I_D}{\partial V_{control}}\right)\right) = 20 \cdot \log\left(\frac{R_{LOAD} \cdot C_t \cdot \left(V_{in(rms)}\right)^2}{24 \cdot L \cdot I_t \cdot V_{out,nom}}\right) \qquad \text{(NCP1605)}$$

- 电源段极点以负载的函数而变化 The power stage pole varies as a function of the load:

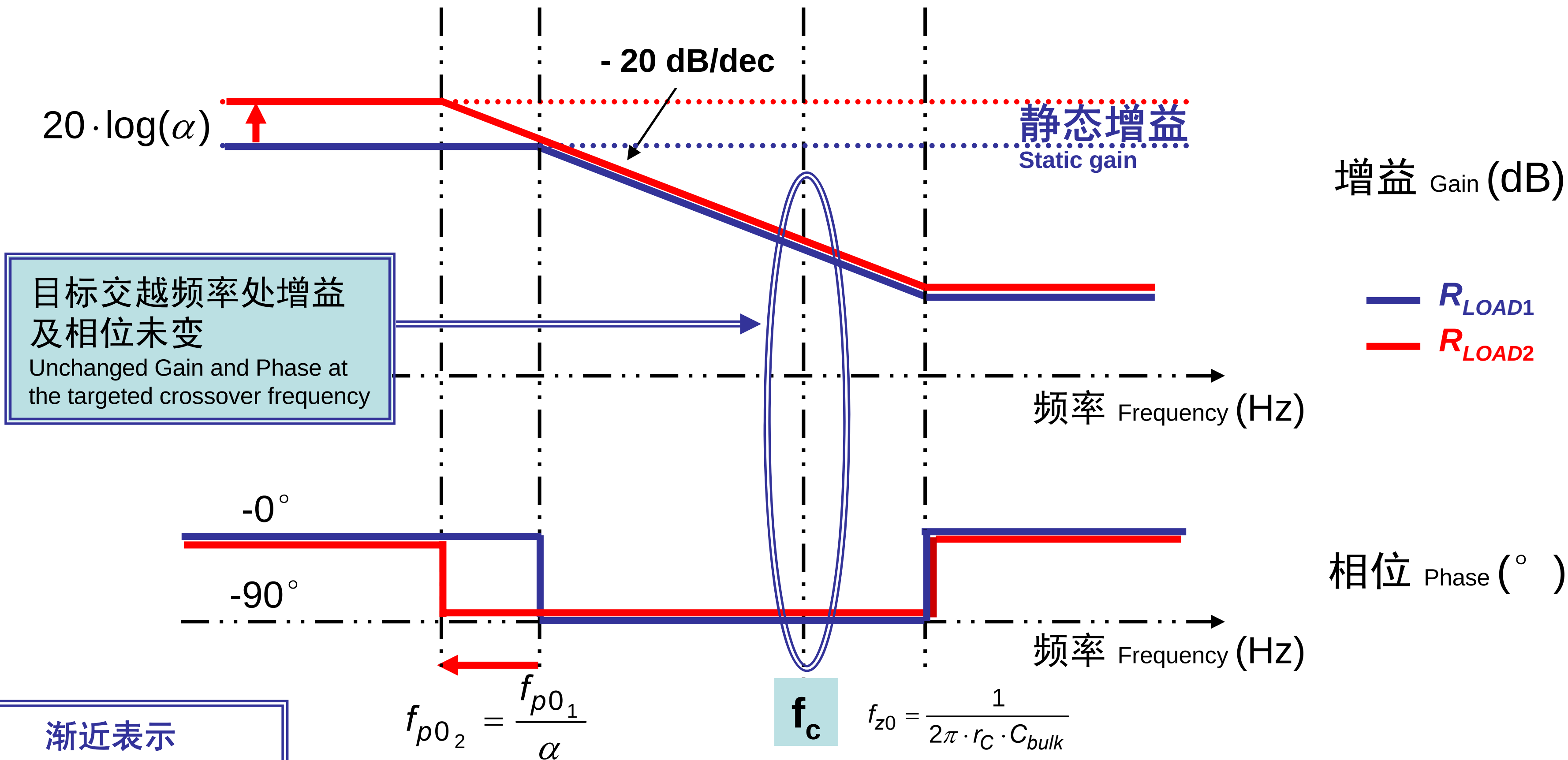
$$f_{p0} = \frac{n+2}{2\pi \cdot R_{LOAD} \cdot C_{bulk}} = \frac{2}{\pi \cdot R_{LOAD} \cdot C_{bulk}} \qquad \text{(NCP1605)}$$

- 在关闭环路时最坏情况如何？ What is the worst case when closing the loop?

负载对开环图的影响

Load Influence on the Open Loop Plots

- 增加负载电阻 Let's increase R_{LOAD} $\left(R_{LOAD2} = \alpha \cdot R_{LOAD1} \quad with \quad \alpha > 1\right)$

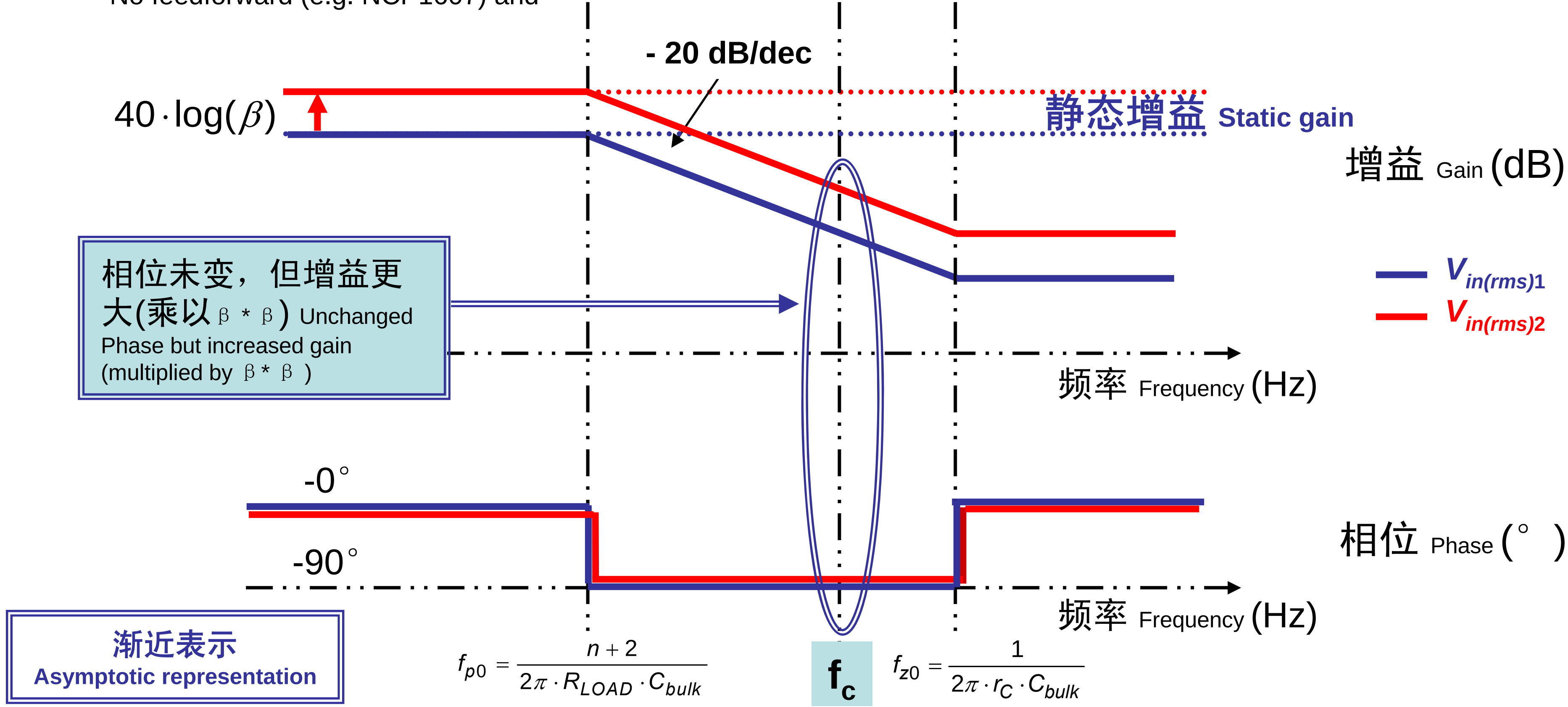


渐近表示
Asymptotic representation

f_c及 Φ_m不受影响！ **f_c and ϕ_m are not affected!**

交流线路对开环图的影响
Line Influence on the Open Loop Plots

❑ 无前反馈(如NCP1607)，及 $\left(V_{in(rms)2} = \beta \cdot V_{in(rms)1} \quad with \quad \beta > 1\right)$
No feedforward (e.g. NCP1607) and



环路交越频率乘以 β ² The loop crossover frequency is β ² increased

负载及交流线路考虑因素
Load and Line Considerations

- ❑满载时补偿 Compensate at full load
  - –与较轻负载时交越频率相同 Same crossover frequency at lighter loads
  - –优化设定了零点频率(不处于太低频率) The zero frequency is set optimally (not at a too low frequency)

- ❑在高交流线路输入时补偿 Compensate at high line
  - –交流高线路输入是最坏情况，因为没有前馈，静态增益正比于 $\left(V_{in(rms)}\right)^2$

    High line is the worst case as in the absence of feedforward, the static gain is proportional to
  - –即可得到 This leads to:

$$\left(f_c\right)_{HL} = \left(\frac{\left(V_{in(rms)}\right)_{HL}}{\left(V_{in(rms)}\right)_{LL}}\right)^2 \cdot \left(f_c\right)_{LL}$$

其中，HL代表最高线路输入，LL代表最低线路输入 Where HL stands for Highest Line and LL for Lowest Line

  - –在通用主电源应用中，高线路交越频率是低线路交越频率的9倍 In universal mains applications, the high-line crossover frequency is 9 times higher than the low-line one:

$$\left(f_c\right)_{HL} = \left(\frac{265}{90}\right)^2 \cdot \left(f_c\right)_{LL} \cong 9 \cdot \left(f_c\right)_{LL}$$

交越频率选择

Crossover Frequency Selection

- ❑没有前馈的条件下，$(f_c)_{HL} \le f_{line}$是个好选择 In the absence of feedforward, $(f_c)_{HL} \le f_{line}$ is a good option

- ❑有前馈时，应该选择 $(f_c)_{HL} \le \frac{f_{line}}{2}$，获得更好的低频纹波衰减 With feedforward, $(f_c)_{HL} \le \frac{f_{line}}{2}$ is rather selected for a better attenuation of the low frequency ripple

- ❑确保在交流线路输入范围下，PFC升压极点在满载时保持低于交越频率！
  Get sure that on the line range, the PFC boost pole remains lower than the crossover frequency at full load!

$$f_{p0} \le (f_c)_{LL}$$

- ❑否则，就增大大电容 If not, increase $\boldsymbol{C_{bulk}}$

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  - – 实际案例：NCP1605驱动的PFC段 Practical example: NCP1605-driven PFC stages
- ❑ 补偿环路 Compensating the loop
  - – 第2类补偿 Type-2 compensation
  - – 交流线路及功率电平影响 Influence of the line and power level
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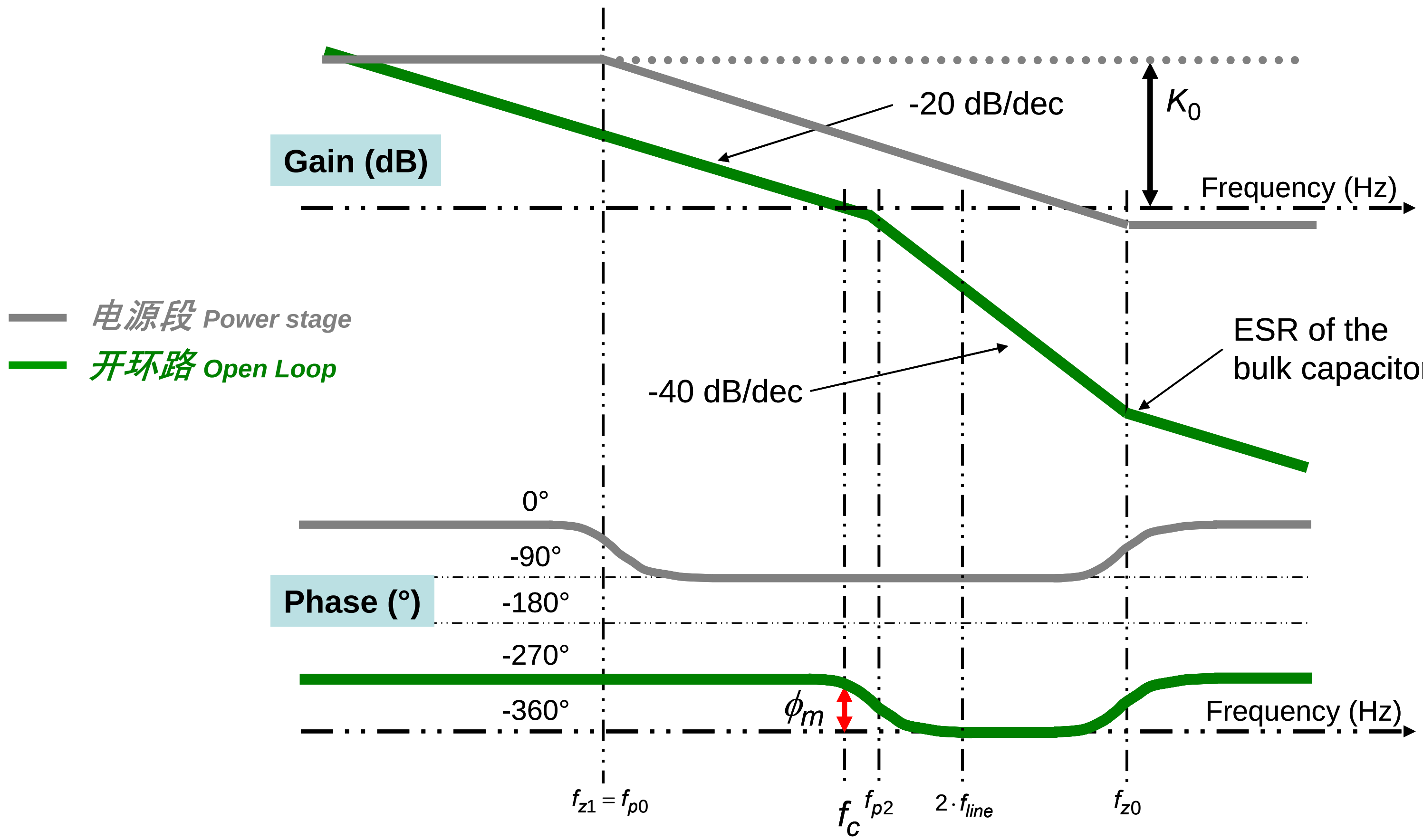
补偿技术
Compensation Techniques

- 存在几种技术 Several techniques exist:
  - 手动设置，“k因数”(Venable)……manual placement, “k factor” (Venable)…
    - \+ 系统化 Systematic
    - \- PFC升压增益将在f_c频率计算 The PFC boost gain is to be computed at f_c
    - -零点及高极点位置没有灵活性 No flexibility in the zero and high pole locations

$$f_c = k \cdot f_{z1} = \frac{f_{p2}}{k}$$

  - 极点和零点消除 Pole and zero cancellation:
    - ✓设置补偿零点，这样它就消除电源段极点 Place the compensation zero so that it cancels the power stage pole:
    - ✓迫使极点位于原点，从而在($f = f_c$)时消除PFC升压增益 Force the pole at the origin to cancel the PFC boost gain when ($f = f_c$)
    - ✓以高频极点调节相位余量 Adjust the phase margin with the high frequency pole

极点和零点消除 Pole and Zero Cancellation…



- ❑ f_{p2}越高，相位余量越大 The higher f_{p2}, the larger the phase margin
- ❑ f_{p2}越低，低频纹波抑制越佳 The lower f_{p2}, the better the rejection of the low frequency ripple
- ❑ $\phi_m = 45°$ 若 if $f_{p2} = f_c$

极点和零点设置 Poles and Zero Placement

- 针对满载、高线路输入来设计补偿
  Design the compensation for full load, high line:

$$R_{LOAD} = R_{LOAD(\min)}$$

- 恰当设置原极点以消除f_c时的静态增益K_0 Place the origin pole to cancel K_0, the static gain at f_c:

$$f_{p0} = \frac{f_c}{K_0} \quad \text{for} \quad R_{LOAD} = R_{LOAD(\min)}$$

$$\text{where}: \quad \frac{\hat{v}_{out}}{\hat{v}_{CONTROL}} = K_0 \cdot \frac{1 + s \cdot r_C \cdot C_{bulk}}{1 + s \cdot \left(\frac{R_{LOAD(\min)} \cdot C_{bulk}}{n+2} \right)}$$

- 恰当设置零点，消除PFC升压极点
  Place the zero so that it cancels the PFC boost pole

$$\left(f_{z1} = f_{p0} \right) \quad \text{for} \quad R_{LOAD} = R_{LOAD(\min)}$$

- 恰当设置f_{p2}，获得目标相位余量
  Place f_{p2} to obtain the targeted phase margin:

$$f_{p2} = \frac{f_c}{\tan\left(90° - \phi_m\right)}$$

示例 Example

- 宽范围主电源，基于NCP1605的150 W应用 A wide mains, 150-W application driven by the NCP1605
- $V_{out,nom} = 390$ V
- $(V_{in(rms)})_{LL} = 90$ V
- $(V_{in(rms)})_{HL} = 265$ V
- $L = 150$ µH
- $C_t = 4.7$ nF
- $C_{bulk} = 100$ µF
- $r_C = 500$ mW (ESR)
- $f_c = 50$ Hz

and $F_m = 60°$

@ high line (265 V)

$$\frac{\hat{v}_{out}}{\hat{v}_{CONTROL}} = K_0 \cdot \frac{1 + s \cdot r_C \cdot C_{bulk}}{1 + s \cdot \left(\frac{R_{LOAD} \cdot C_{bulk}}{4}\right)} \quad where: \quad K_0 = \frac{R_{LOAD} \cdot C_t \cdot \left(V_{in(rms)}\right)^2}{24 \cdot L \cdot I_t \cdot V_{out,nom}}$$

$$R_{LOAD(\min)} = \frac{\left(V_{out,nom}\right)^2}{\left(P_{out}\right)_{\max}} = \frac{390^2}{150} \cong 1\ k\Omega$$

$$R_0 = \frac{V_{out,nom}}{V_{ref} \cdot G_{EA}} = \frac{390}{2.5 \cdot 200 \cdot 10^{-6}} = 780\ k\Omega \quad (OTA)$$

$$C_1 = \frac{K_{0(\min)}}{2\pi \cdot f_c \cdot R_0} = \frac{R_{LOAD(\min)} \cdot C_t \cdot \left(V_{in(rms)}\right)_{HL}^2}{2\pi \cdot f_c \cdot R_0 \cdot 24 \cdot L \cdot I_t \cdot V_{out,nom}} = \frac{10^3 \cdot 4.7 \cdot 10^{-9} \cdot 265^2}{2\pi \cdot 50 \cdot 780k \cdot 24 \cdot 150\mu \cdot 370\mu \cdot 390} \cong 2.59\mu F \quad ==> \quad 2.2\,\mu F$$

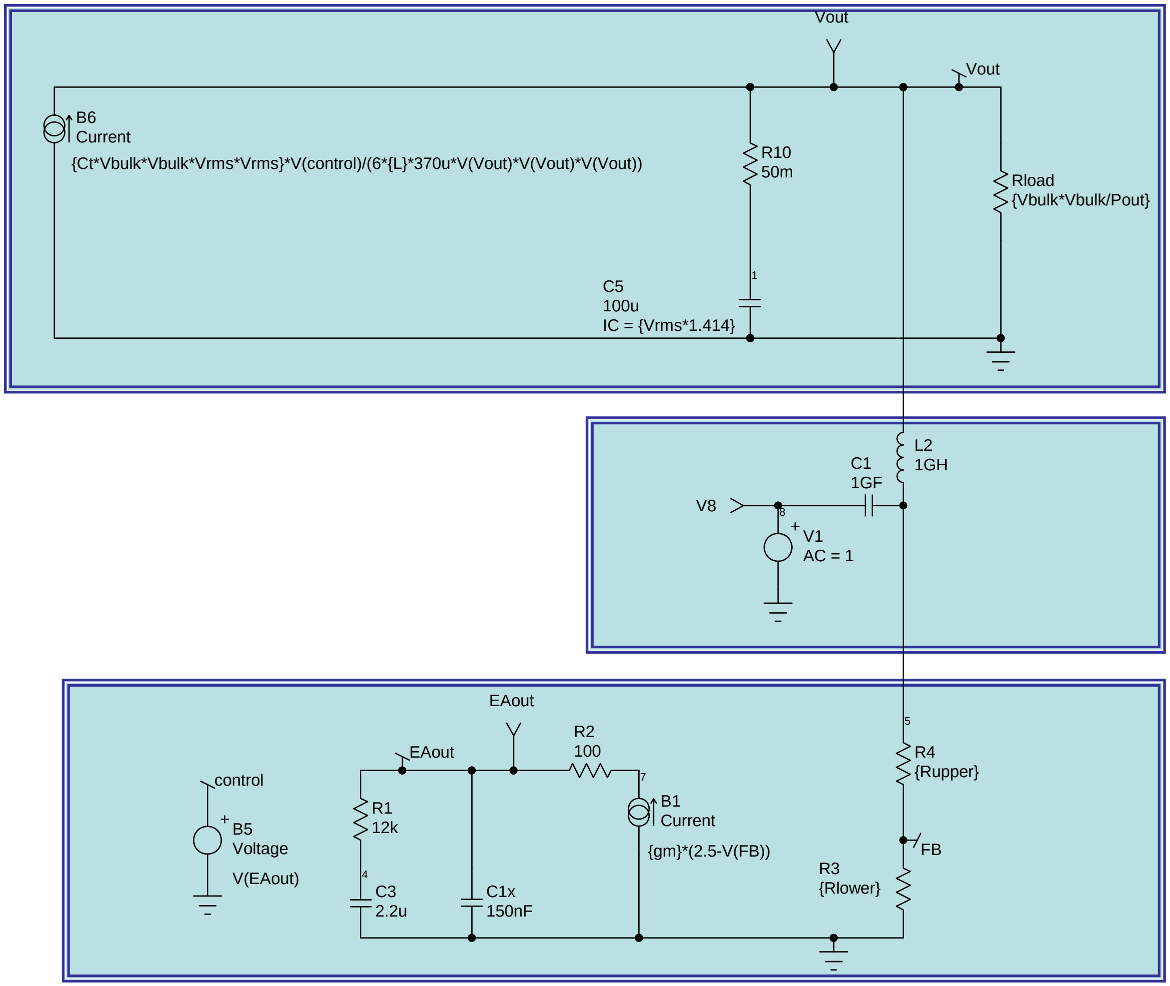
$$R_1 = \frac{R_{LOAD(\min)} \cdot C_{bulk}}{(n+2) \cdot C_1} = \frac{10^3 \cdot 100 \cdot 10^{-6}}{(2+2) \cdot 2.2 \cdot 10^{-6}} \cong 11.36\ k\Omega \quad ==> \quad 12\ k\Omega$$

$$C_2 = \frac{\tan(90° - \phi_m)}{2\pi \cdot f_c \cdot R_1} = \frac{\tan(90° - 60°)}{2\pi \cdot 50 \cdot 12 \cdot 10^3} \cong 153\ nF \quad ==> \quad 150\ nF$$

$$f_{p1} = \frac{1}{2\pi \cdot R_0 \cdot C_1} = 93\,mHz \qquad f_{z1} = \frac{1}{2\pi \cdot R_1 \cdot C_1} = 6\,Hz \qquad f_{z1} = \frac{1}{2\pi \cdot R_1 \cdot C_2} = 88\,Hz$$

仿真验证 Simulation Validation

- ❑ 仿真电路基于大信号模型 The simulation circuit is based on the large signal model:

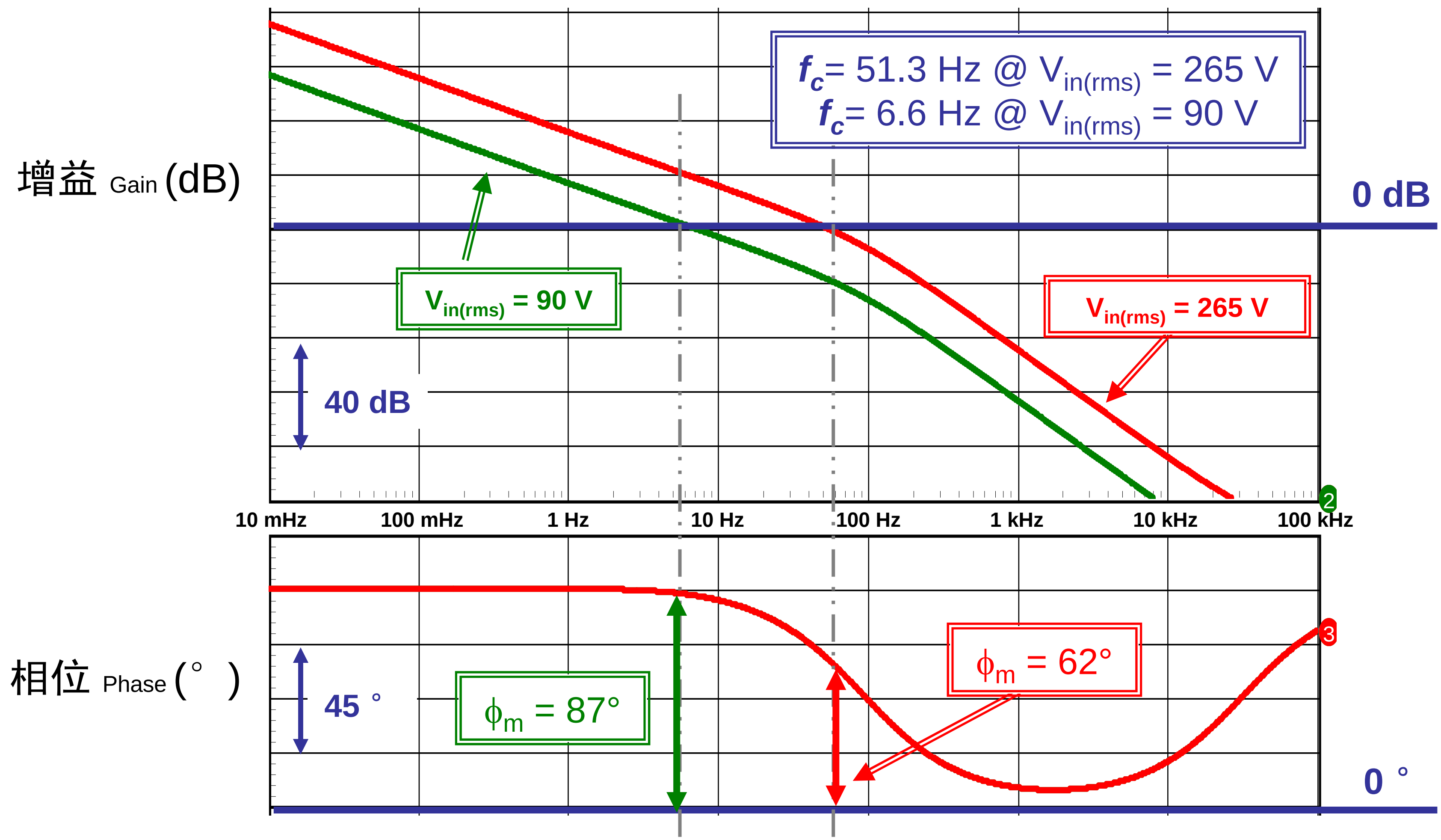


采用NCP1605的PFC段的大信号模型 Large signal model of the NCP1605-driven PFC stage

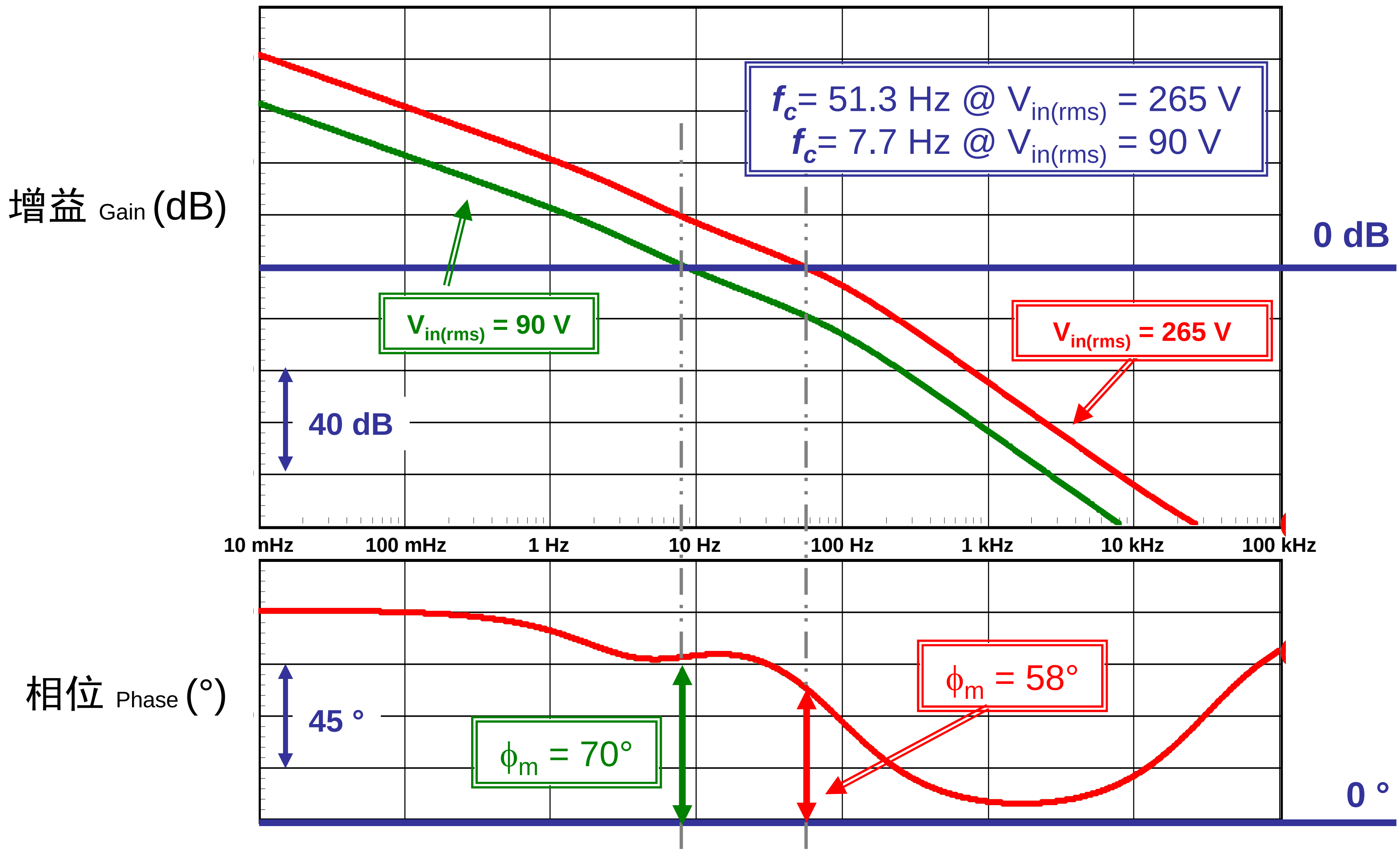
交流干扰的产生及抑制 Generation and injection of the ac perturbation

反馈及稳压电路(含第2类补偿) Feedback and regulation circuit (including type-2 compensation)

环路开路特性-满载 Open Loop Characteristic – Full Load

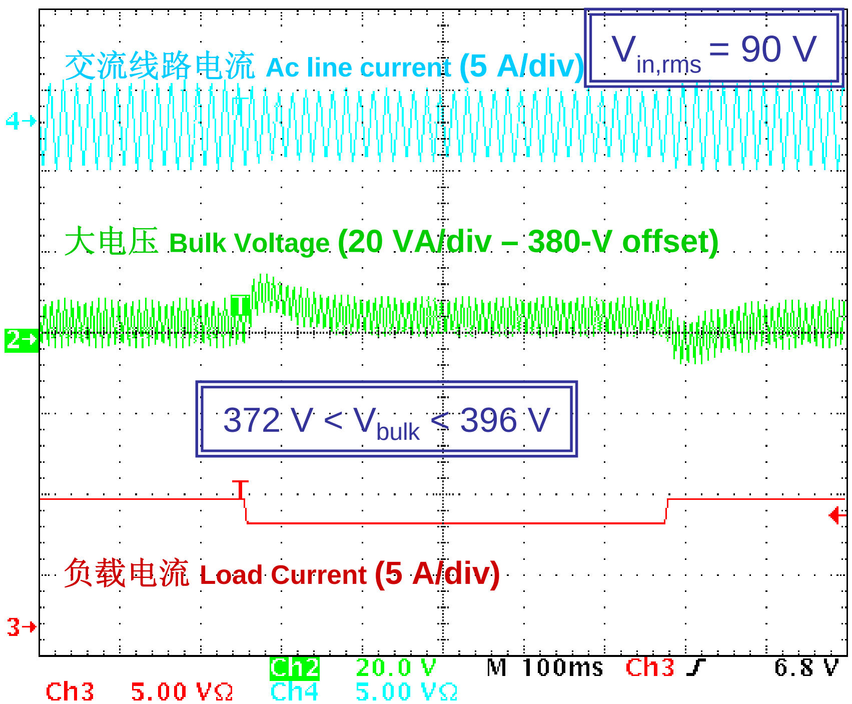


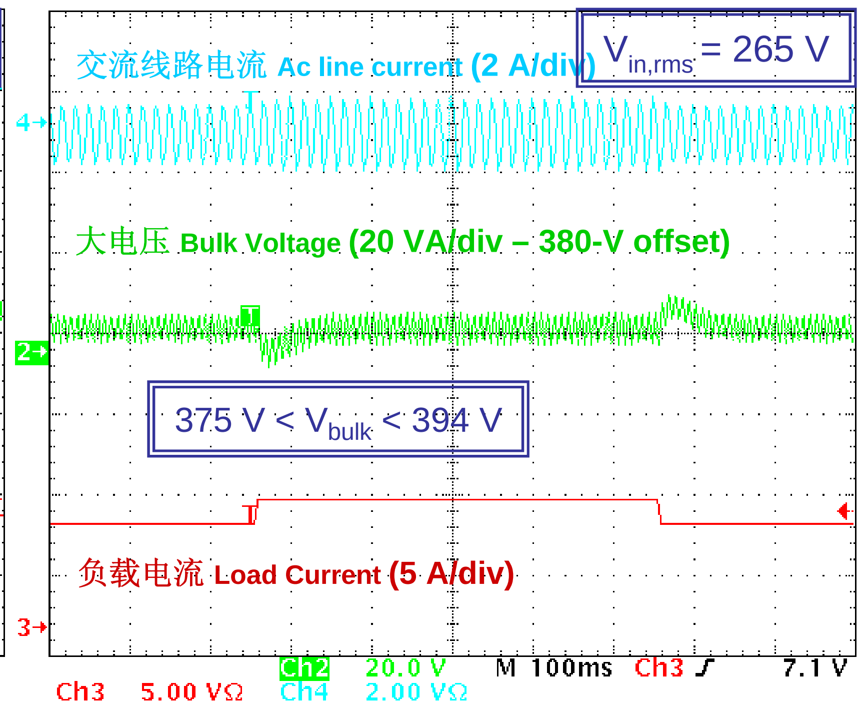
环路开路特性-中等负载Open Loop Characteristic – Mid Load



满载实验结果 Experimental Results at Full Load

- PFC段负载为19 V/7 A A 19-V / 7-A loads the PFC stage
- 下行转换器电流在6.3 A与7.7 A之间摆动(±10%)，并带有2 A/µs的斜坡
  The downstream converter swings between 6.3 A and 7.7 A (+/-10%) with a 2-A/µs slope

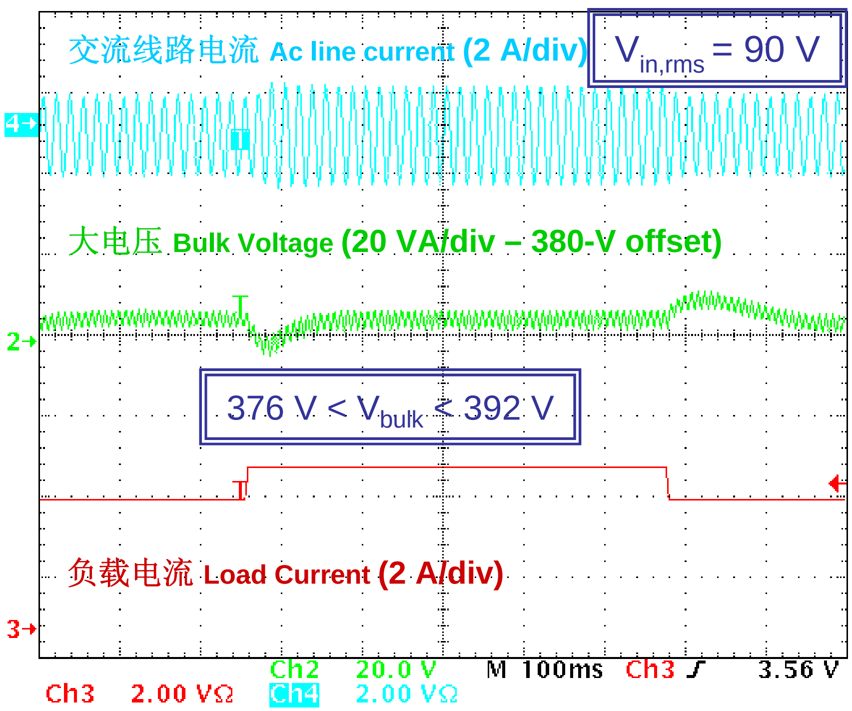


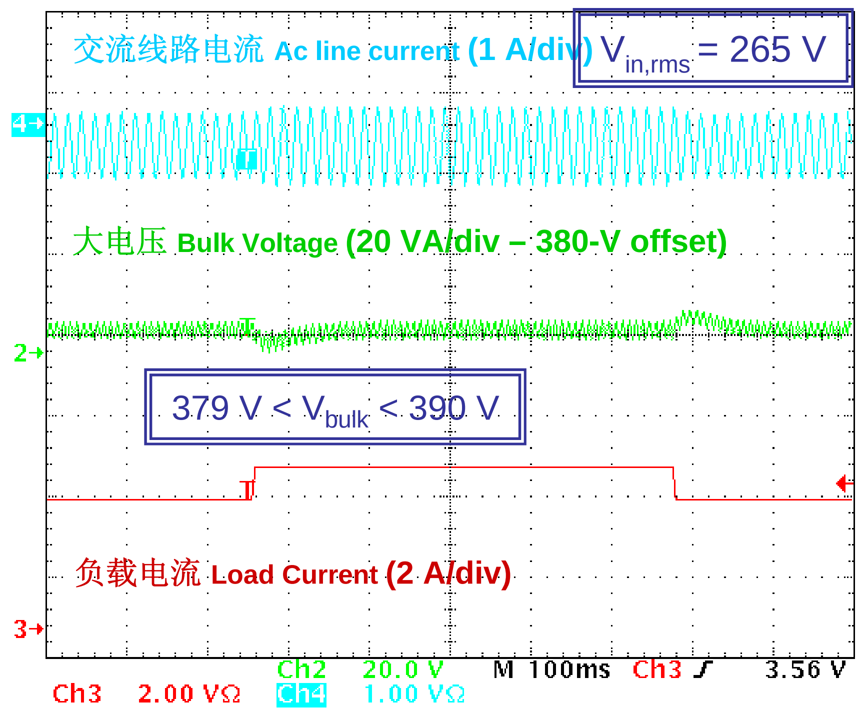


- 高线路输入、较大带宽降低V_{bulk}漂移，加速输出电压恢复 The high-line, larger bandwidth reduces the V_{bulk} deviations and speeds-up the output voltage recovery

中等负载实验结果 Experimental Results at Medium Load

- PFC段负载为19 V/7 A A 19-V / 7-A loads the PFC stage
- 下行转换器电流在3.1 A与3.9 A之间摆动(±10%)，并带有2 A/μs的斜坡
  The downstream converter swings between 3.1 A and 3.9 A (+/-10%) with a 2-A/μs slope

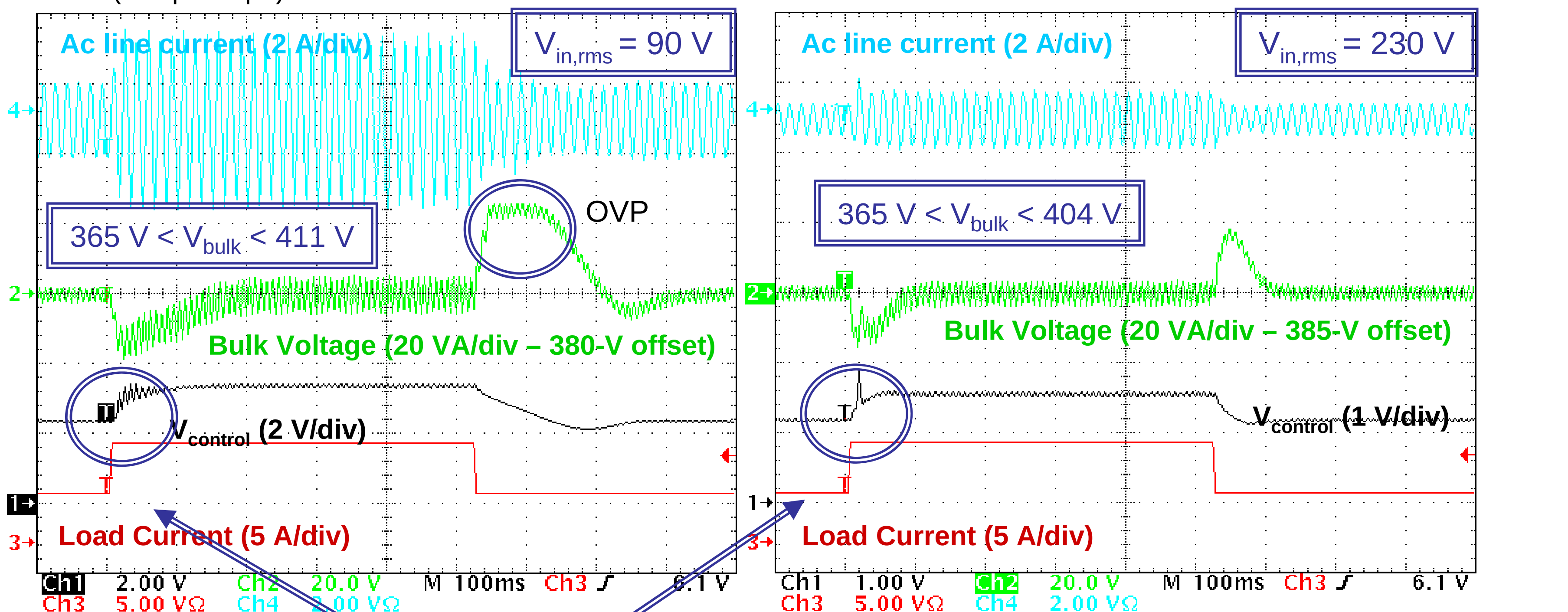




- 电路仍然呈现一阶响应 The circuit still exhibits a first order response

陡然负载改变 Abrupt Load Changes

- PFC段负载为19 V/7 A A 19-V / 7-A loads the PFC stage
- 下行转换器电流在7.0 A至3.5 A间摆(2 A/µs斜坡) The downstream converter swings from 7.0 A to 3.5 A (2-A/µs slope)



NCP1605(FCCrM)、NCP1654(CCM)和NCP1631(交错式)中应用了动态响应增强器，在出现较大欠冲时加速环路反应速度 The dynamic response enhancer speeds-up the loop reaction in case of a large undershoot Implemented in NCP1605 (FCCrM), NCP1654 (CCM) and NCP1631 (Interleaved)

- 动态响应增强器减少低交流线路输入时的欠冲 The dynamic response enhancer reduces the undershoot at low line

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总结 Summary

- 以基于NCP1605的PFC为例，阐述了PFC补偿的一般考虑因素
  General considerations were illustrated by the case of NCP1605-driven PFC stages
- 能够轻易导出升压PFC的小信号模型
  A small signal model of PFC boosts can be easily derived
- 建议的方法与PFC工作模式无关
  The proposed method is independent of the operating mode
- 推荐第2类补偿 A type-2 compensation is recommended
- 如果没有应用前反馈，环路带宽和相位余量跟线路幅度的函数变化 If no feed-forward is implemented, the loop bandwidth and phase margin vary as a function of the line magnitude
- 交越频率不跟随负载的函数而变化
  The crossover frequency does not vary as a function of the load
- 即使PFC段为电源馈电(负阻抗)，也能使用电阻型负载-参见备份资料
  A resistive load can be used for the computation even if the PFC stage feeds a power supply (negative impedance) – See back-up

For More Information

- View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com

- View reference designs, design notes, and other material supporting the design of highly efficient power supplies at www.onsemi.com/powersupplies