ON Semiconductor®

Analysis and Design of Quasi-Square Wave Resonant Converters

Agenda

1. Quasi-Resonant (QR) Generalities
2. Limiting the free-running frequency
3. Calculating the QR inductor
4. Choosing the Power Components
5. Predicting the Losses of a QR Power Supply
6. Synchronous Rectification
7. Loop Compensation
8. NCP1380, our future QR controller

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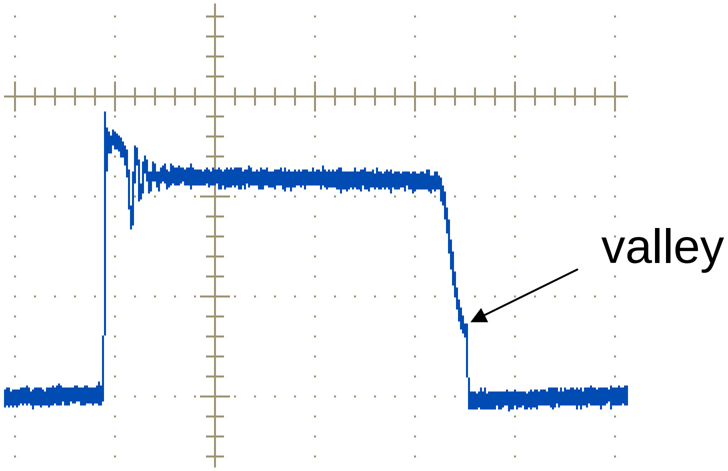
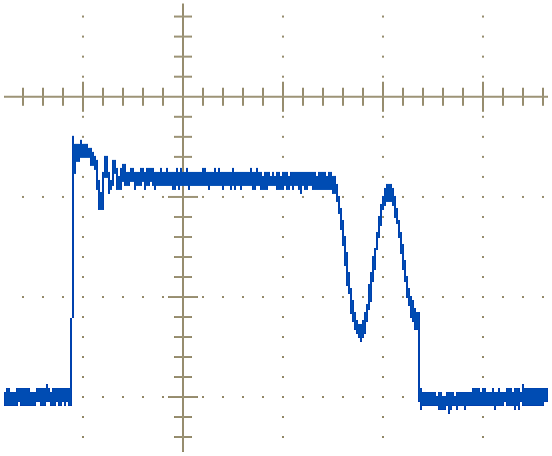
What is Quasi-Square Wave Resonance ?

❑ MOSFET turns on when $V_{DS}(t)$ reaches its minimum value.

- ➢ Minimize switching losses
- ➢ Improves the EMI signature



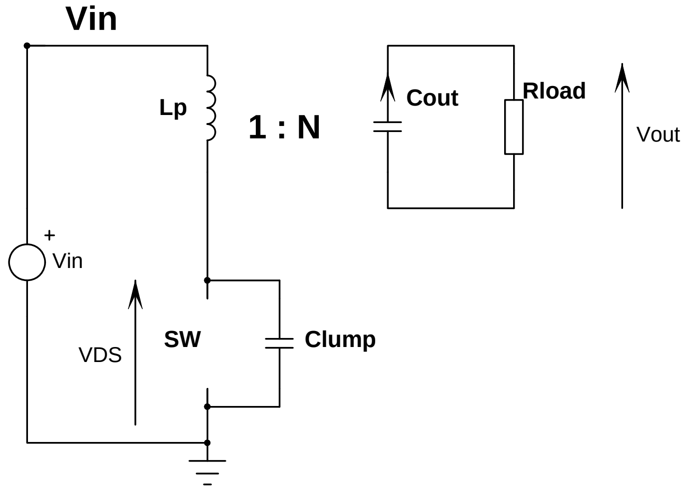
MOSFET turns on in first valley

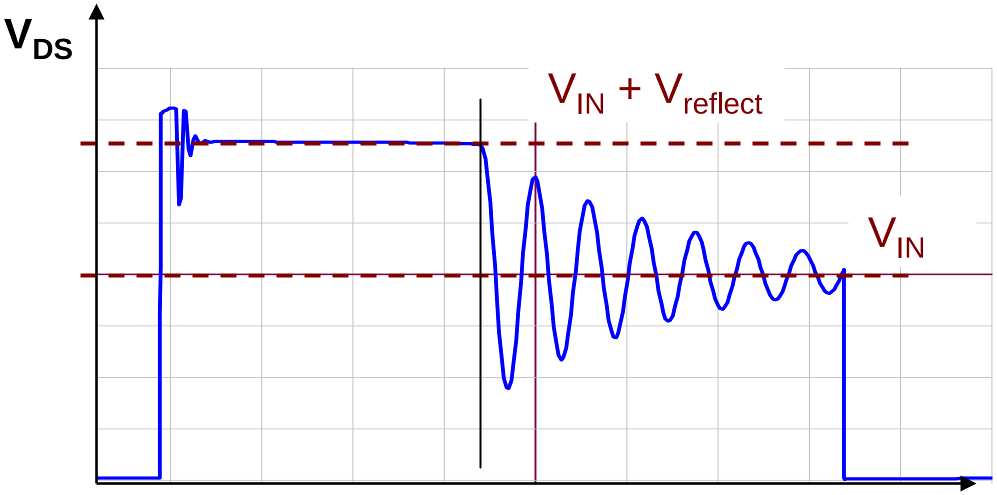


MOSFET turns on in second valley

Quasi-Resonant Operation

- In DCM, V_{DS} must drop from (V_{IN} + $V_{reflect}$) to V_{IN}
- Because of L_p-C_{lump} network → oscillations appear
- Oscillation half period: $t_x = \pi\sqrt{L_p C_{lump}}$





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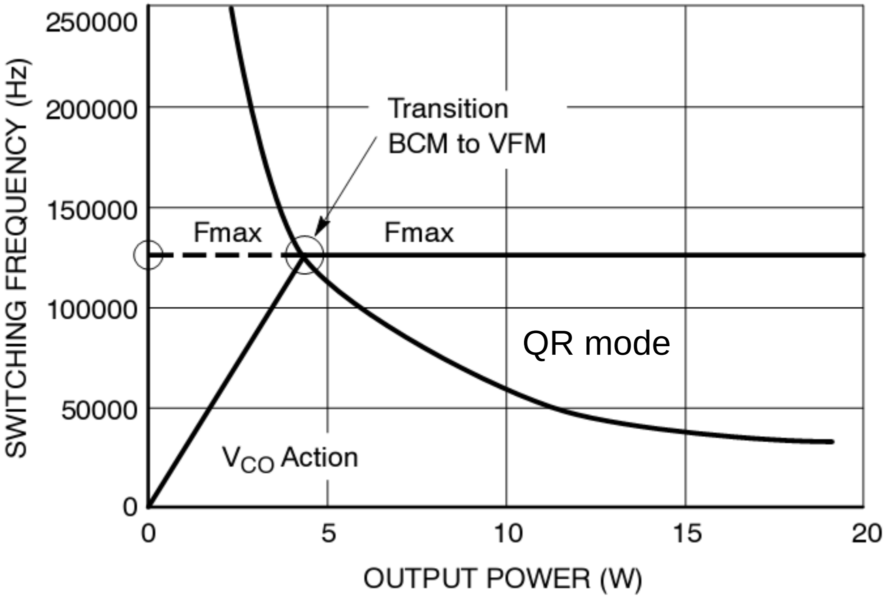
A Need to Limit the Switching Frequency

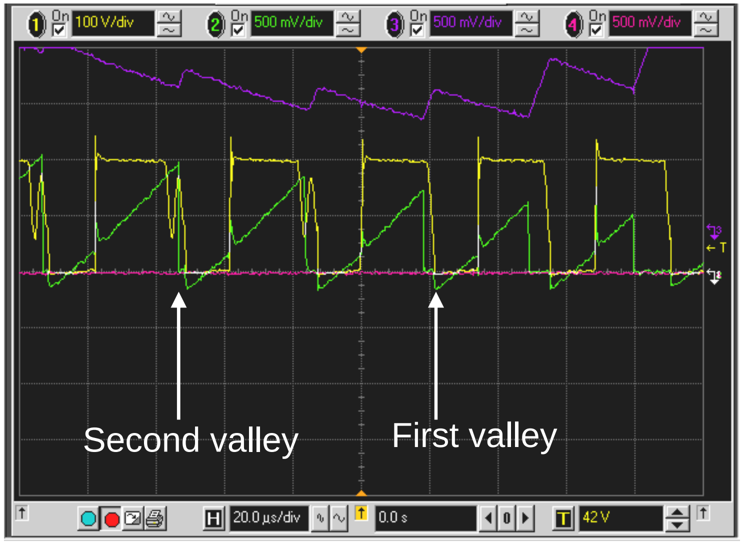
- In a self-oscillating QR, F_{sw} increases as the load decreases

➡ Higher losses at light load if F_{sw} is not limited

- 2 methods to limit F_{sw}:
  - Frequency clamp with frequency foldback
  - Changing valley with valley lockout

Frequency Foldback in QR Converters

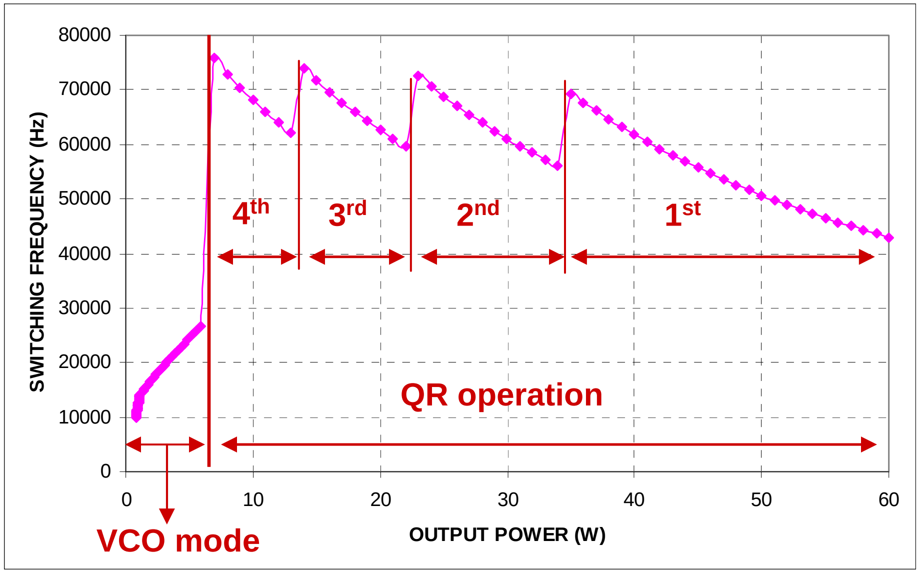




- ☐ In light load, frequency increases and hits clamp
  - ➢ Multiple valley jumps
  - ➢ Jumps occur at audible range
  - ➢ Creates signal instability

Changing Valley

- As the load decreases, the controller changes valley (1st to 4th valley in NCP1380)
- The controller stays locked in a valley until the output power changes significantly.
  - No valley jumping noise
  - Natural switching frequency limitation



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Calculating the QR Inductor

❑ Calculation steps:

1. Primary to secondary turns ratio
2. Primary and secondary peak current
3. Inductance value
4. Primary and secondary rms current

Turns Ratio Calculation

❑ Derate maximum MOSFET BV_{dss}:

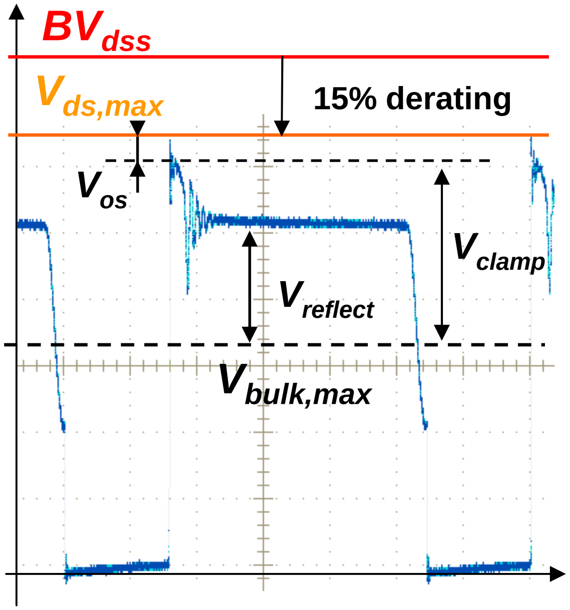
$$V_{ds,max} = BV_{dss}\boxed{k_D}$$

k_D: derating factor

❑ For a maximum bulk voltage, select the clamping voltage:

$$V_{clamp} = V_{ds,max} - V_{in,max} - \boxed{V_{os}}$$

V_{os}: diode overshoot



❑ Deduce turns ratio:

$$N_{ps} = \frac{N_s}{N_p} = \frac{k_c(V_{out} + V_f)}{V_{clamp}}$$

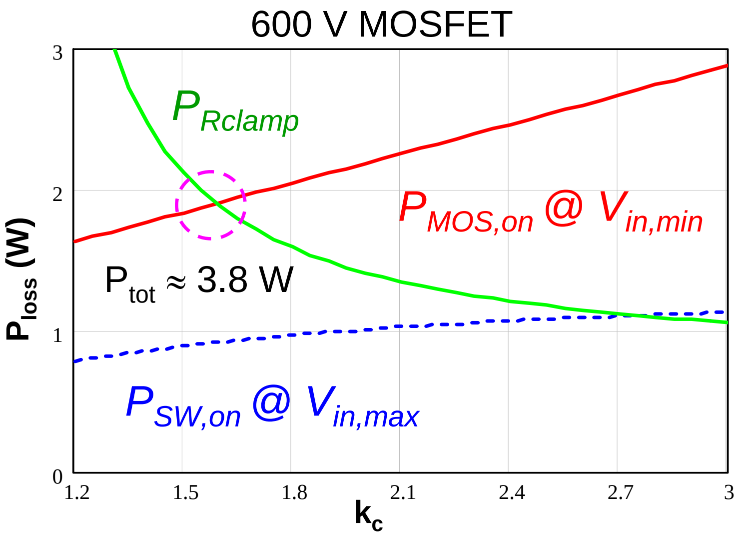
k_c: clamping coef.

$k_c = V_{clamp} / V_{reflect}$)

How to Choose k_c

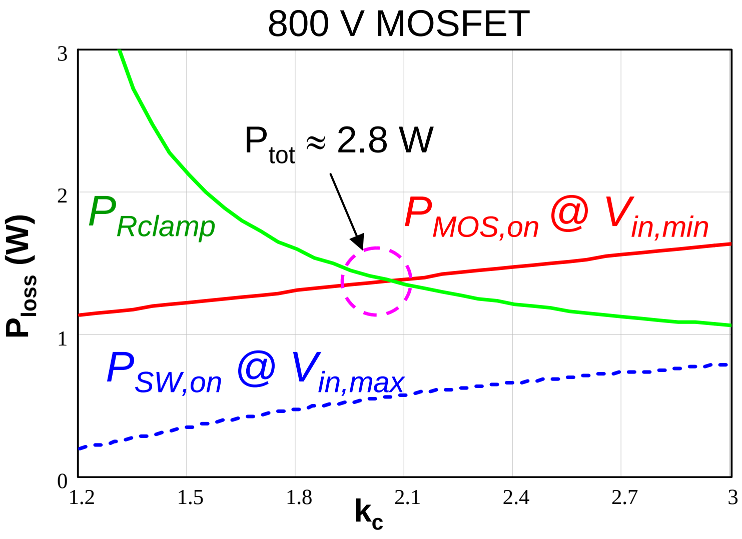
- ❑ Choose k_c to equilibrate MOS conduction losses and clamping resistor losses.

600 V MOSFET



$P_{tot} \approx 3.8$ W

800 V MOSFET



$P_{tot} \approx 2.8$ W

$$P_{Rclamp} = k_{leak} \frac{P_{out}}{\eta} \frac{k_c}{k_c - 1}$$

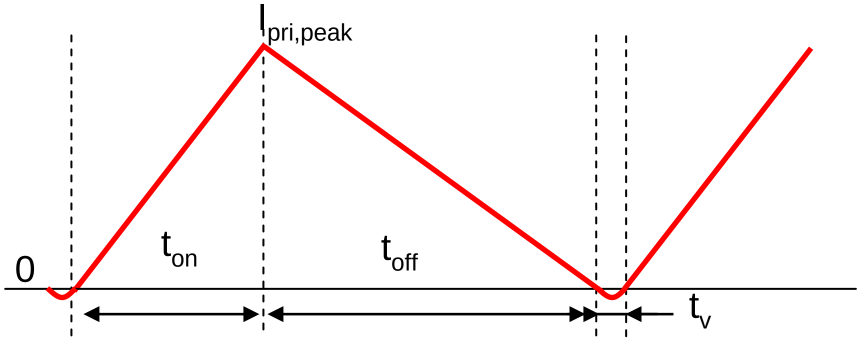
$$P_{MOS,on} = R_{dson} \frac{4P_{out}^{\ 2}}{3\eta^2 V_{in,min}} \left(\frac{1}{V_{in,min}} + \frac{k_c}{BV_{dss} k_D - V_{in,max} - V_{os}} \right)$$

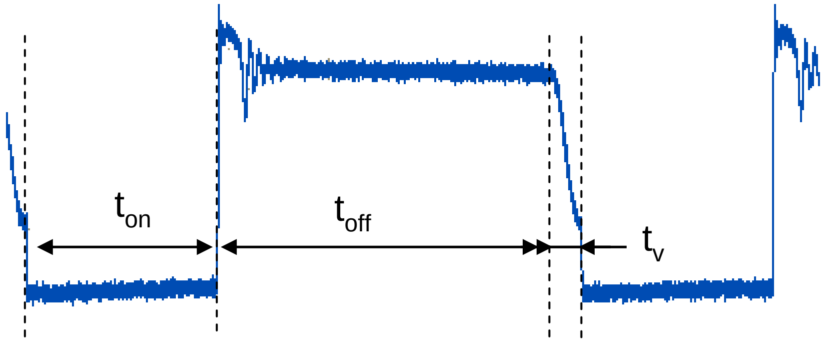
$$P_{sw,on} = \frac{1}{2} \left(V_{in,max} + \frac{BV_{dss} k_D - V_{in,max} - V_{os}}{k_c} \right)^2 C_{OSS} F_{sw,max}$$

Primary Peak Current and Inductance

- $P_{out} = \frac{1}{2} L_{pri} I_{pri,peak} F_{sw} \eta$

DCM





- $T_{sw} = \frac{I_{pri,peak} L_{pri}}{V_{in,min}} + \frac{I_{pri,peak} L_{pri} N_{ps}}{V_{out} + V_f} + \pi \sqrt{L_{pri} \boxed{C_{lump}}}$ ← C_{oss} contribution alone.

$$\boxed{I_{pri,peak} = 2 \frac{P_{out}}{\eta} \left(\frac{1}{V_{in,min}} + \frac{N_{ps}}{V_{out} + V_f} \right) + \pi \sqrt{\frac{2 P_{out} C_{lump} F_{sw}}{\eta}}}$$

$$\boxed{L_{pri} = \frac{2 P_{out}}{I_{pri,peak}{}^2 F_{sw} \eta}}$$

RMS Current

- Calculate maximum duty-cycle at maximum P_{out} and minimum V_{in}:

$$d_{max} = \frac{I_{pri,peak} L_{pri}}{V_{in,min}} F_{sw,min}$$

- Deduce primary and secondary RMS current value:

$$I_{pri,rms} = I_{pri,peak} \sqrt{\frac{d_{max}}{3}}$$

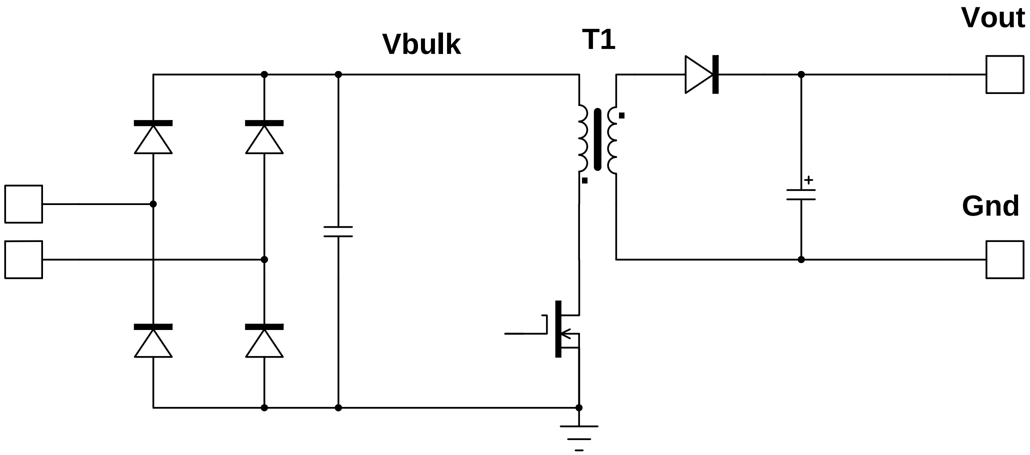
$$I_{sec,rms} = \frac{I_{pri,peak}}{N_{ps}} \sqrt{\frac{1 - d_{max}}{3}}$$

$I_{pri,rms}$ and $I_{sec,rms}$ → Losses calculation

Design Example

❑ Power supply specification:

- V_{out} = 19 V
- P_{out} = 60 W
- $F_{sw,min}$ = 45 kHz
- 600 V MOSFET
- V_{in} = 85 ~ 265 Vrms



Design Example

- Based on equations from slides 11 to 14:
  - Turns ratio: $N_{ps} = \dfrac{k_c(V_{out}+V_f)}{B_{Vdss}k_D - V_{in,max} - V_{os}} = \dfrac{1.5\times(19+0.8)}{600\times0.85-375-20} \Rightarrow \boxed{N_{ps}\approx 0.25}$
  - Peak current: $I_{pri,peak} = \dfrac{2P_{out}}{\eta}\left(\dfrac{1}{V_{in,min}}+\dfrac{N_{ps}}{V_{out}+V_f}\right)+\pi\sqrt{\dfrac{2P_{out}C_{lump}F_{sw}}{\eta}}$

    $= \dfrac{2\times60}{0.85}\left(\dfrac{1}{100}+\dfrac{0.25}{19.8}\right)+\pi\sqrt{\dfrac{2\times60\times250p\times45k}{0.85}} \Rightarrow \boxed{I_{pri,peak}=3.32\,A}$
  - Inductance: $L_{pri} = \dfrac{2P_{out}}{I_{pri,peak}{}^2F_{sw}\eta} = \dfrac{2\times60}{3.32^2\times45k\times0.85} \Rightarrow \boxed{L_{pri}=285\,\mu H}$
  - Max. duty-cycle: $d_{max} = \dfrac{I_{pri,peak}L_{pri}}{V_{in,min}}F_{sw,min} = \dfrac{3.32\times285\mu}{100}45k \Rightarrow \boxed{d_{max}=0.43}$
  - Primary rms current: $I_{pri,rms} = I_{pri,peak}\sqrt{\dfrac{d_{max}}{3}} = 3.32\sqrt{\dfrac{0.43}{3}} \Rightarrow \boxed{I_{pri,rms}=1.26A}$
  - Secondary rms current: $I_{sec,rms} = \dfrac{I_{pri,peak}}{N_{ps}}\sqrt{\dfrac{1-d_{max}}{3}} = \dfrac{3.32}{0.25}\sqrt{\dfrac{1-0.43}{3}} \Rightarrow \boxed{I_{sec,rms}=5.8\,A}$

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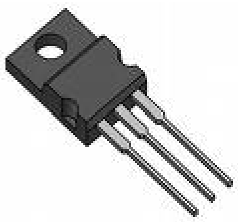
MOSFET



- TO220 package: $R_{\theta JA} = 62$ °C / W
- Ambient temperature: $T_A = 50$ °C, MOS junction temperature: $T_J = 110$ °C

- Power dissipated by TO-220 without heatsink: $$P_{TO-220} = \frac{T_J - T_A}{R_{\theta JA}} \approx 1W$$
- MOS $R_{DS(on)}$ @ $T_J = 110$ °C: $$R_{DSon120} = \frac{P_{TO-220}}{I_{pri,RMS}^{2}} = \frac{1}{1.3^2} = 0.6\Omega$$

Assume we do not want a heatsink $\xrightarrow{!}$ $\boxed{\text{15 A, 600 V MOSFET}}$

MOS Heatsink

- ☐ We choose a 7 A, 600 V MOS: $R_{DS(on)120}$ = 1.2 Ω, $R_{DS(on)25}$ = 0.6 Ω

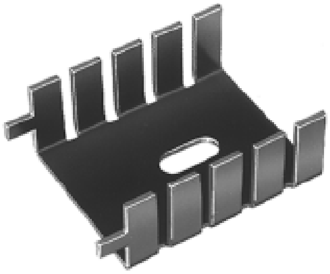
$\uparrow T_j$

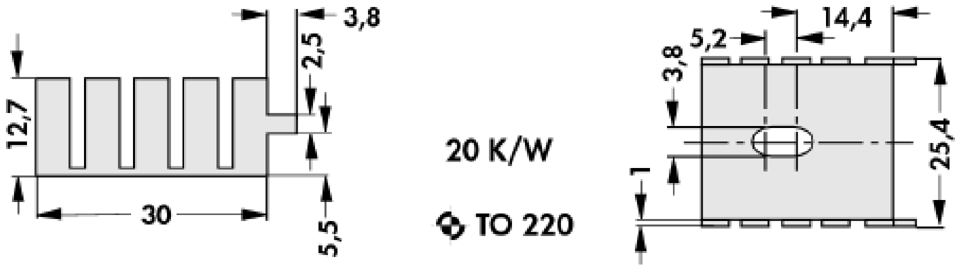
- MOS conduction losses:

$$P_{cond} = R_{DS(on)120} I_{pri,rms}^{\;2} = 1.2 \times 1.26^2 = \boxed{1.9W}$$

- Thermal resistance of the heatsink:

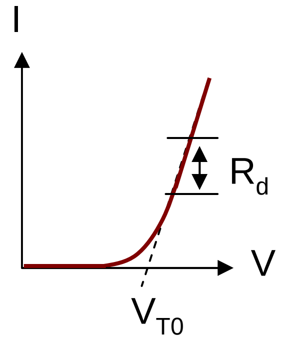
$$R_{\theta SA} = \frac{T_J - T_A}{P_{cond}} - R_{\theta JC} - R_{\theta CS} = \frac{110-50}{1.9} - 2.5 - 1.6 = 27\,°C/W$$





Output Diode

- **TO-220 package → power dissipation: 1 W**
- **MBR20200**: V_{T0} = 0.60 V, R_d = 20 mΩ



➡ Diode conduction losses:

$$P_{diode} = V_{T0} I_{out} + R_d I_{sec,rms}{}^2$$

$$P_{diode} = 0.60 \times 3.2 + 0.02 \times 5.8^2 = \boxed{2.60\,W}$$

➡ Heatsink:

$$R_{\theta SA} = \frac{T_J - T_A}{P_{cond}} - R_{\theta JC} - R_{\theta CS} = \frac{110-50}{2.6} - 2.0 - 1.6$$

$$R_{\theta SA} \approx 19\,°C/W$$

Output Capacitor Selection

- ☐ Maximum output voltage ripple: $V_{ripple} = 2\% V_{out} = 0.38$ V

➡ Maximum ESR of output capacitor:

$$R_{Cout} \le \frac{V_{ripple}}{I_{sec,peak}} = \frac{0.38}{13.2} \approx \boxed{30\,\text{m}\Omega}$$

➡ RMS current circulating in C_{out}:

$$I_{Cout,RMS} = \sqrt{I_{sec,rms}{}^2 - I_{out}{}^2} = \sqrt{5.8^2 - 3.2^2} \approx \boxed{4.83\,\text{A}}$$

Two 1200-µF capacitors (3.2 Arms, 13 mΩ / capacitor)

➡ Losses in C_{out}:

$$P_{Cout} = R_{Cout} I_{Cout,RMS}{}^2 = 6.5m \times 4.83^2 = \boxed{0.15W}$$

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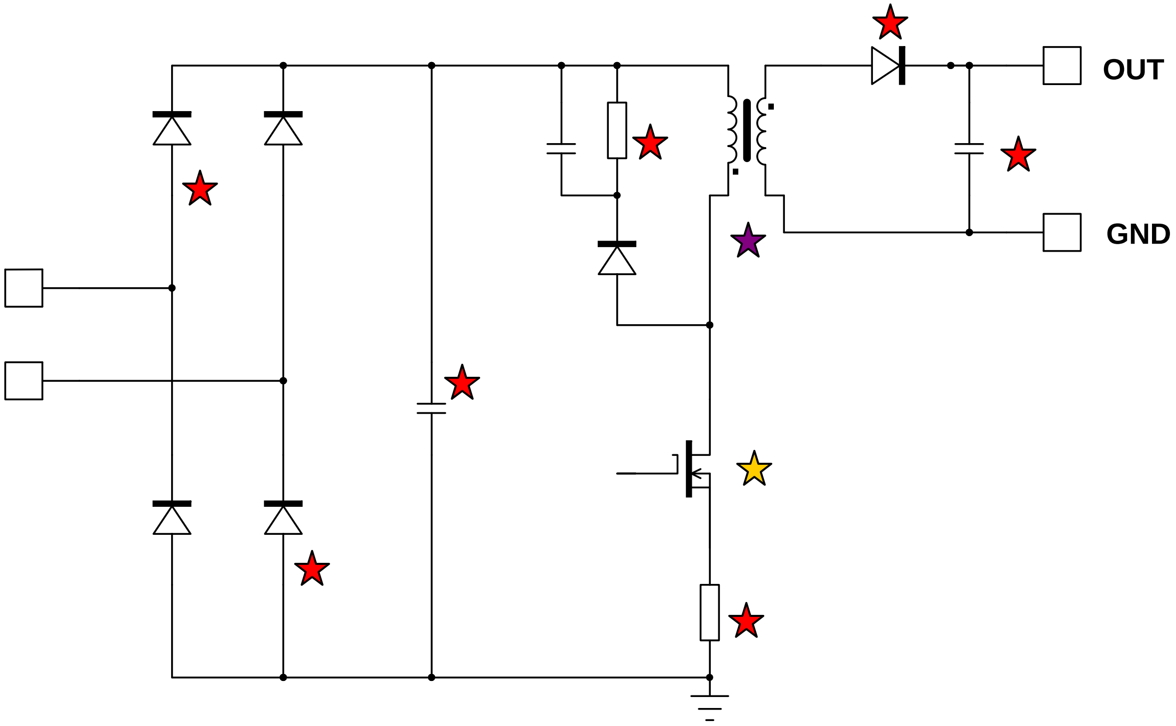
Origin of Losses



- ★ Conduction losses in ESR of capacitor, diodes, clamp resistor, sense resistor
- ☆ Conduction and switching losses in MOSFET
- ★ Copper and core losses in inductor

Switching Losses at Turn-On

- ☐ Traditional approach:

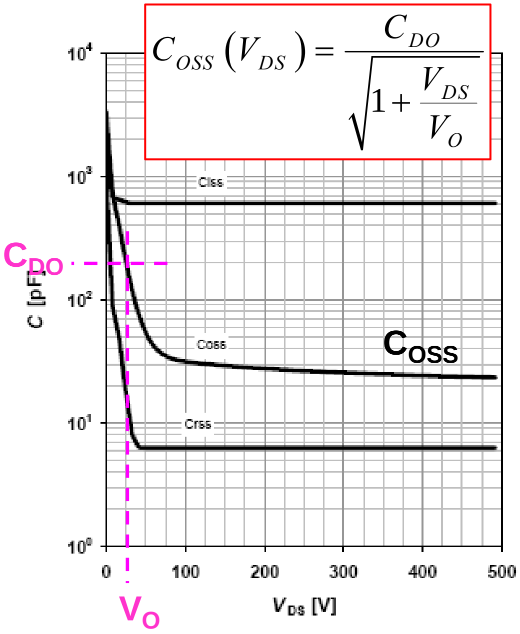
$$P_{sw,on} = \frac{1}{2} C_{OSS} \left(V_{in,min} - \frac{V_{out} + V_f}{N_{ps}} \right)^2 F_{sw}$$

$$= \frac{1}{2} 200p \left(100 - \frac{19 + 0.8}{0.25} \right)^2 45k = 2\,\mathrm{mW}$$

- ☐ Use the **variable** capacitor for losses calculation:

$$P_{sw,on} = \frac{2}{3} \left(V_{in,min} - \frac{V_{out} + V_f}{N_{ps}} \right)^{\frac{3}{2}} C_{DO} \sqrt{V_O} F_{sw}$$

$$= \frac{2}{3} \left(100 - \frac{19 + 0.8}{0.25} \right)^{3/2} 200p \sqrt{25}\, 45k = \boxed{3.6\,\mathrm{mW}}$$



$$C_{OSS}(V_{DS}) = \frac{C_{DO}}{\sqrt{1 + \frac{V_{DS}}{V_O}}}$$

Losses are negligible!

Bulk Capacitor Losses

- ☐ Power losses caused by ac current in the bulk capacitor ESR (350 mΩ)

$$P_{bulk} = R_{bulk} I_{bulk,rms}^{2}$$

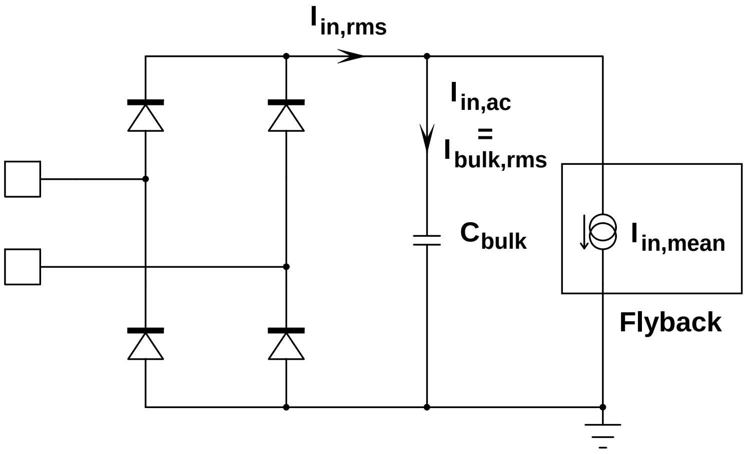
$$I_{bulk,rms} = I_{in,mean}\sqrt{\frac{2}{3F_{line}t_c} - 1}$$

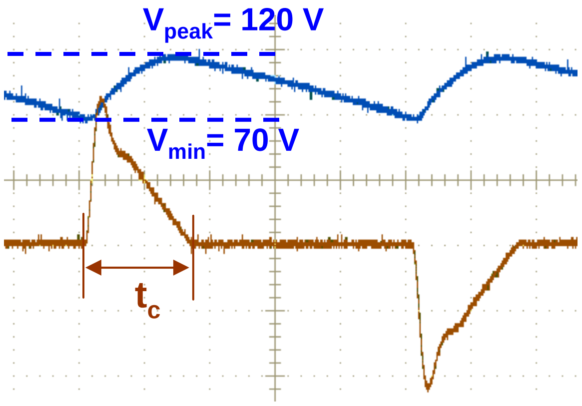
Conduction time of diode bridge

$$t_c = \frac{1}{4F_{line}} - \frac{\arcsin\left(\frac{V_{min}}{V_{peak}}\right)}{2\pi F_{line}} = 3ms$$

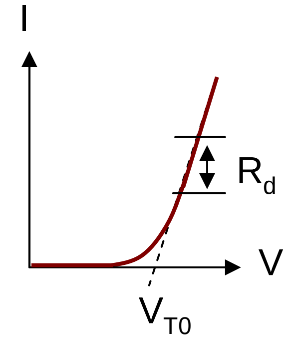
➡ $$I_{bulk,rms} = 0.70\sqrt{\frac{2}{3\times 50\times 3m} - 1} = 1.3A$$

➡ $$P_{bulk} = 350m\times 1.3^2 = \boxed{0.59W}$$





Diode Bridge Losses



- ☐ KBU4K
- ☐ From datasheet curves: V_{T0} = 0.70 V , R_d = 70 mΩ
- ☐ There are two diodes conducting at the same time.
- ☐ Two diodes always conduct during half a cycle:

$$P_{diodes} = 2\left(V_{T0}\frac{I_{in,mean}}{2} + R_d\, I_{d,rms}^{2}\right) = 2\times\left(0.7\times 0.35 + 70m\times 1.04^{2}\right) = 640\,mW$$

$$I_{d,rms} = \frac{I_{in,mean}}{\sqrt{3F_{line}t_c}} = \frac{0.70}{\sqrt{3\times 50\times 3m}} = 1.04\,A$$

- ☐ As two diodes always conduct, over a cycle, the bridge power is:

$$P_{KBU\,4K} = 2P_{diodes} = \boxed{1.28\,W}$$

RCD Clamp Losses

- Power losses in clamping resistor:

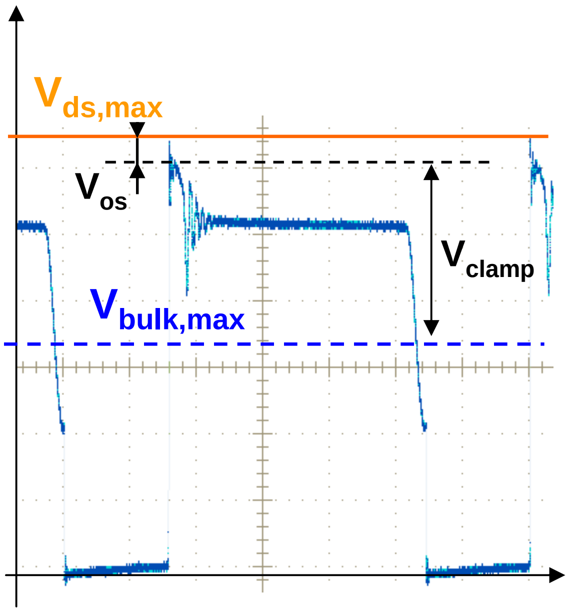
$$P_{Rclamp} = \frac{V_{clamp}^{\;2}}{R_{clamp}}$$

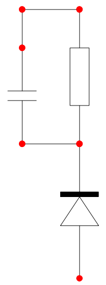
- R_{clamp} can be calculated with:

$$R_{clamp} = \frac{2V_{clamp}\left(V_{clamp} - \dfrac{V_{out}+V_f}{N_{ps}}\right)}{F_{sw}L_{leak}I_{peak}^{\;2}}$$

$$R_{clamp} = \frac{2\times 120\left(120 - \dfrac{19+0.8}{0.25}\right)}{45k\times 2.8\mu\times 3.32^2} = 7\,k\Omega \Rightarrow R_{clamp} = 7.3\,k\Omega$$

$$P_{Rclamp} = \frac{120^2}{7.3k} \approx \boxed{2\,W}$$

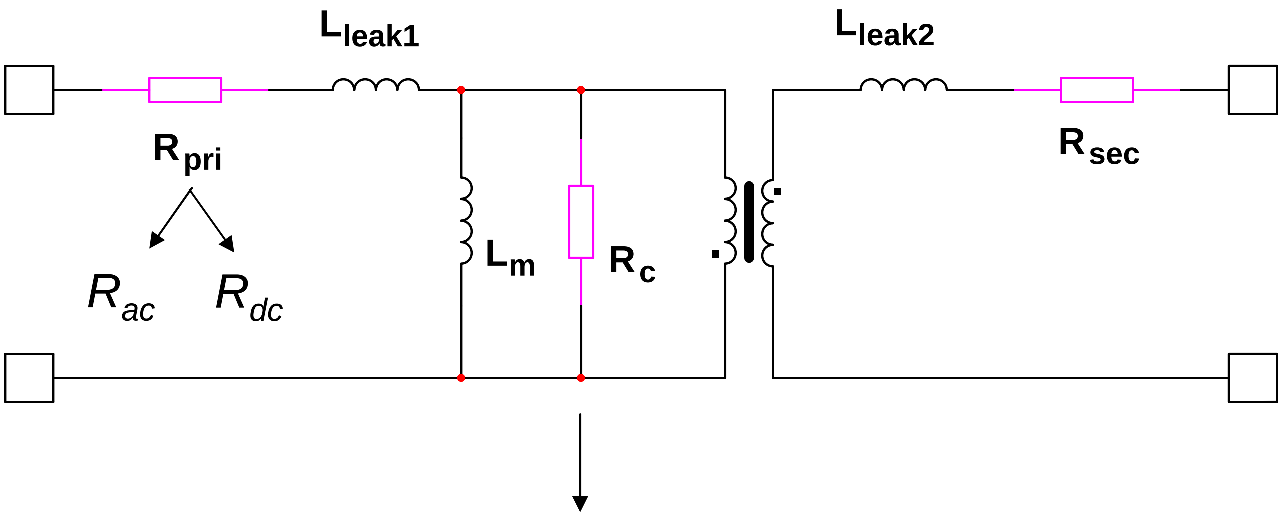




Inductor Losses

$$P_{Rpri} = R_{pri,dc} I_{in,mean}^{2} + R_{pri,ac} I_{pri,ac}^{2}$$

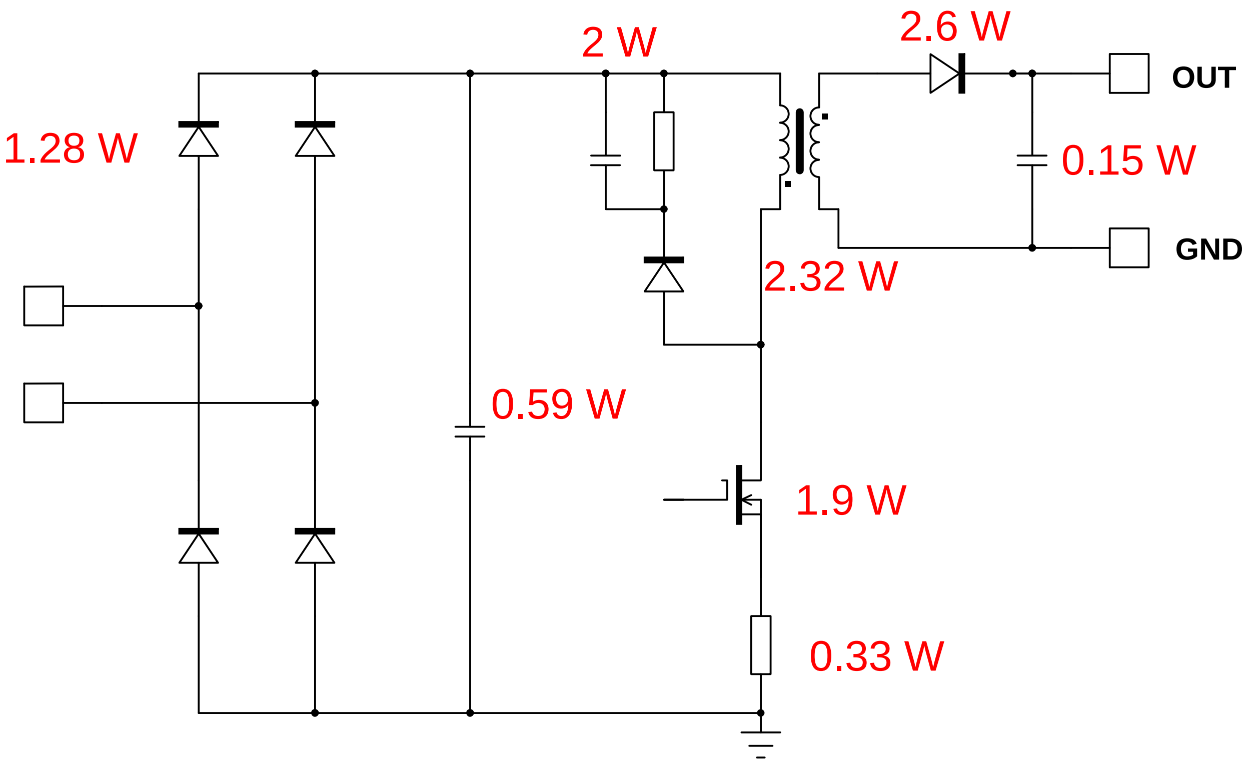
$$P_{Rsec} = R_{sec,dc} I_{out}^{2} + R_{sec,ac} I_{sec,ac}^{2}$$



Core losses:

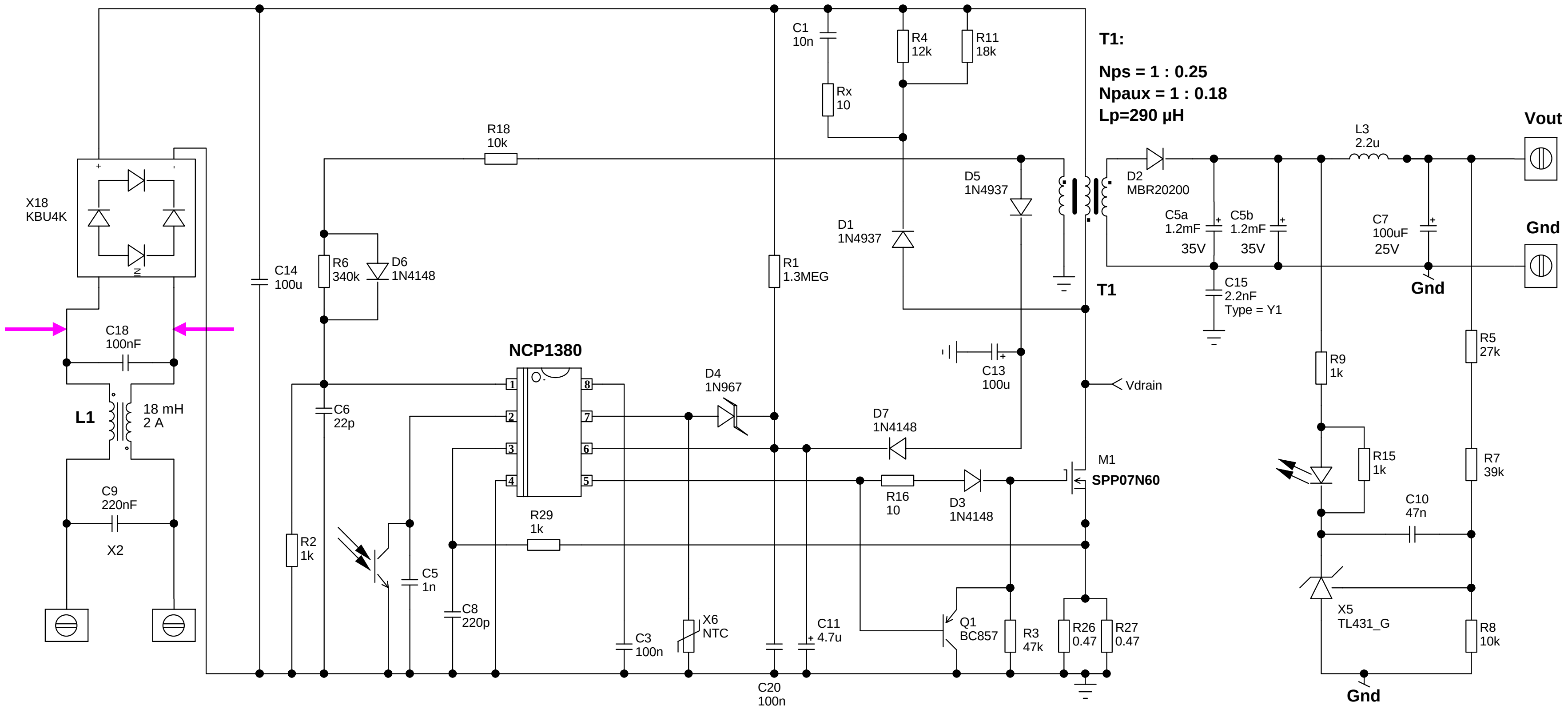
Determined from data provided by the manufacturer

Losses Summary for the 19 V / 60 W Adapter



- ☐ Total losses: $P_{loss} = 11.14W$
- ☐ Estimated efficiency: $\eta = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{60}{60 + 11.14} \approx \boxed{84.4\%}$

Comparison with Real Adapter



- ☐ Efficiency measured after the EMI filter at 85 Vrms (120 Vdc)

Measured	P_{out} = 60.1 W	P_{in} = 70.9 W	η = 84.8%
Calculated	P_{out} = 60 W	P_{in} = 71.14 W	η = 84.4%

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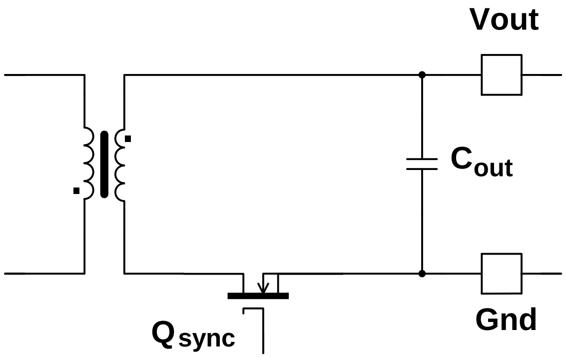
Synchronous Rectification

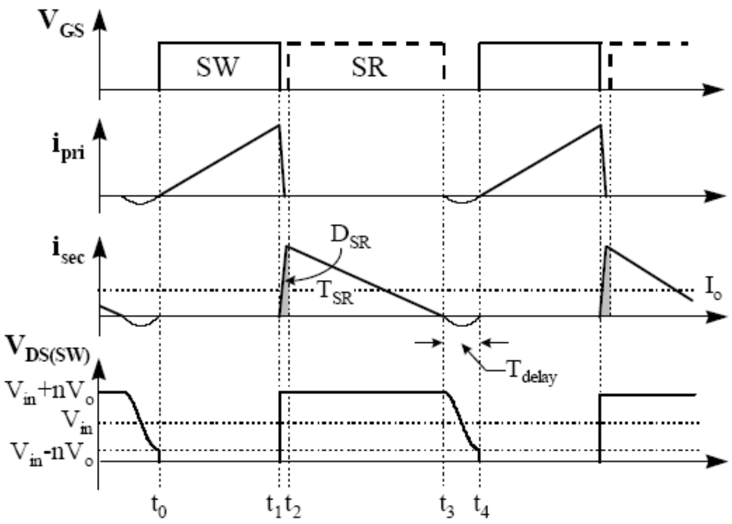
- ☐ High rms currents in secondary side → increased losses in the output diode.
- ☐ Replace the diode with a MOSFET featuring a very low $R_{DS(on)}$.

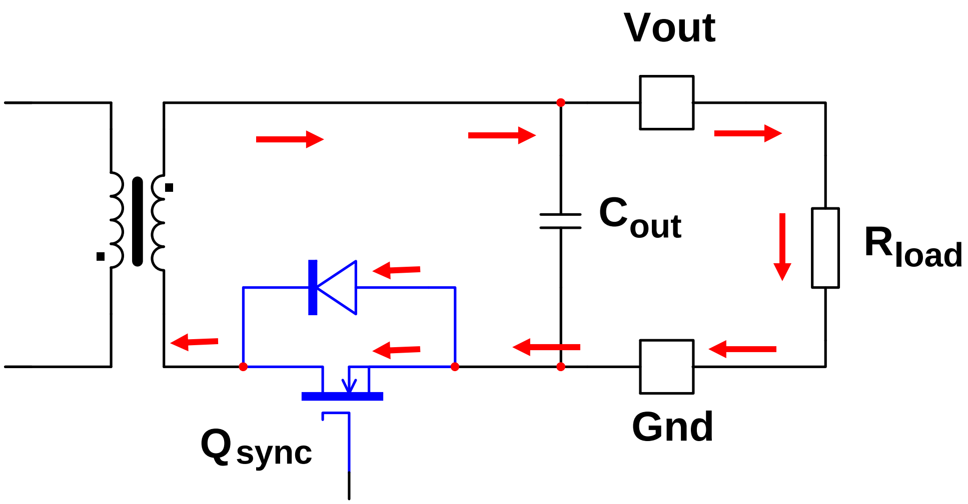
+	-
Increased efficiency	Degraded standby power



Synchronous Rectification Basics

- ❑ During (t_2-t_1), current flows into the body diode
- ❑ Minimize (t_2-t_1) duration to reduce body diode conduction.





- ❑ Body diode conducts before the MOSFET is turned-on.

➡ No switching losses

Losses in the Sync. Rect. Switch

$$\boxed{P_{Qsync} = P_{ON} + P_{Qdiode}}$$

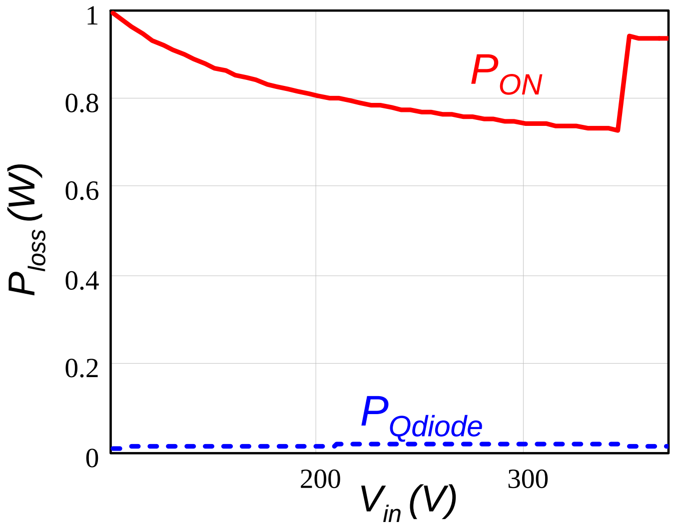
- Body diode conduction losses

$$P_{Qdiode} = V_f I_{out} F_{sw} t_{delay}$$

→ Low if t_{delay} small

- MOSFET conduction losses

$$P_{ON} = R_{DS(on)120} I_{sec,rms}{}^2$$


Body diode and MOS conduction losses for the 19 V/65 W adapter

- Losses in the Sync. Rect. switch are mainly conduction losses.

Choosing the Sync. Rect. MOSFET

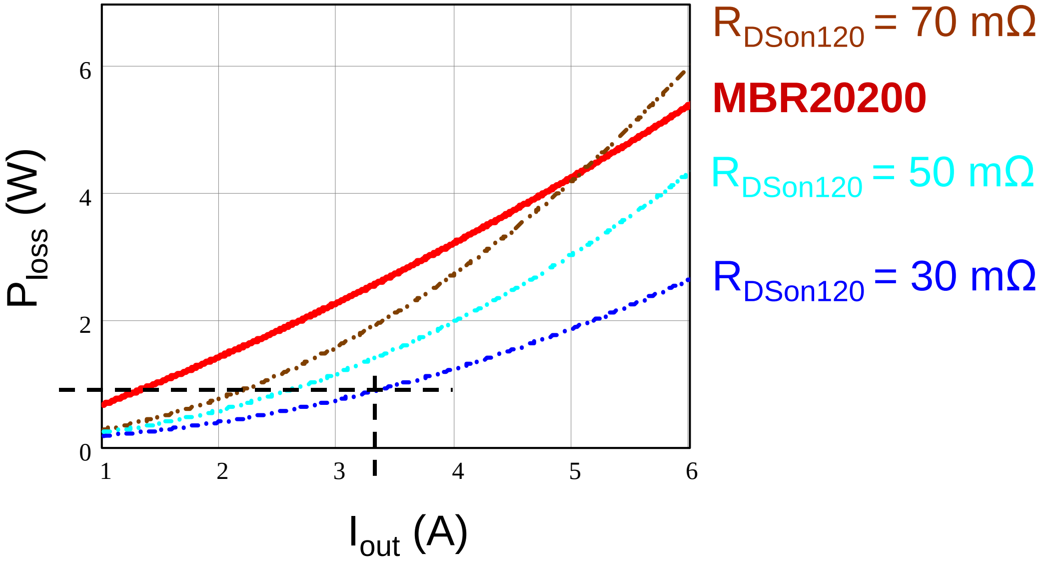
- Target around 1 W conduction losses in Sync. Rect. switch to avoid using an heatsink.

$$R_{DSon120} = \frac{1W}{I_{sec,RMS}^{2}}$$

V_{out} = 19 V

$F_{sw,min}$ = 45 kHz

Universal mains



60 W QR Sync. Rect. Calculations

☐ Body diode losses:

$$P_{Qdiode} = V_f I_{out} F_{sw} t_{delay} = 0.7 \times 3.2 \times 45000 \times 70n$$

$$P_{Qdiode} = 7\,mW$$

☐ MOSFET losses:

$$P_{ON} = R_{DS(on)120} I_{sec,rms}{}^2 = 30m \times 5.8^2$$

$$P_{ON} = 1W$$

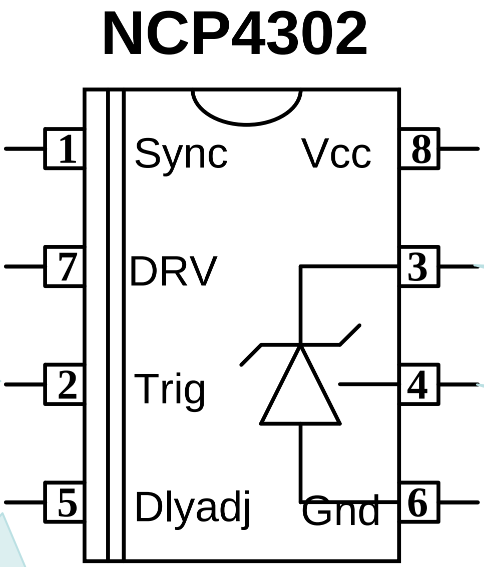
⬇

☐ Total Sync. Rect switch losses: $P_{Qsync} = 1 + 0.007 \approx \boxed{1W}$

☐ Losses into the MBR20200 diode: $\boxed{\text{2.6 W}}$

➡ Power loss saving: $\boxed{\text{1.6 W}}$

Using NCP4302



CS input connected to the drain of the MOSFET

Trigger input for CCM. Connect it to Gnd if not used.

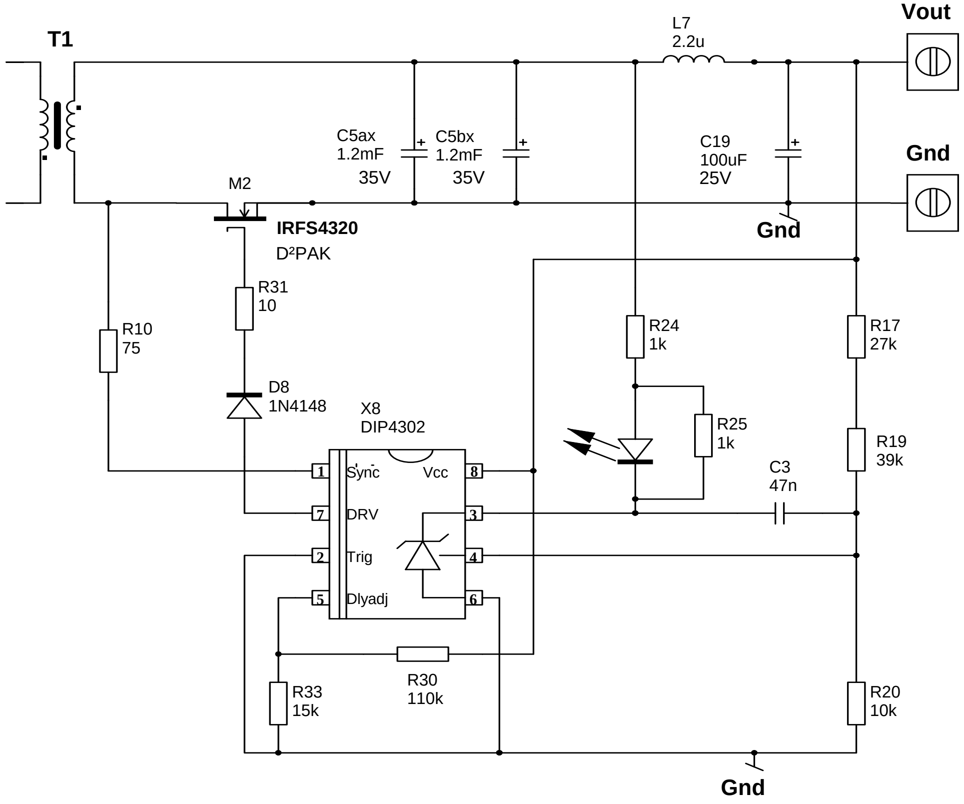
TL431 Cathode

TL431 V_{REF} input

Adjust:
- minimum **on-time** of the Sync. MOSFET
- the minimum **off-time** of the Sync. MOSFET

to be immune to drain ringing of the primary switch.

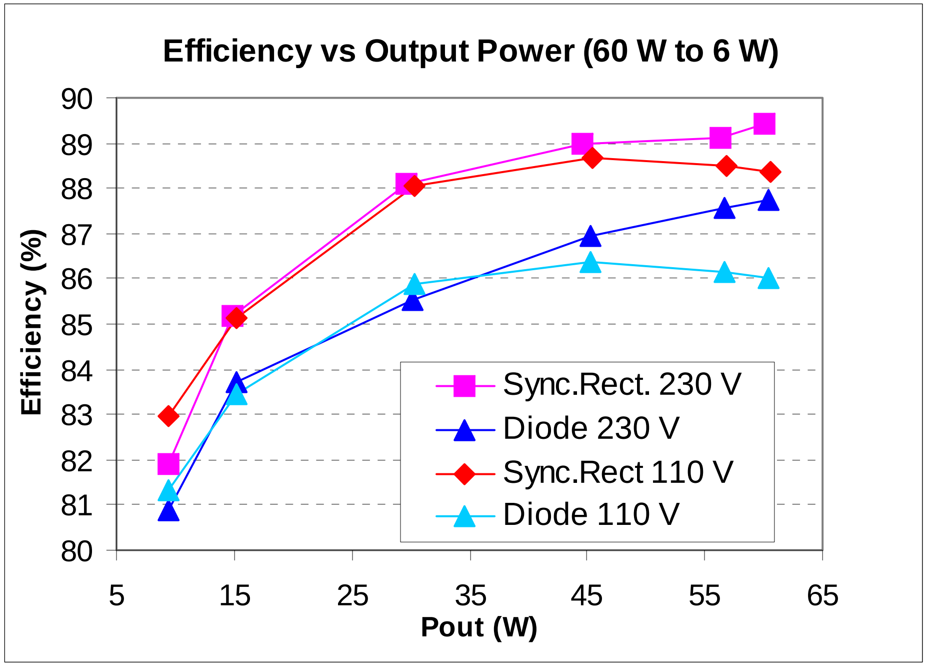
Measured Efficiency with Sync. Rect.

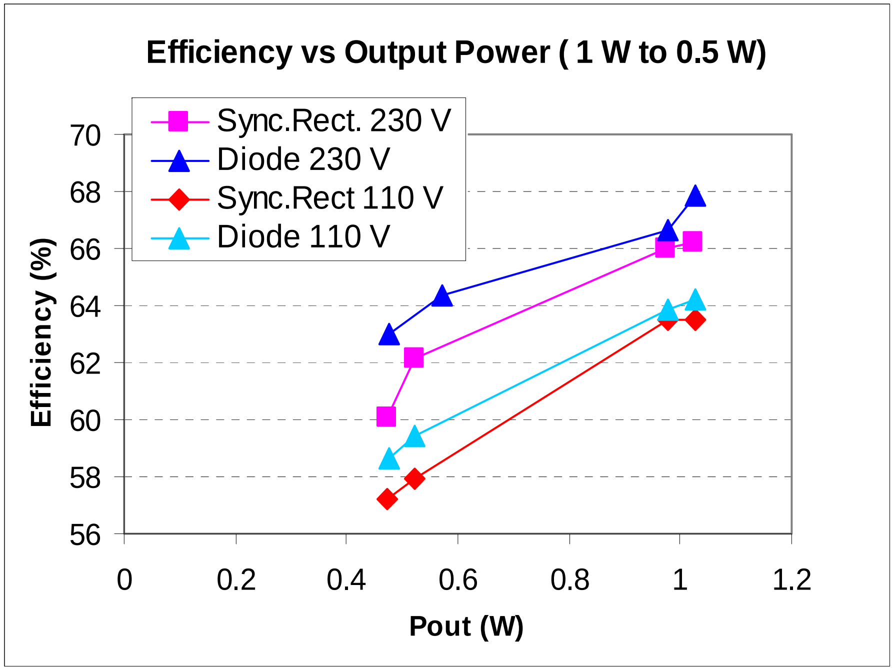


- ❑ Efficiency measured after the EMI filter at 85 Vrms

Measured	P_{out} = 60.1 W	P_{in} = 69.25 W	η = 86.8%
Calculated	P_{out} = 60 W	P_{in} = 69.54 W	η = 86.3%

Measured efficiency with Diode and Sync. Rect.


Efficiency vs Output Power (60 W to 6 W)


Efficiency vs Output Power (1 W to 0.5 W)

Standby power	230 Vrms	Diode	P_{in} = 110 mW
		Sync. Rect.	P_{in} = 140 mW
	85 Vrms	Diode	P_{in} = 90 mW
		Sync. Rect.	P_{in} = 122 mW

Agenda

1. Quasi-Resonant (QR) Generalities
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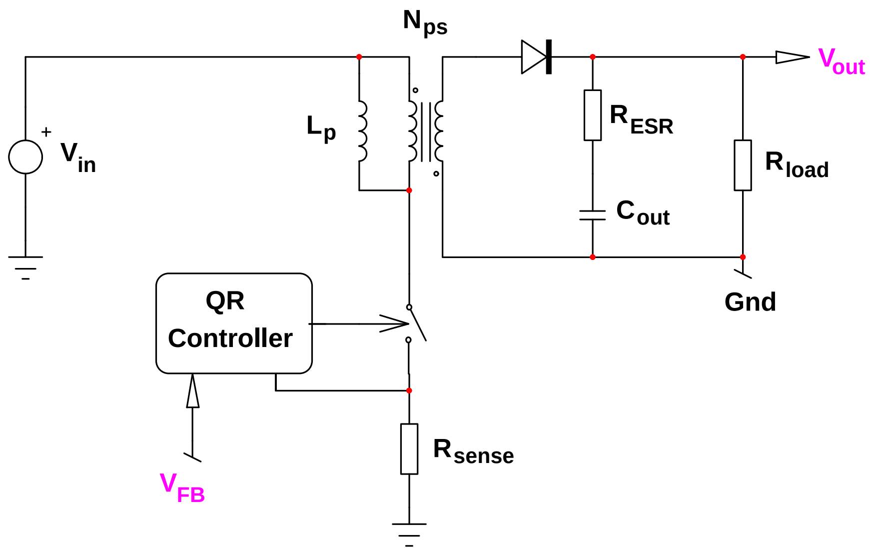
Power Stage

- Borderline Conduction Mode Approximation.
- Neglect the high frequency Right Half Plane Zero (RHPZ)

Open loop transfer function of power stage

$$\frac{\hat{v}_{out}(s)}{\hat{v}_{FB}(s)} = H(s) = \frac{\eta V_{IN} R_{load}}{2\alpha R_{sense}\left(2V_{out} + N_{ps}V_{IN}\right)}\left(\frac{R_{ESR}C_{out}\, s + 1}{(R_{eq} + R_{ESR})C_{out}\, s + 1}\right)$$



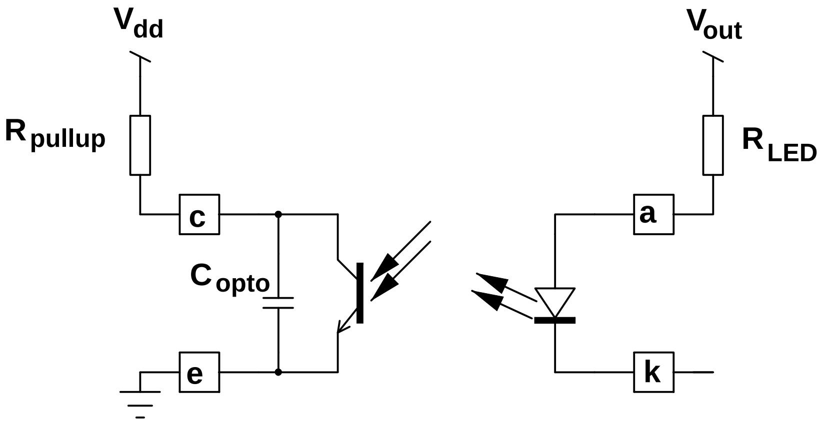
$$R_{eq} = R_{load}\frac{V_{out} + N_{ps}V_{IN}}{2V_{out} + N_{ps}V_{IN}}$$

α: internal dividing ratio between FB and CS from datasheet (typically 3 or 4)

The Optocoupler Pole

- Parasitic capacitance of optocoupler ➔ opto pole

$$s_{opto} = \frac{1}{1 + sR_{pullup}C_{opto}}$$



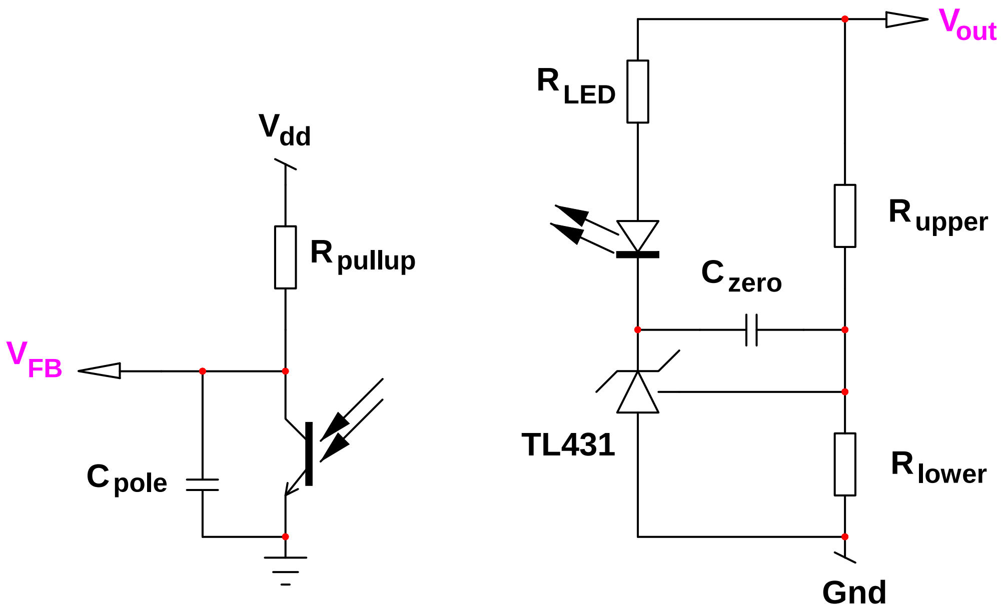
Optocoupler characterization reveals a pole at 5 kHz

- If f_{opto} close to f_c (R_{pullup} high) ➔ phase margin degradation

➡ Include the optocoupler pole in the power stage to calculate the phase shift at the crossover frequency.

$$H(s) = \frac{\eta V_{IN} R_{load}}{2\alpha R_{sense}\left(2V_{out} + N_{ps}V_{IN}\right)} \frac{\left(R_{ESR}C_{out}\,s + 1\right)}{\left((R_{eq} + R_{ESR})C_{out}\,s + 1\right)\left(R_{pullup}C_{opto}s + 1\right)}$$

Compensating the QR with TL431



$$G(s)=\frac{V_{FB}(s)}{V_{out}(s)}=\underbrace{-\mathrm{CTR}\frac{R_{pullup}}{R_{LED}}}_{\text{Mid-band gain}}\left(\frac{\overbrace{sR_{upper}C_{zero}+1}^{\text{Low frequency zero}}}{\underbrace{sR_{upper}C_{zero}}_{\text{Pole at the origin}}}\right)\underbrace{\left(\frac{1}{1+sR_{pullup}C_{pole}}\right)}_{\text{High frequency pole}}$$

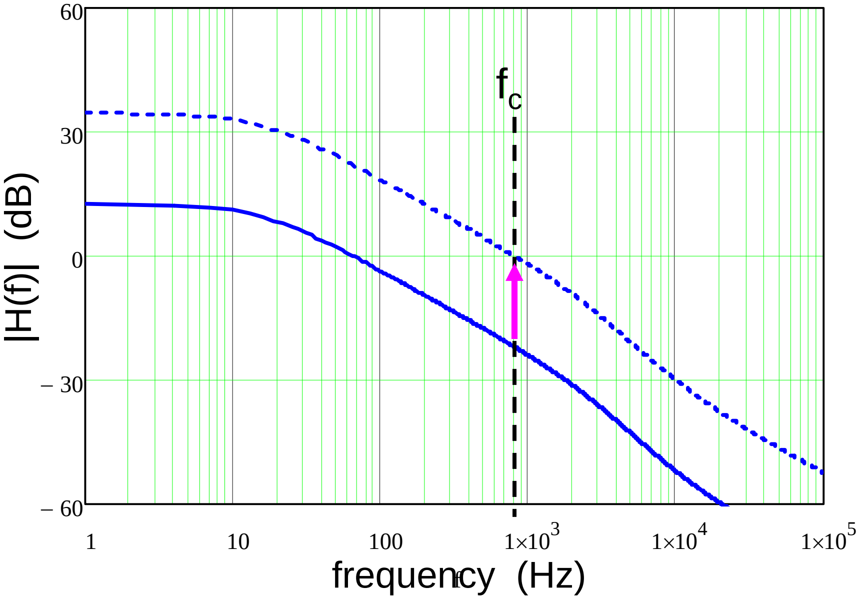
Compensating the QR Converter

- ☐ Calculate f_c according to specified V_{out} undershoot for an output step load.

$$f_c \approx \frac{\Delta I_{out}}{\Delta V_{out} C_{out} 2\pi}$$

- ☐ Calculate R_{LED} to boost the gain at crossover.

$$R_{LED} = CTR \frac{R_{pullup}}{10^{-\frac{H(f_c)}{20}}}$$



K Factor Method

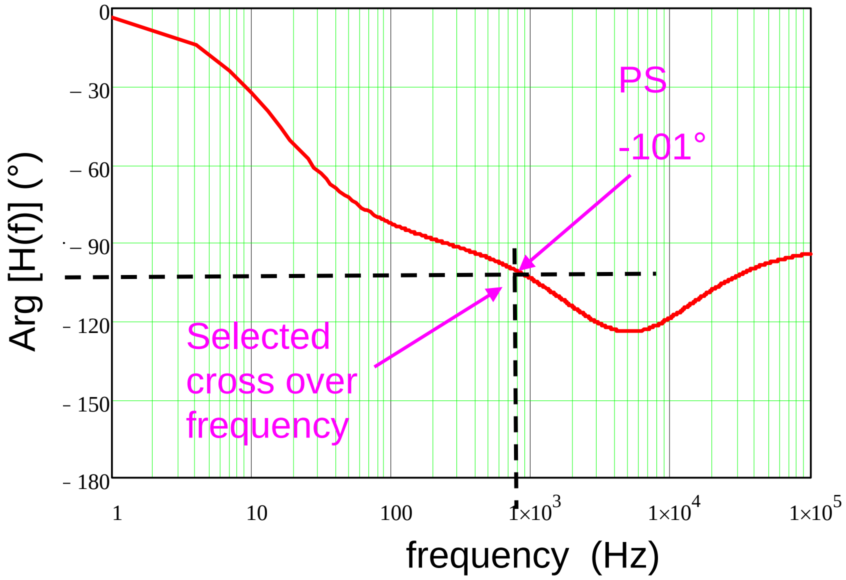
- Needed phase boost:

$$Boost = PM - PS - 90$$

Selected phase margin

Power stage phase shift

$$k = \tan\left(\frac{Boost}{2} + 45\right)$$



- Place the zero at frequency: f_c/k

$$C_{zero} = \frac{1}{2\pi R_{upper}\frac{f_c}{k}}$$

- Place the pole at frequency: $k*f_c$

$$C_{pole} = \frac{1}{2\pi R_{pullup} k f_c}$$

Loop Compensation Example

- ❑ Specification: ΔV_{out} = 230 mV for ΔI_{out} = 2.8 A

$$f_c \approx \frac{\Delta I_{out}}{\Delta V_{out} C_{out} 2\pi} = \frac{2.8}{230m \times 2.4m \times 2\pi} \Rightarrow \boxed{f_c = 800\,Hz}$$

- ❑ Calculated mid-band gain: 18.6 dB

$$R_{LED} = CTR\frac{R_{pullup}}{10^{\frac{-H(f_c)}{20}}} = 0.6\frac{18k}{10^{\frac{22}{20}}} \approx \boxed{1k\Omega}$$

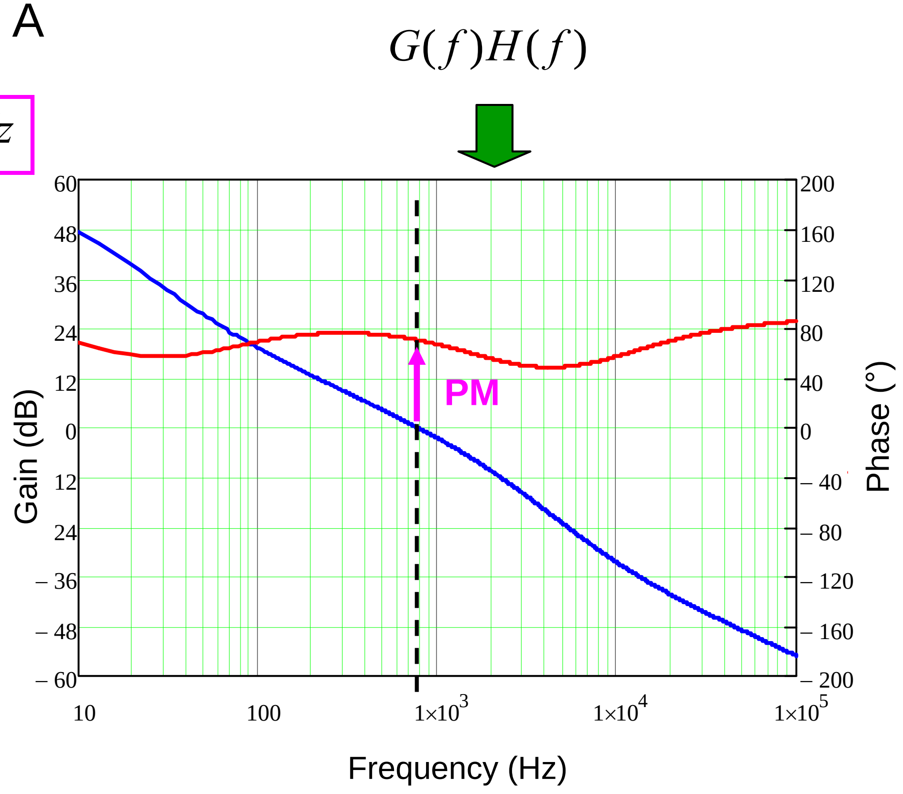
- ❑ Needed Phase Boost:

$$Boost = PM - PS - 90 = 70 - (-101) - 90 = 81^\circ$$

$$k = \tan\left(\frac{81}{2} + 45\right) \Box\, 12.5$$

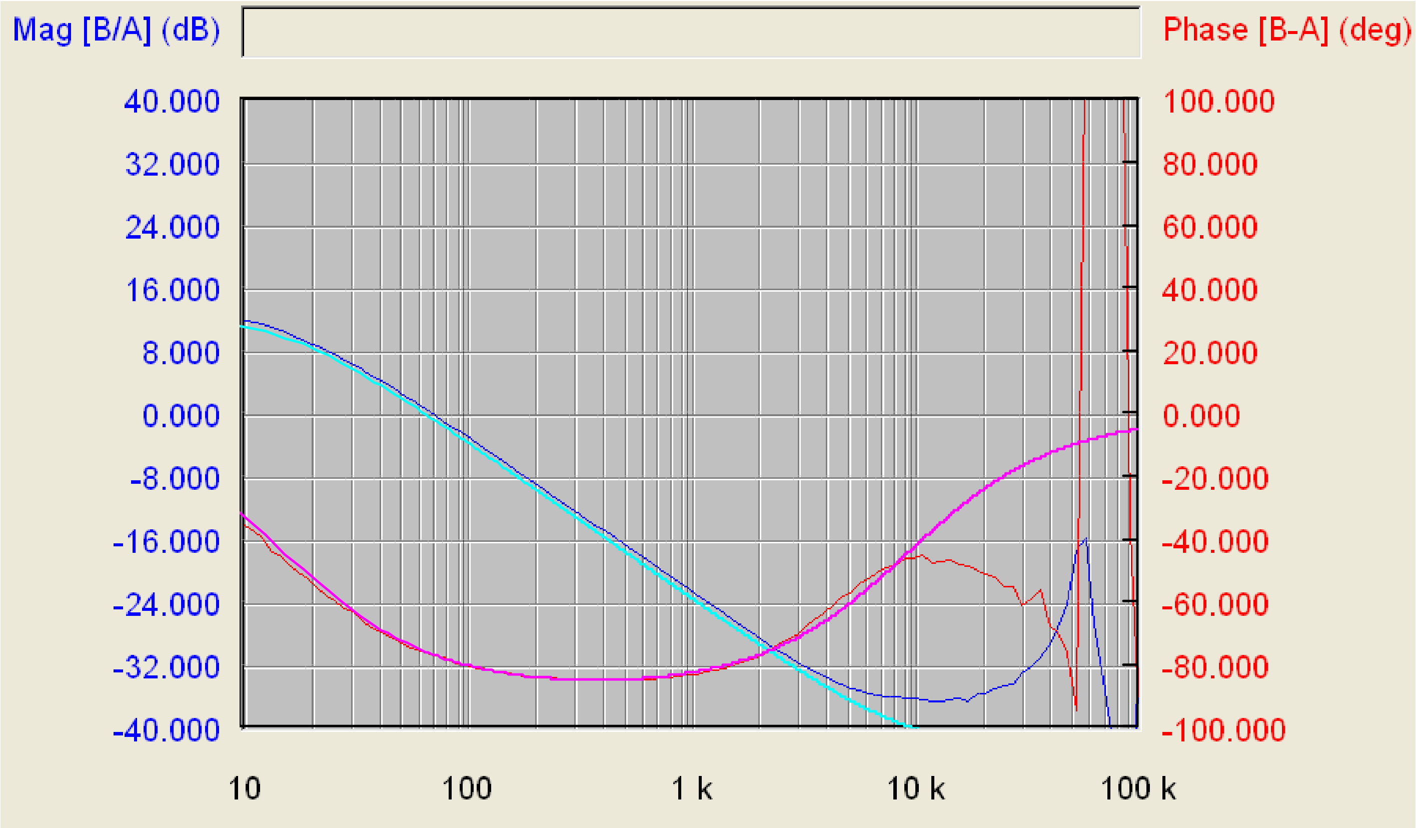
$$C_{zero} = \frac{1}{2\pi R_{upper}\frac{f_c}{k}} = \frac{1}{2\pi \times 66k \times \frac{800}{12.5}} = 38\,nF \Rightarrow \boxed{C_{zero} = 47\,nF}$$

$$C_{pole} = \frac{1}{2\pi R_{pullup} k f_c} = \frac{1}{2\pi \times 18k \times 12.5 \times 800} = 0.8\,nF \Rightarrow \boxed{C_{pole} = 1\,nF}$$



Measurement versus Calculation

- ☐ Power stage gain and phase



-- Measured gain

-- Measured phase

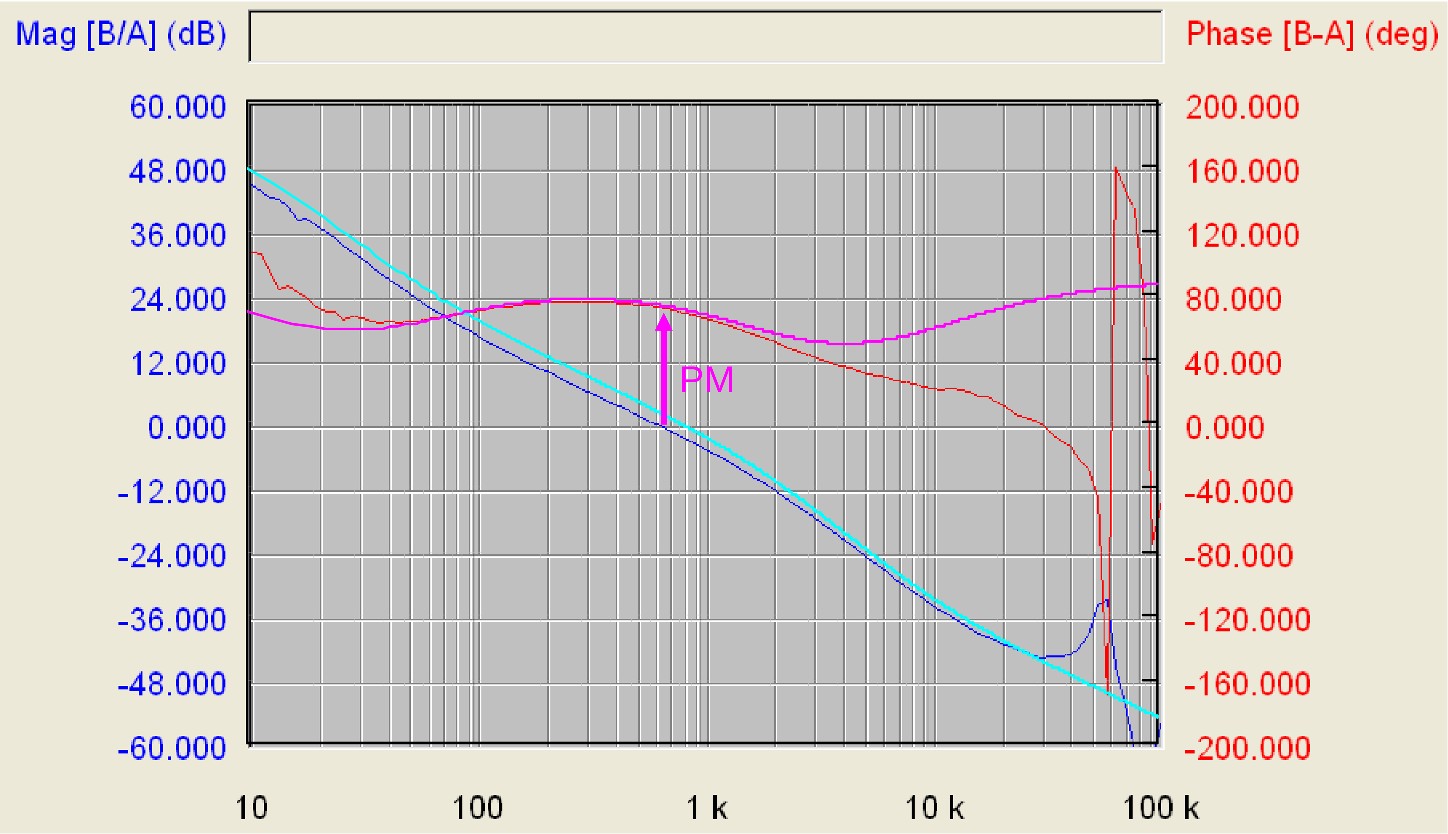
-- Calculated gain

-- Calculated phase

The RHPZ is around 20 kHz.

Measurement versus Calculation

- Loop gain and phase



-- Measured gain

-- Measured phase

-- Calculated gain

-- Calculated phase

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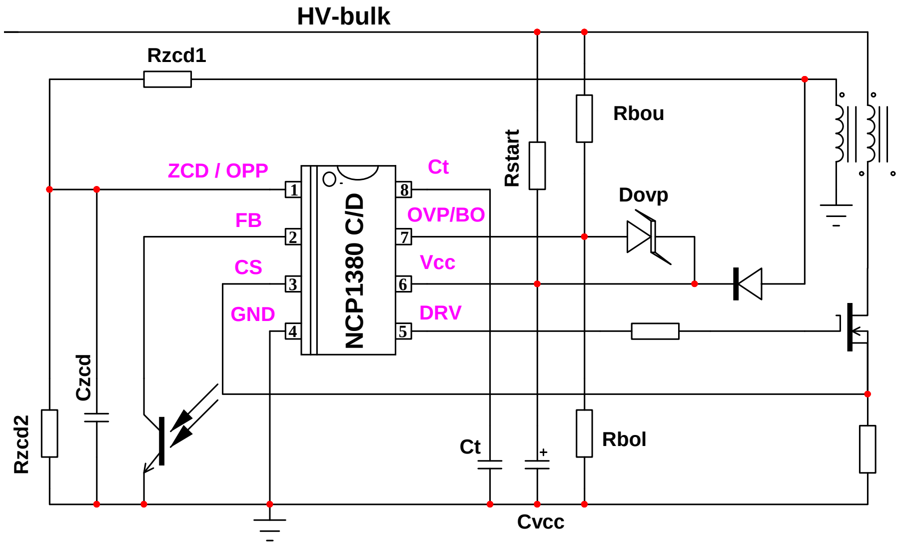
NCP1380 Features

- Operating modes:
  - QR current-mode with valley lockout for noise immunity
  - VCO mode in light load for improved efficiency
- Protections
  - Over power protection
  - Soft-start
  - Short circuit protection
  - Over voltage protection
  - Over temperature protection
  - Brown-Out



- Sampling date: end of January 09
- Mass production: end of Feb. 09

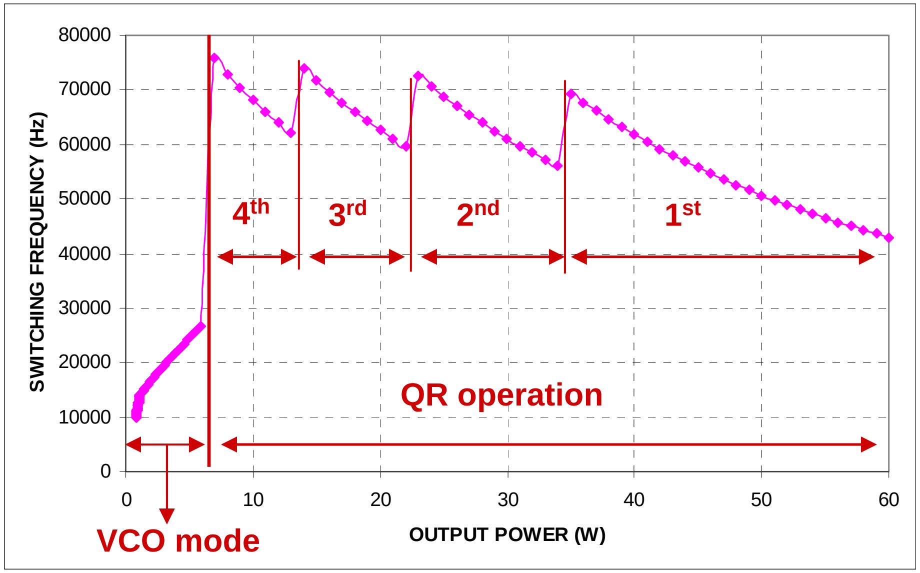
Control Topology Comparison

	Fixed F_{sw}	**Quasi Resonant**	**Fixed On Time (FOT)(NCP1351)**	**QR-FOT (NCP1380)**
Frequency	Fixed	Variable (max power at min F_{sw})	Variable (max power at max F_{sw})	Variable (min P_{out} at min F_{sw})
Light load efficiencies	Normal (with skip mode or freq foldback)	Valley jumping problem (noise) Max F_{sw} at min P_{out}	Best	Best
Full load efficiencies	Normal	Best	Normal	Best
Operating mode	CCM/DCM	BCM (Borderline)	CCM/DCM	BCM/DCM
Transformer size	Normal	Larger	Normal	Normal
EMI	Normal	Smaller	Normal	Smaller

QR-FOT: your key to improve standby (FOT) and optimize both efficiency and EMI (QR) for a wide output power range !!!

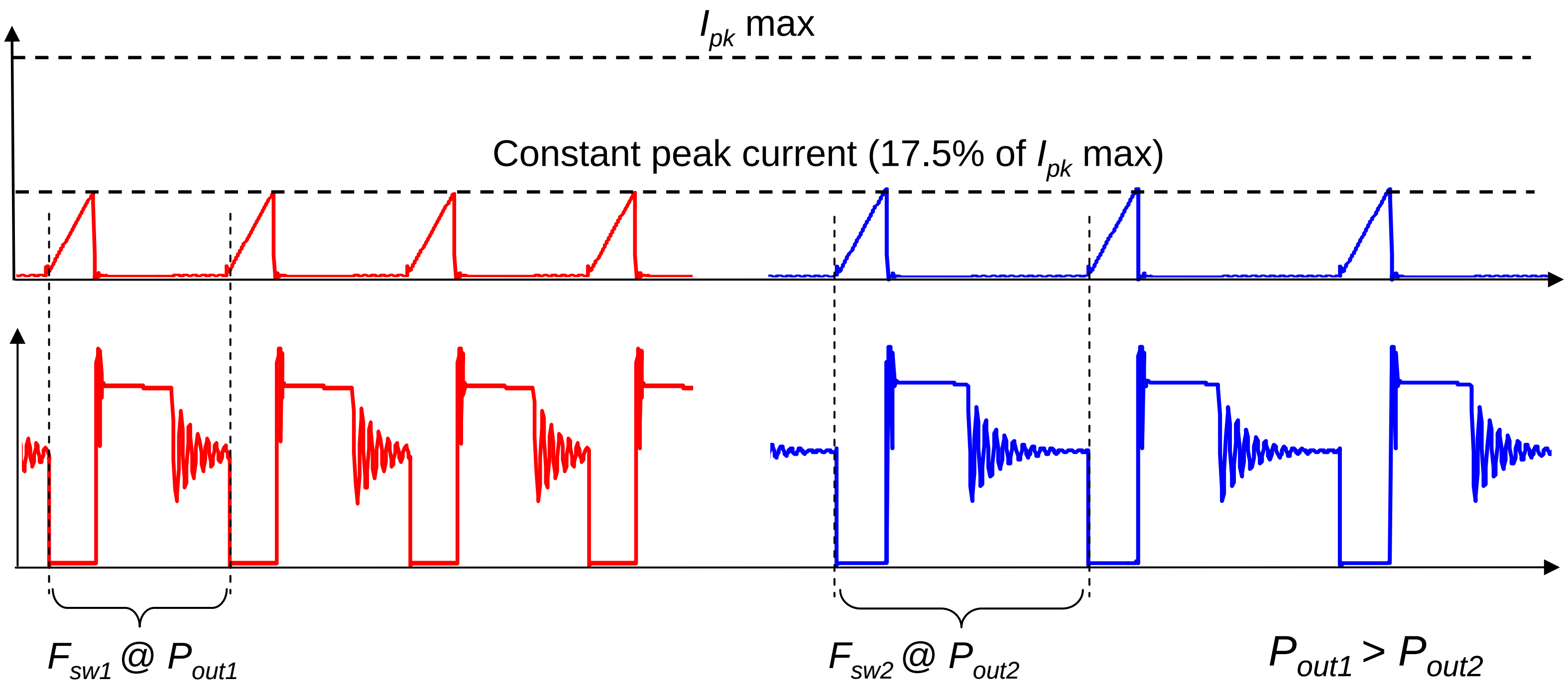
QR Mode with Valley Lockout

- As the load decreases, the controller changes valley (1st to 4th valley)
- The controller stays locked in a valley until the output power changes significantly.
    - No valley jumping noise
    - Natural switching frequency limitation



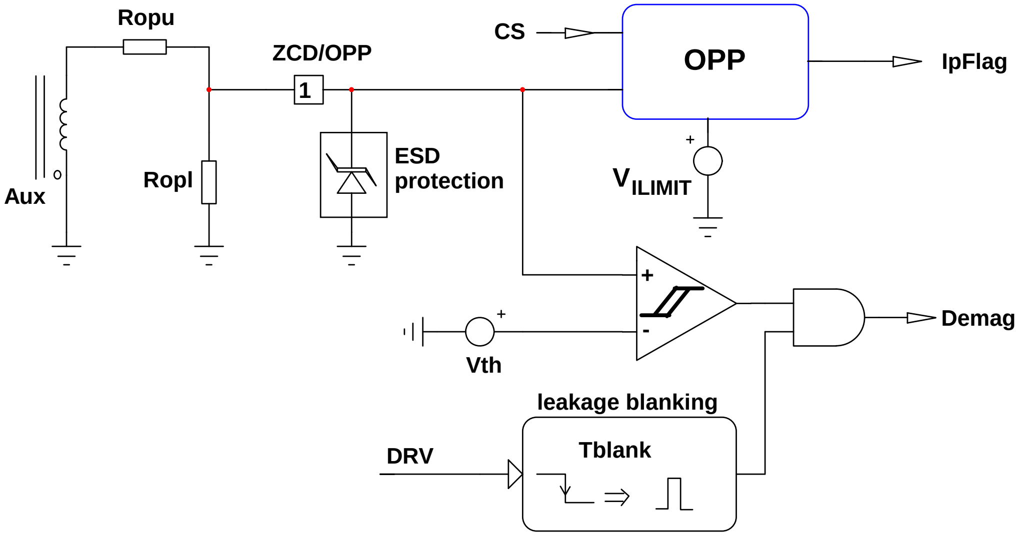
VCO Mode

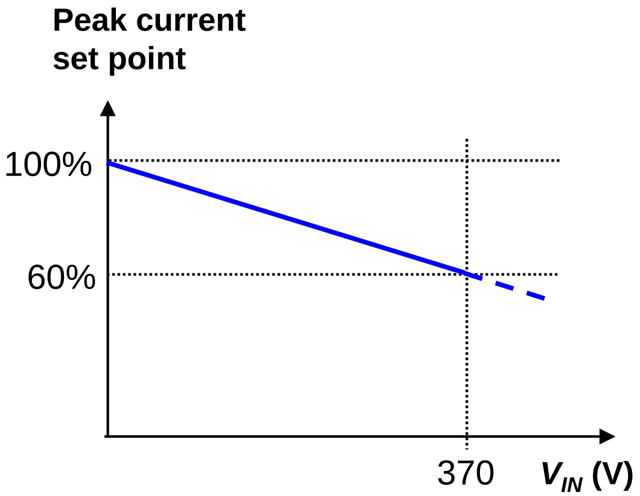
- ☐ Occurs when $V_{FB} < 0.8$ V (P_{out} decreasing) or $V_{FB} < 1.6$ V (P_{out} increasing)
- ☐ Fixed peak current (17.5% of $I_{pk,max}$), variable frequency set by the FB loop.



OPP: How does it Work?

- ☐ L_{aux} with flyback polarity swings to $-NV_{IN}$ during the on time.
- ☐ Adjust amount of OPP voltage with R_{opu} // R_{opl}.
- ☐ $V_{CS,max} = 0.8\text{ V} + V_{OPP}$





Non dissipative OPP !

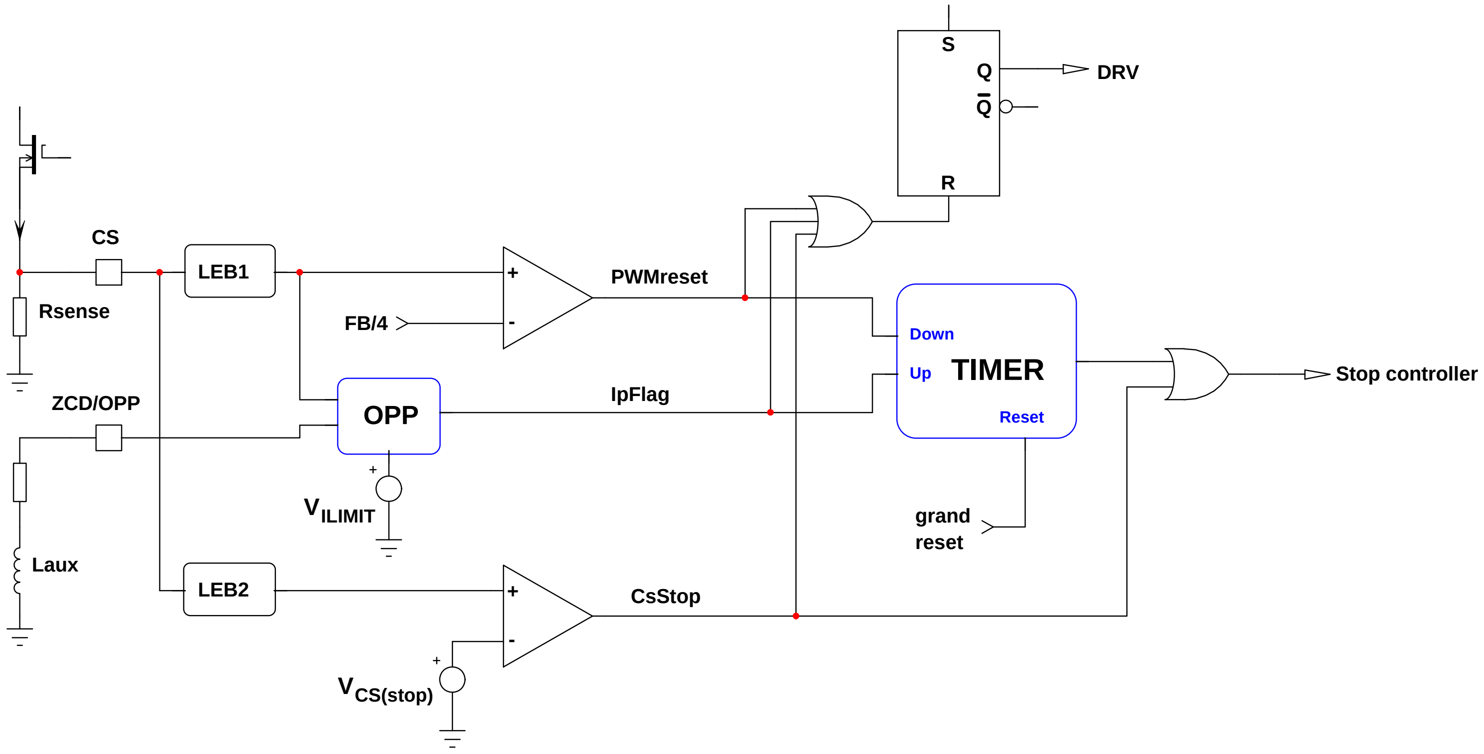
NCP1380 Versions

- ❑ 4 versions of NCP1380: A, B, C and D

	OTP	OVP	BO	**Auto-Recovery** Over current protection	**Latched** Over current protection
NCP1380 / A	X	X			X
NCP1380 / B	X	X		X	
NCP1380 / C		X	X		X
NCP1380 / D		X	X	X	

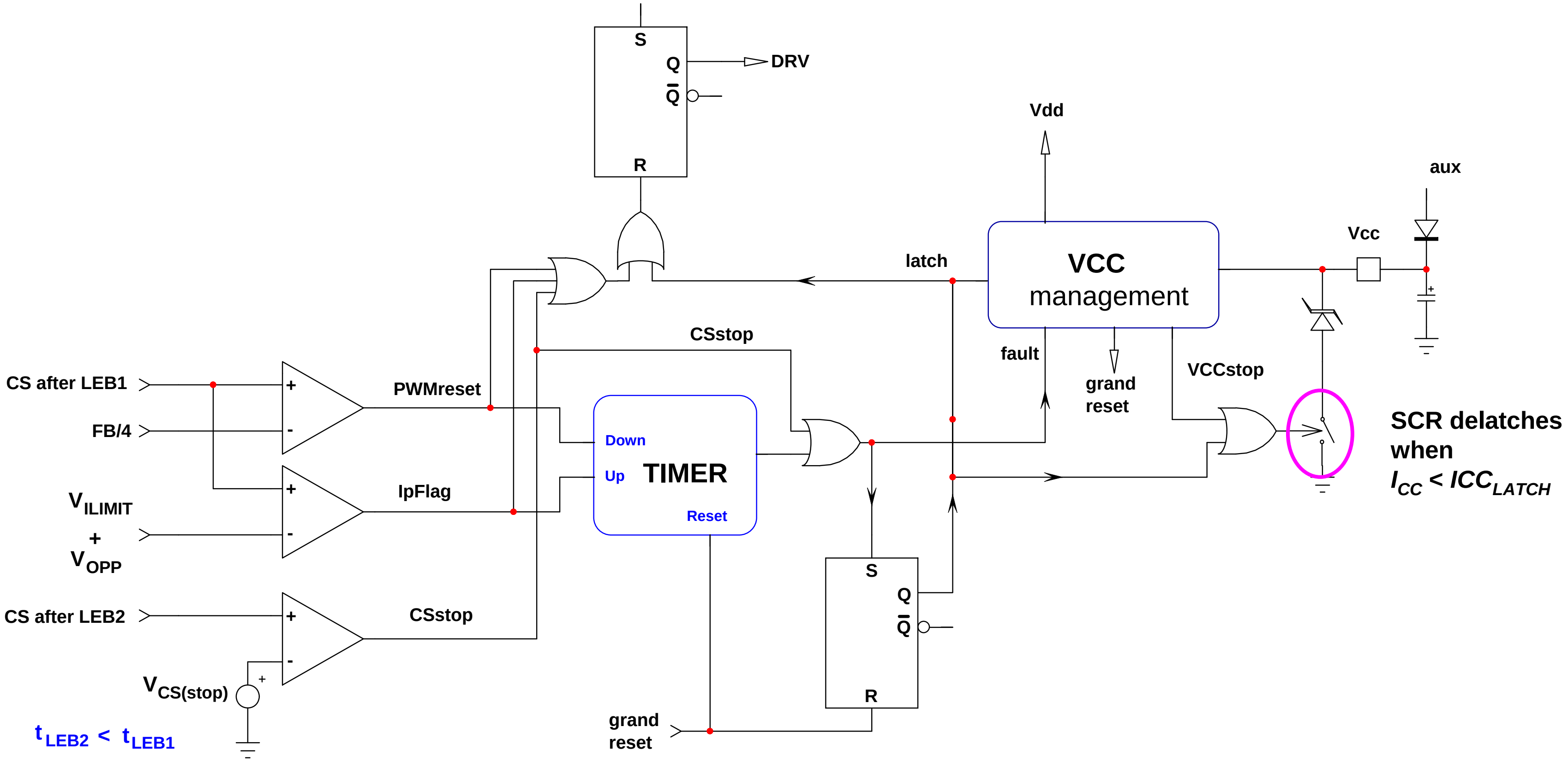
Short-Circuit Protection

- ❑ Internal 80-ms timer for short-circuit validation.
- ❑ Additional CS comparator with reduced LEB to detect winding short-circuit.
- ❑ $V_{CS(stop)} = 1.5 * V_{ILIMIT}$



Short-Circuit Protection (A and C Versions)

- A and C versions: the fault is latched.
  - V_{CC} is pulled down to 5 V and waits for ac removal.



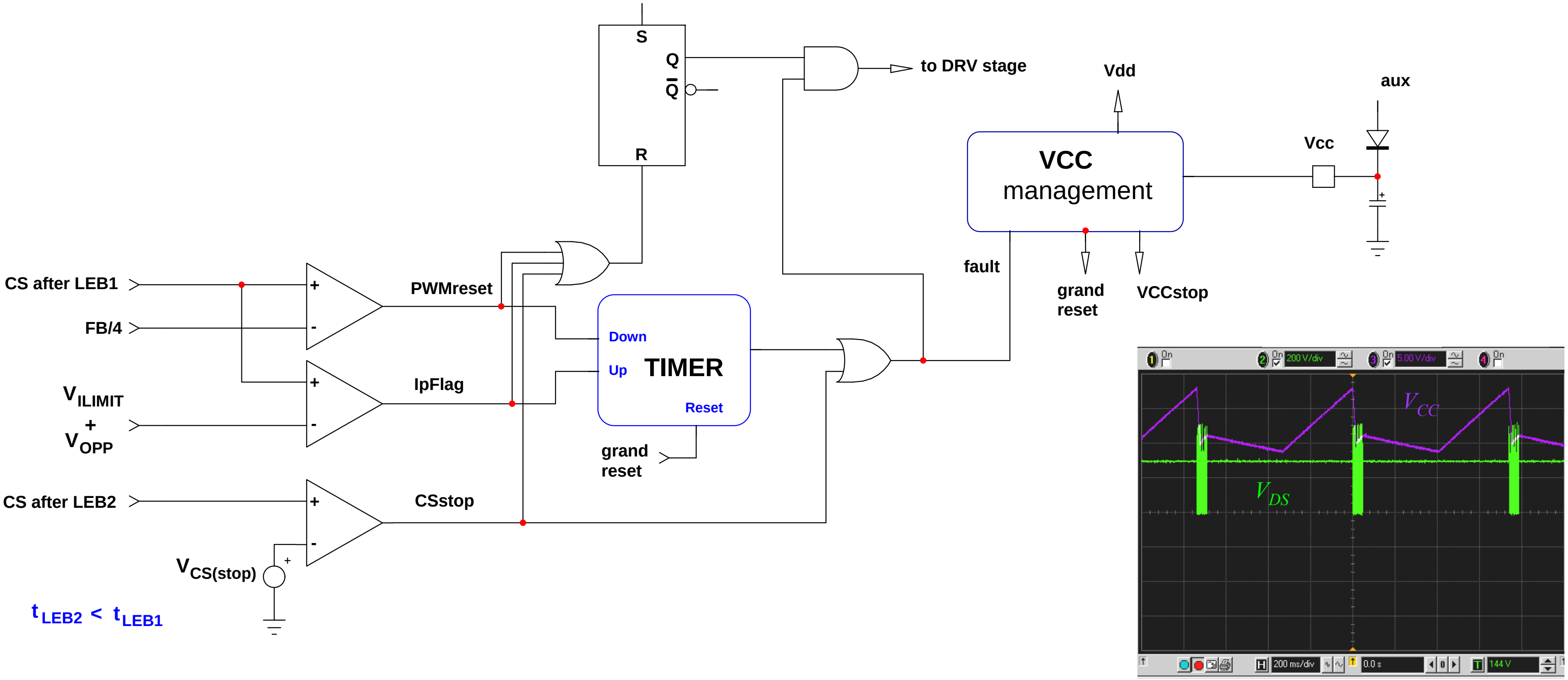
SCR delatches when $I_{CC} < ICC_{LATCH}$

$t_{LEB2} < t_{LEB1}$

Short Circuit Protection (B and D)

- ☐ Auto-recovery short circuit protection: the controller tries to restart
- ☐ Auto-recovery imposes a low burst in fault mode.

➡ Low average input power in fault condition

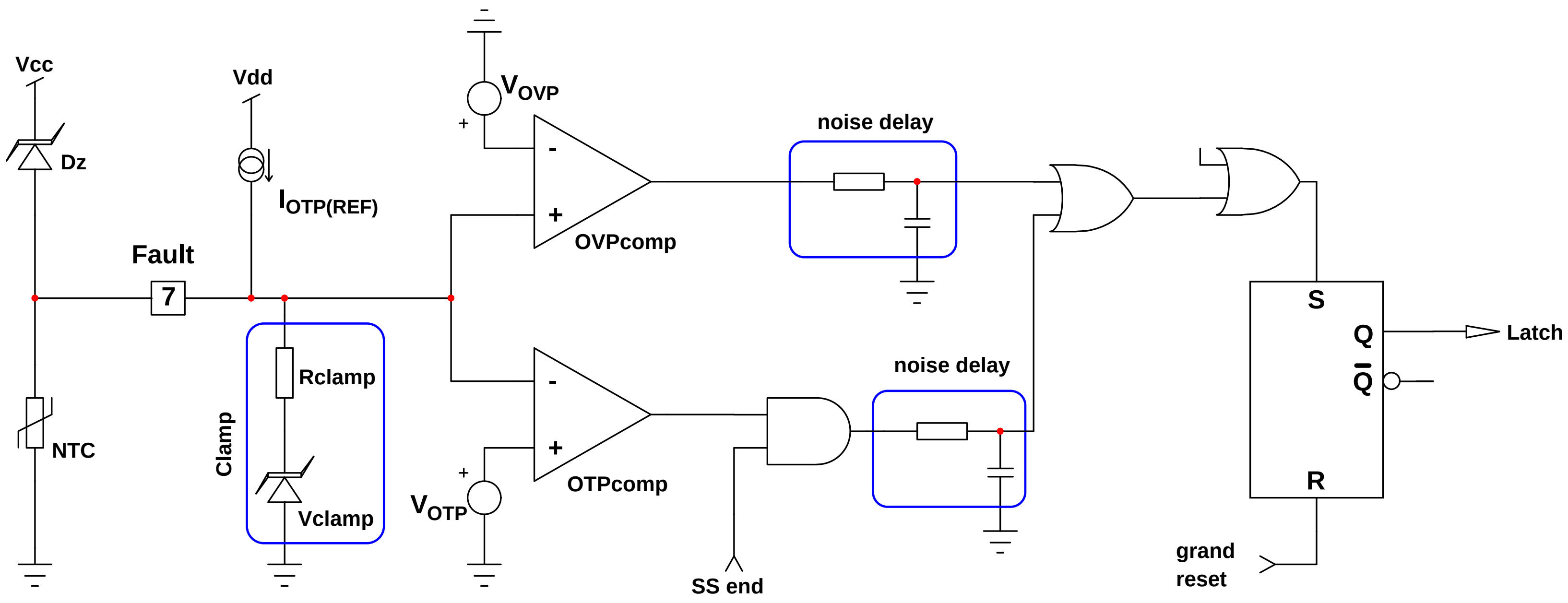


OVP / OTP (A & B Versions)

- OVP and OTP detection are achieved by reading the voltage on the pin 7.
- If the temperature increases, the NTC resistor reduces and V_{Fault} decreases.

  When $V_{Fault} < V_{OTP}$ ➔ the controller is latched.
- If V_{CC} increases, the zener diode injects current in the clamp circuit.

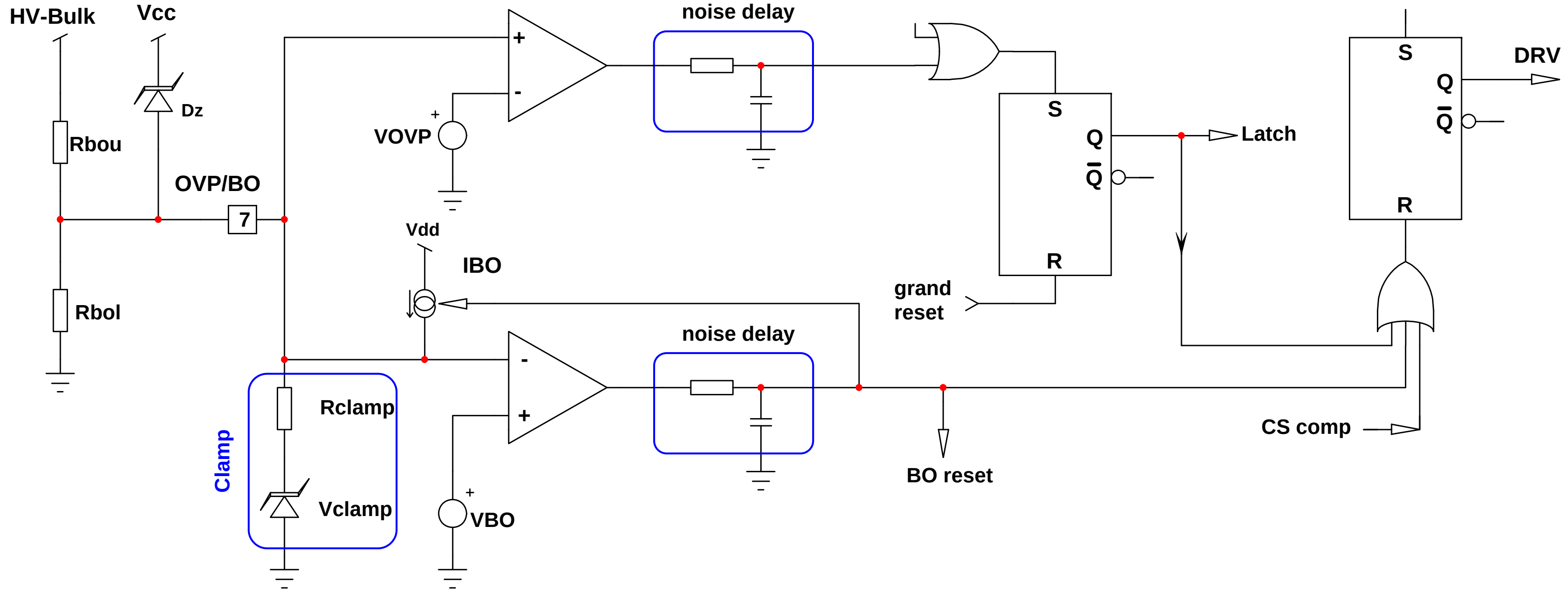
  When $V_{Fault} > V_{OVP}$ ➔ the controller is latched.



BO / OVP (C & D Versions)

BO

- If V_{pin7} > BO threshold & V_{CC} > VCC_{on}, the controller starts pulsing.
- The hysteresis current source is ON when V_{pin7} > BO threshold.



OVP

- If V_{CC} > BV_{Dz}, the zener diode injects current inside the clamp resistor.
- When V_{pin7} reaches the OVP threshold, the controller is latched.

Conclusion

- ☐ Changing valley as the load decreases is a way to limit the maximum switching frequency in QR power supplies.

- ☐ Lots of equations to predict the efficiency of the power supply, but good matching between calculations and the measurement.

- ☐ Synchronous rectification increases the efficiency of the QR power supply but increases also the power consumption in standby.

- ☐ Friendly compensation for QR power supply (DCM: 1st order system)

- ☐ NCP1380 features:
  - QR current-mode with valley lockout for noise immunity for high load.
  - VCO mode in light load for improved efficiency.

For More Information

- View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com

- View reference designs, design notes, and other material supporting the design of highly efficient power supplies at www.onsemi.com/powersupplies