ON Semiconductor®

Design of a QR Adapter with Improved Efficiency and Low Standby Power

Agenda

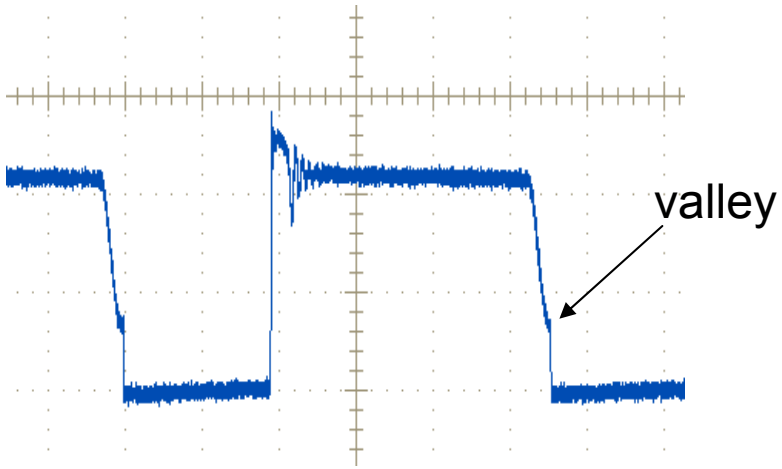
1. Quasi-Resonance (QR) Generalities
2. The Valley Lockout Technique
3. The NCP1379/1380
4. Step by Step Design Procedure
5. Performances of a 60 W Adapter Featuring Valley Lockout

Agenda

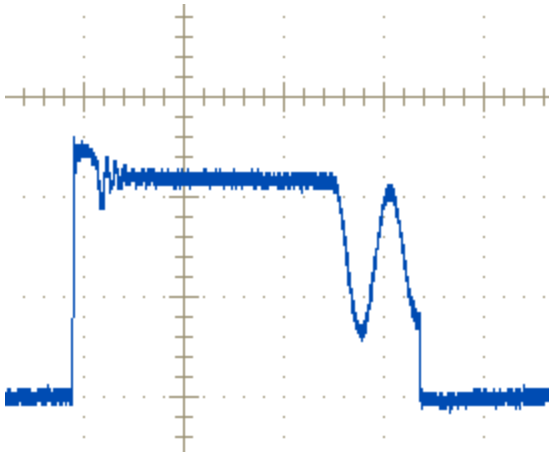
1. Quasi-Resonance (QR) Generalities
2. The Valley Lockout Technique
3. The NCP1379/1380
4. Step by Step Design Procedure
5. Performances of a 60 W Adapter Featuring Valley Lockout

What is Quasi-Square Wave Resonance ?

- MOSFET turns on when $V_{DS}(t)$ reaches its minimum value.
  - ➢ Minimizes switching losses
  - ➢ Improves the EMI signature



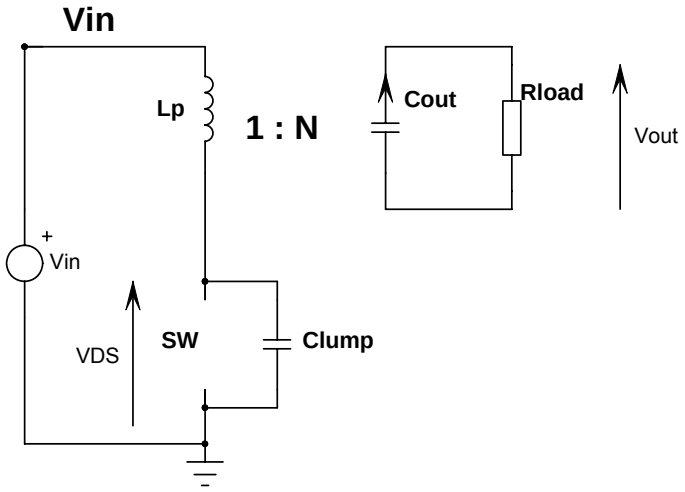
MOSFET turns on in first valley

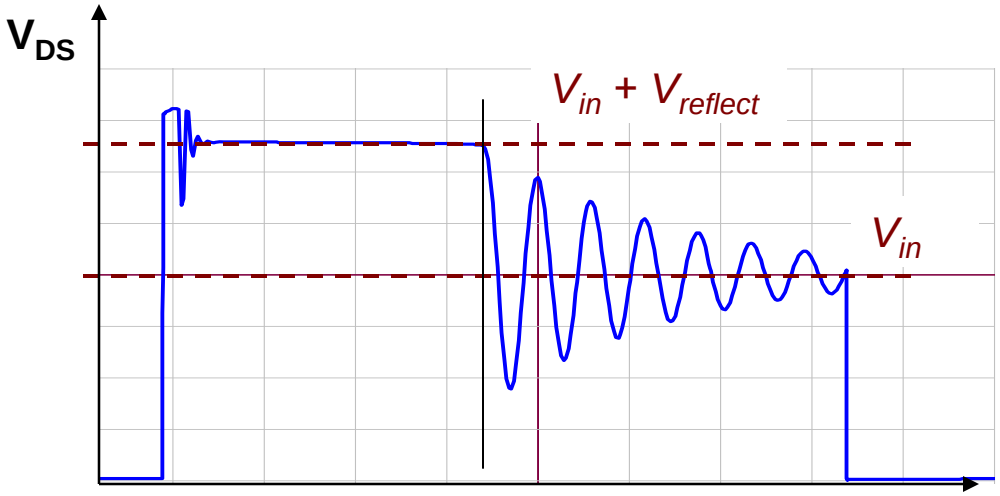


MOSFET turns on in second valley

Quasi-Resonance Operation

- In DCM, V_{DS} must drop from (V_{in} + $V_{reflect}$) to V_{in}
- Because of L_p-C_{lump} network → oscillations appear
- Oscillation half period: $t_x = \pi\sqrt{L_p C_{lump}}$





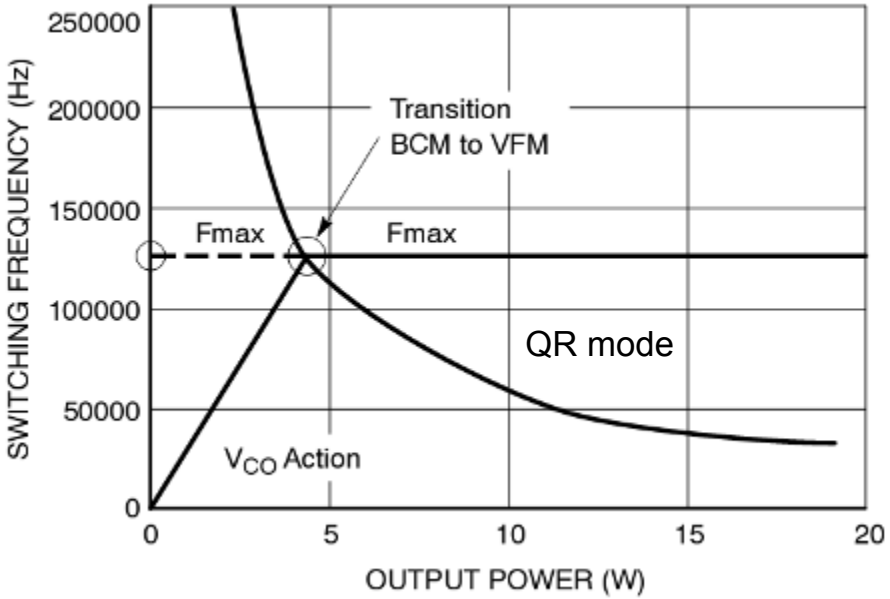
A Need to Limit the Switching Frequency

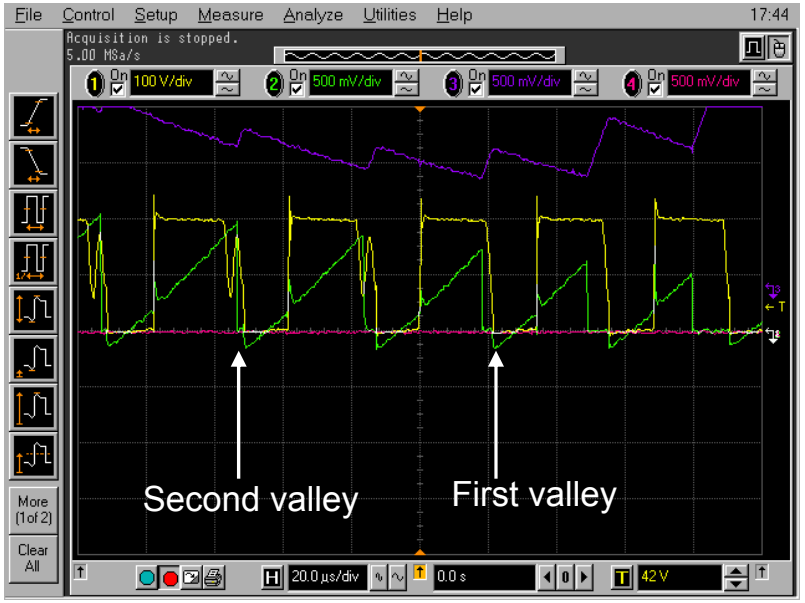
- In a self-oscillating QR, F_{sw} increases as the load decreases

  ⇒ Higher losses at light load if F_{sw} is not limited

- 2 methods to limit F_{sw}:
  - Frequency clamp with frequency foldback
  - Changing valley with valley lockout

Frequency Clamp in QR Converters





- In light load, frequency increases and hits clamp
  - Multiple valley jumps
  - Jumps occur at audible range
  - Creates signal instability

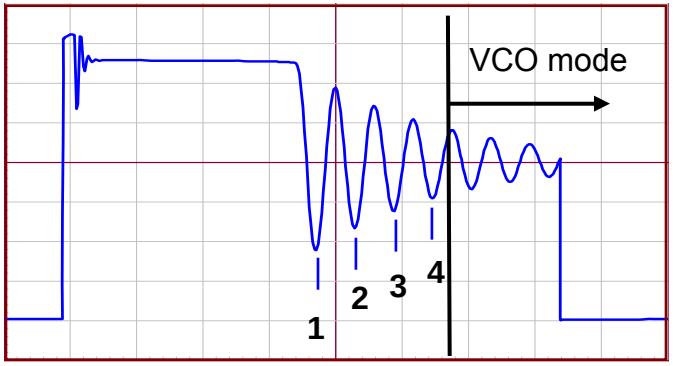
Agenda

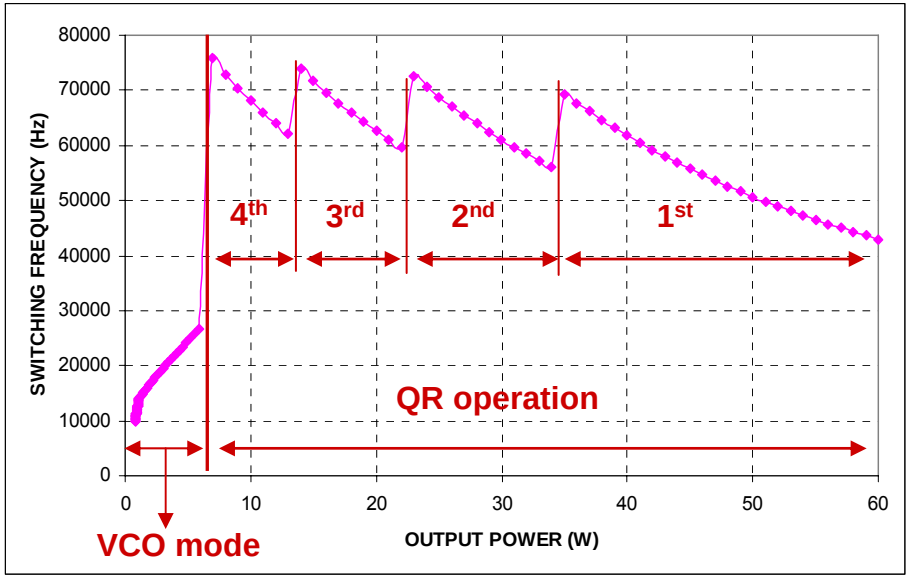
1. Quasi-Resonance (QR) Generalities
2. The Valley Lockout Technique
3. The NCP1379/1380
4. Step by Step Design Procedure
5. Performances of a 60 W Adapter Featuring Valley Lockout

The Valley Lockout

- As the load decreases, the controller changes valley (1st to 4th valley in NCP1380)
- The controller stays locked in a valley until the output power changes significantly.

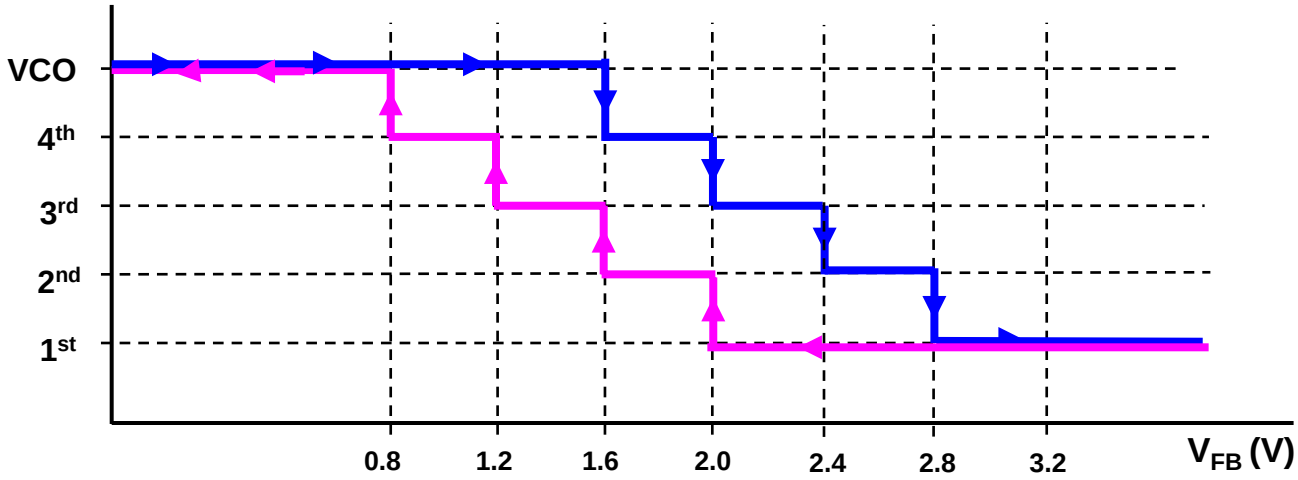
  – No valley jumping noise
  – Natural switching frequency limitation





The Valley Lockout

- FB comparators select the valley and pass the information to a counter.
- The hysteresis of FB comparators locks the valley.
- 2 possible operating set points for a given FB voltage.



V_{FB} increases (P_{OUT} increases)

V_{FB} decreases (P_{OUT} decreases)

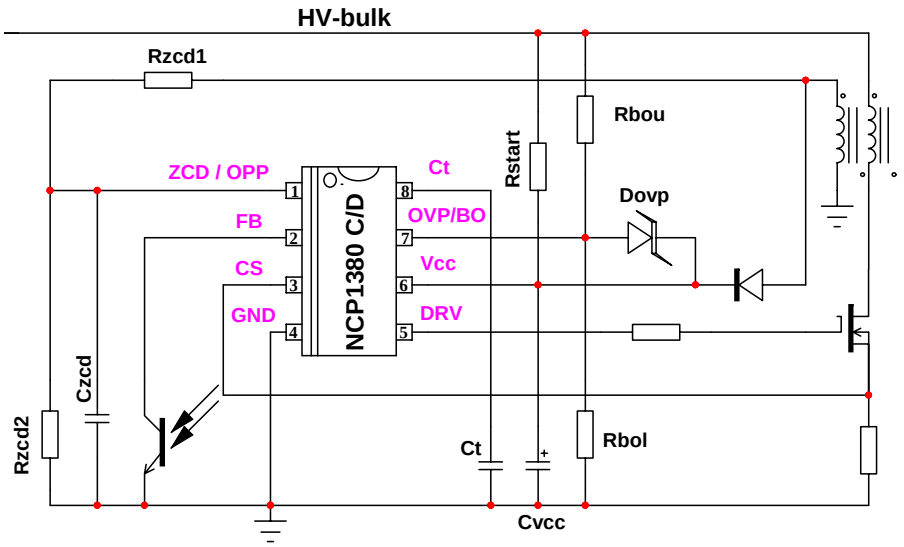
Agenda

1. Quasi-Resonance (QR) Generalities
2. The Valley Lockout Technique
3. The NCP1379/1380
4. Step by Step Design Procedure
5. Performances of a 60 W Adapter Featuring Valley Lockout

NCP1379/1380 Features

- Operating modes:
  - QR current-mode with valley lockout for noise immunity
  - VCO mode in light load for improved efficiency

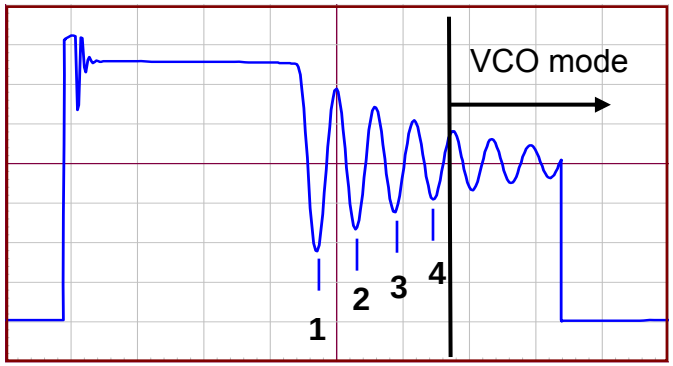
- Protections
  - Over power protection
  - Soft-start
  - Short circuit protection
  - Over voltage protection
  - Over temperature protection
  - Brown-Out

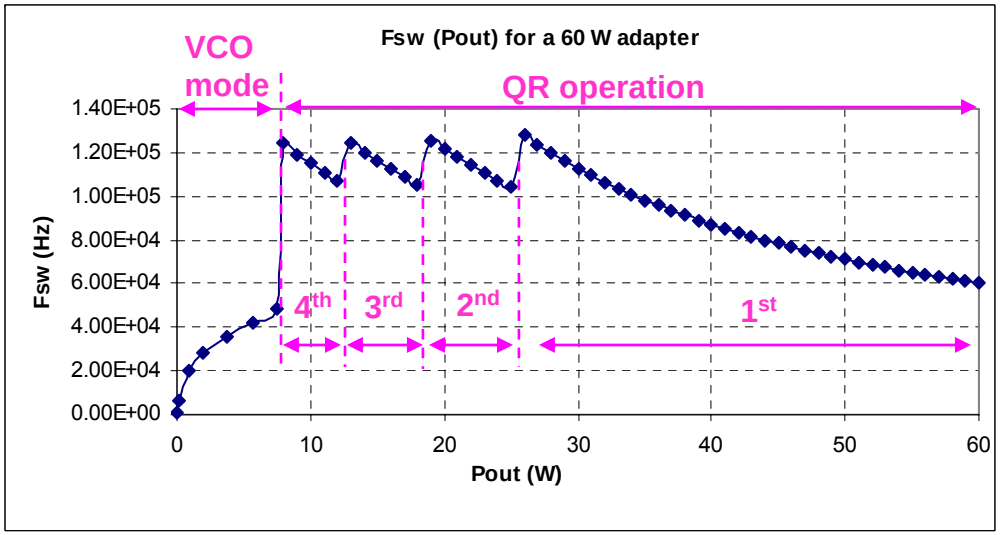


❑ Mass production: Q4 2009

QR Mode with Valley Lockout

- **Operating principle:**
  - Locks the controller into a valley (up to the 4th) according to FB voltage.
  - Peak current adjusts according to FB voltage to deliver the necessary output power.

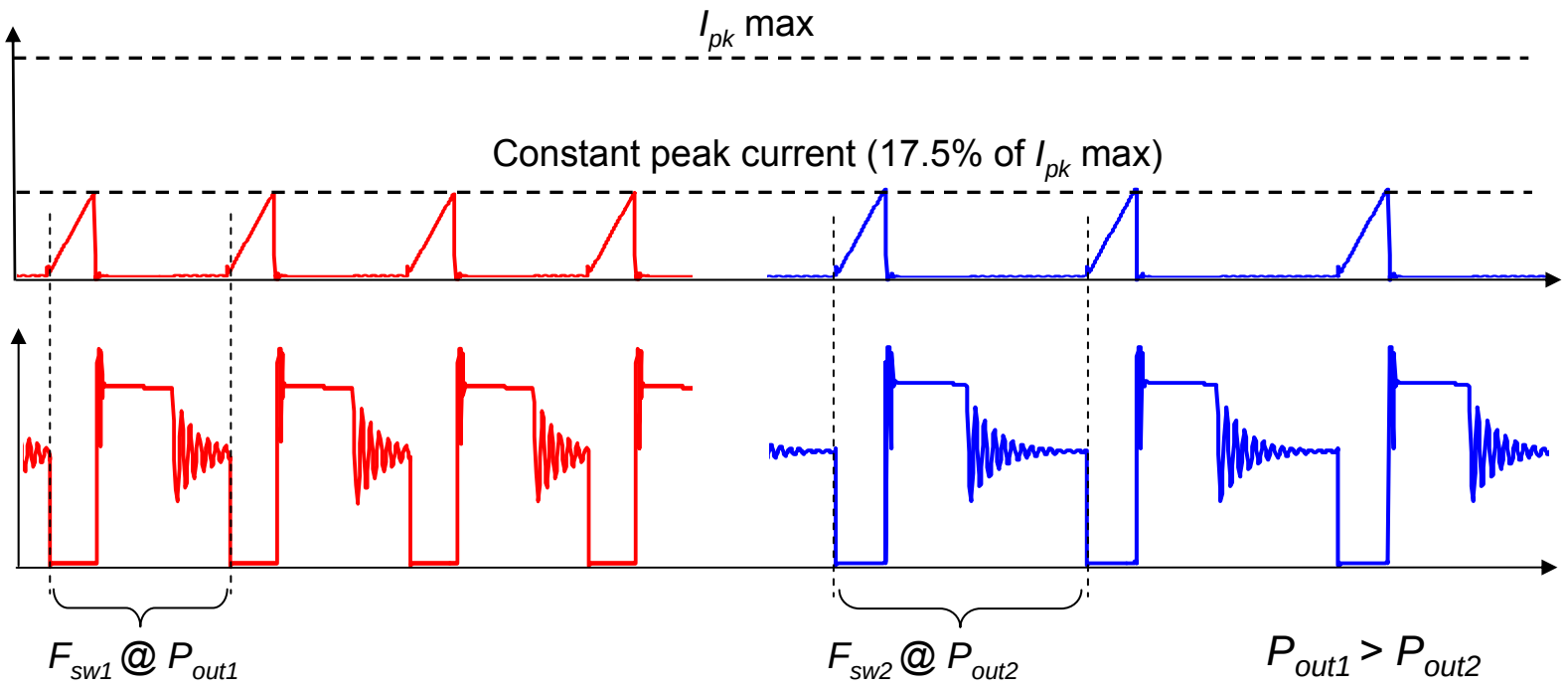




- **Advantages**
  - Solves the valley jumping instability in QR converters
  - Achieves higher min F_{sw} and lower max F_{sw} than in traditional QR converters
  - Reduce the transformer size

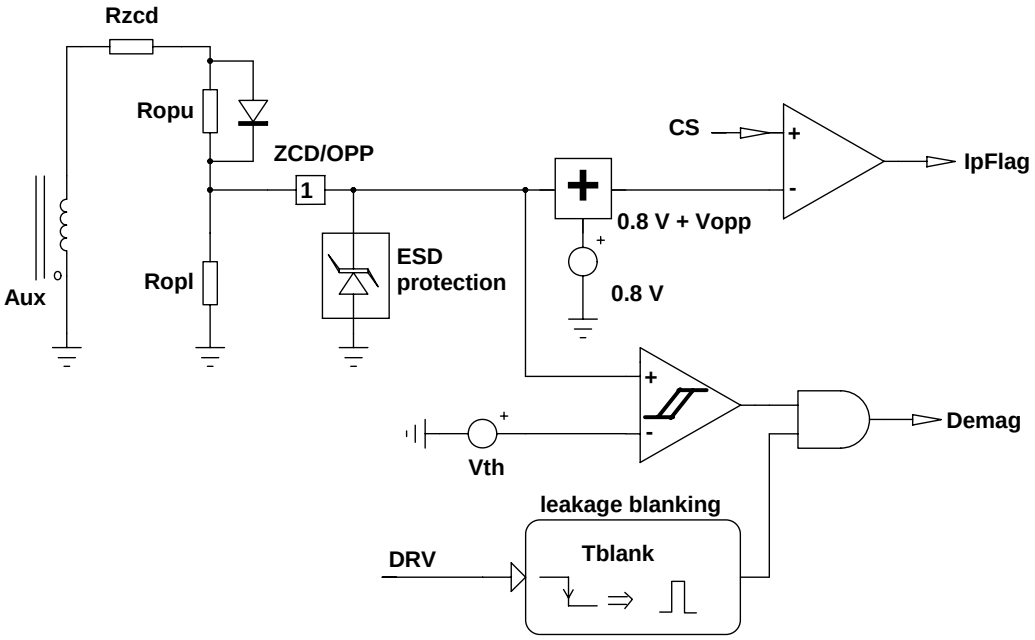
VCO Mode

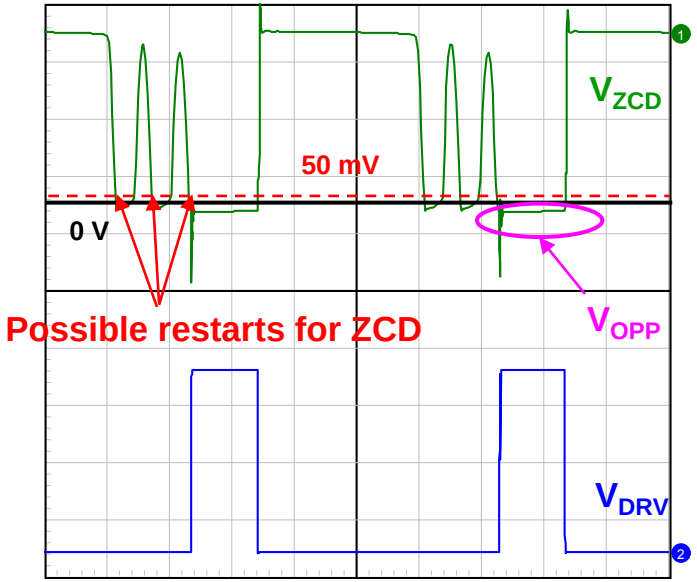
- Occurs when V_{FB} < 0.8 V (P_{out} decreasing) or V_{FB} < 1.4 V (P_{out} increasing)
- Fixed peak current (17.5% of $I_{pk,max}$), variable frequency set by the FB loop.



Combined ZCD and OPP

- Zero-Crossing Detection (ZCD) and Over Power Protection (OPP) are achieved by reading the Aux. winding voltage
  - ZCD function used during the off-time of MOSFET (positive voltage).
  - OPP function used during the on-time of MOSFET (negative voltage)





NCP1380 Versions

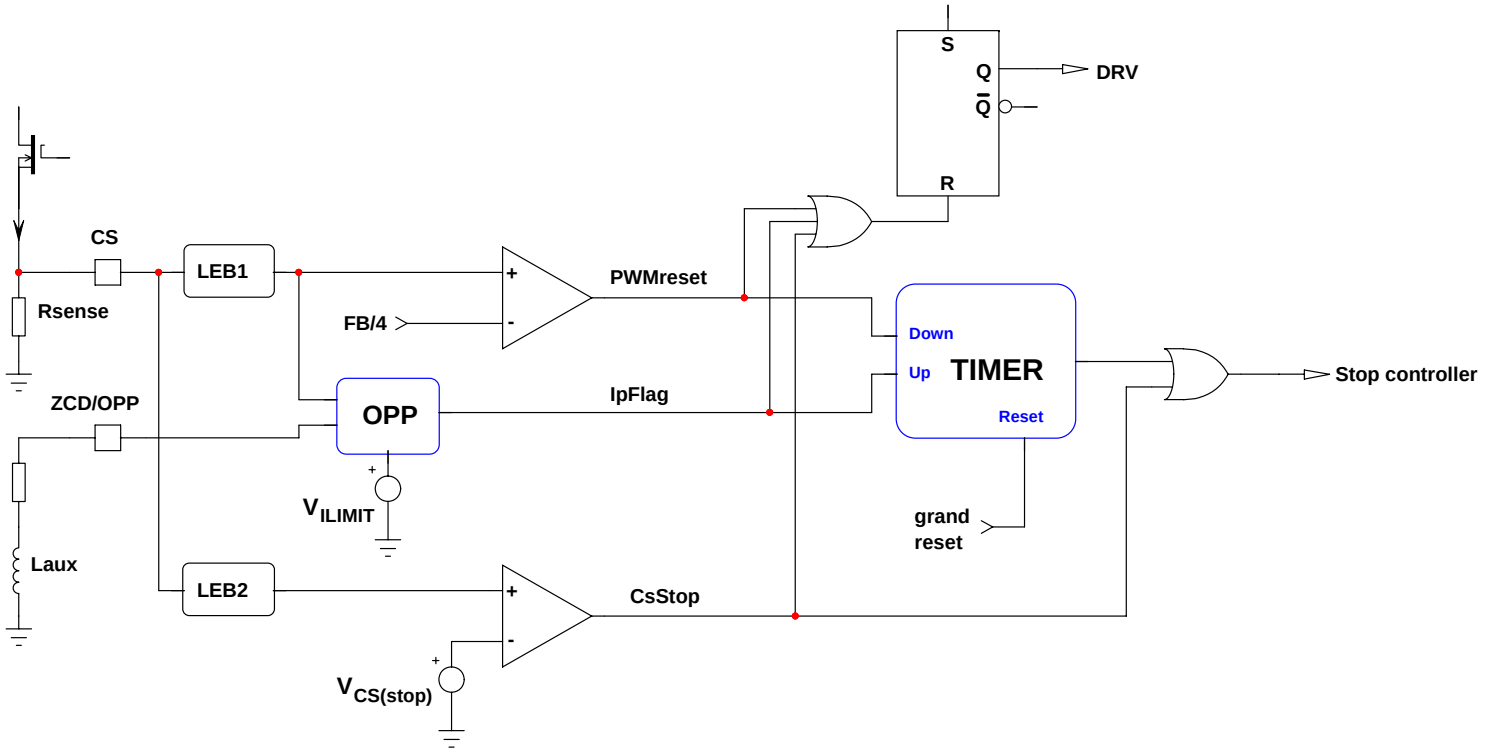
- 4 versions of NCP1380: A, B, C and D

	OTP	OVP	BO	Auto-Recovery Over current protection	Latched Over current protection
NCP1380 / A	X	X			X
NCP1380 / B	X	X		X	
NCP1380 / C		X	X		X
NCP1380 / D		X	X	X	

OTP: Over Temperature Protection
OVP: Over Voltage Protection
BO: Bown-Out

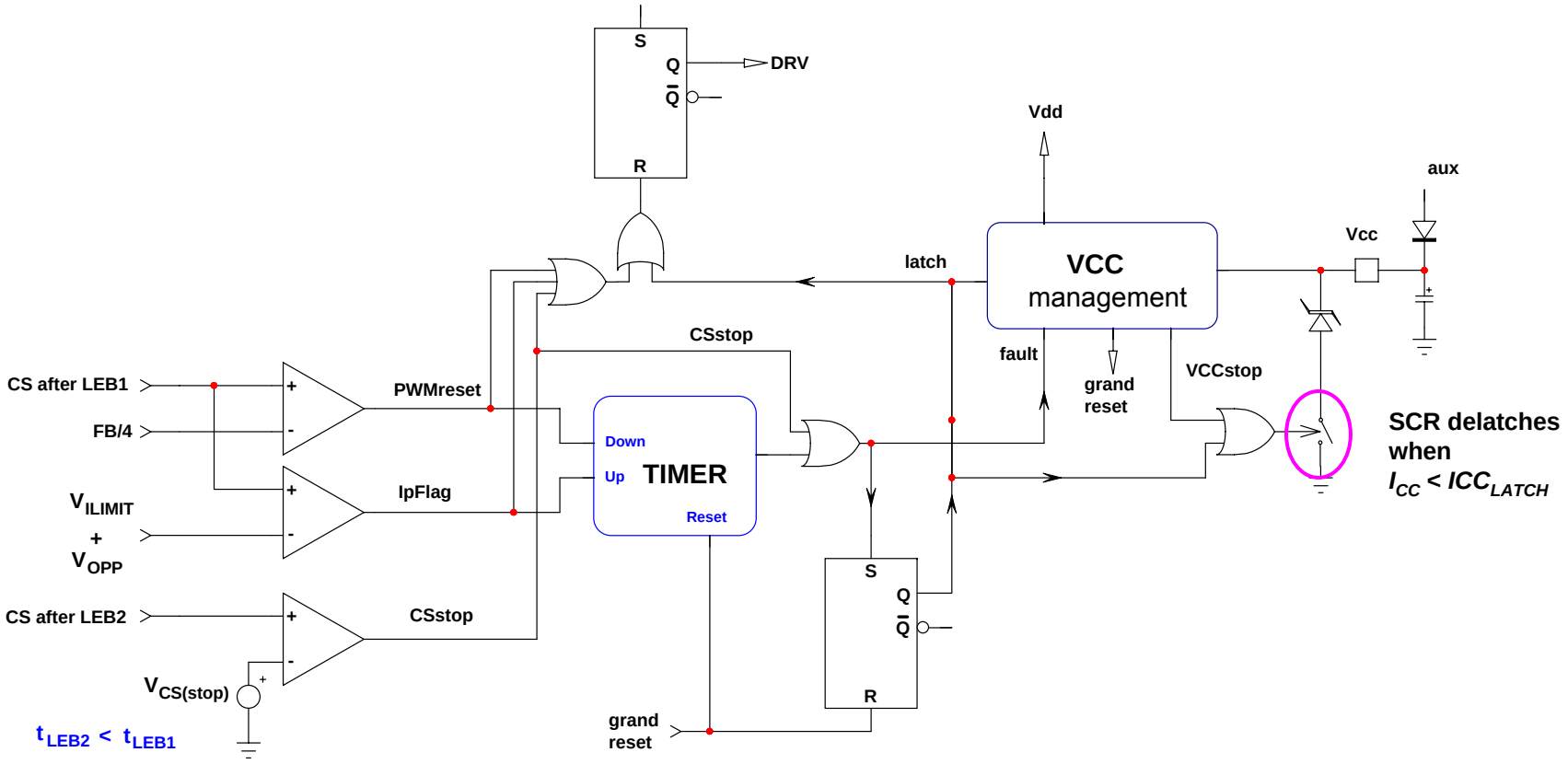
Short-Circuit Protection

- Internal 80 ms timer for short-circuit validation.
- Additional CS comparator with reduced LEB to detect winding short-circuit.
- $V_{CS(stop)} = 1.5 * V_{ILIMIT}$



Short-Circuit Protection (A and C versions)

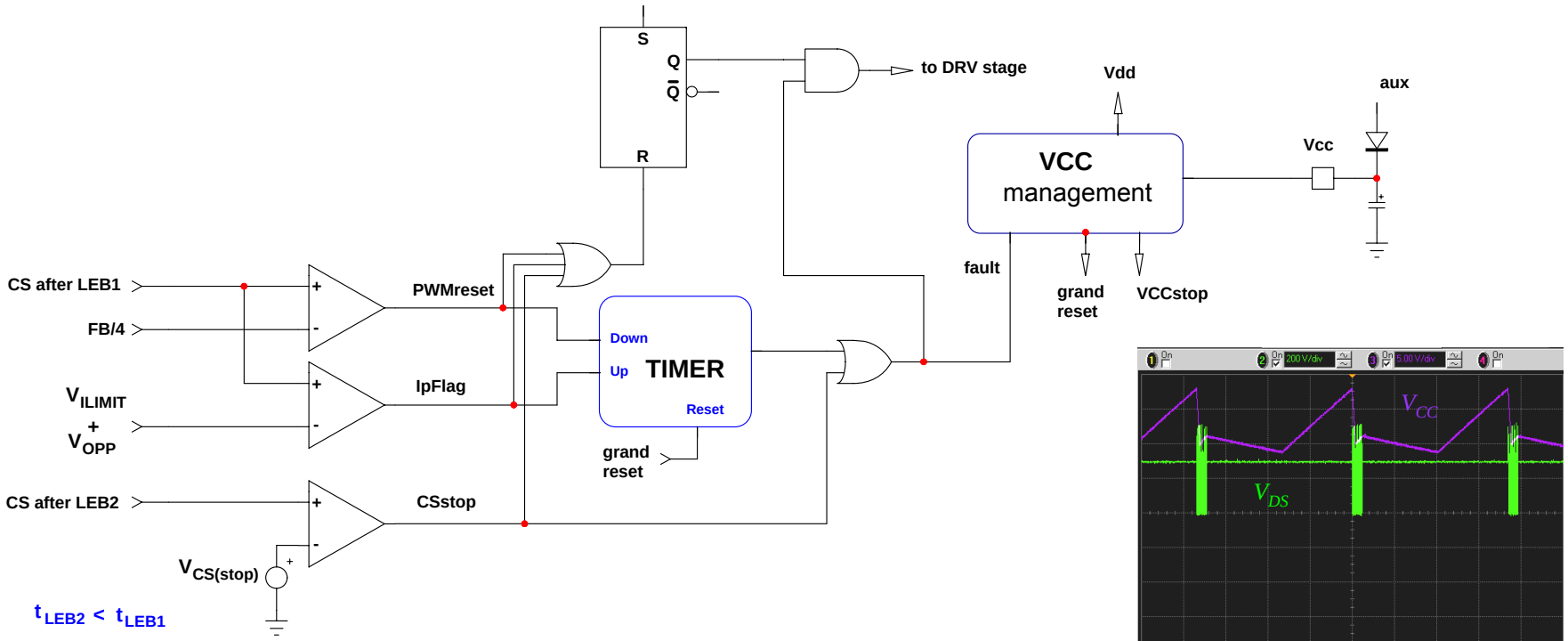
- A and C versions: the fault is latched.
  - V_{CC} is pulled down to 5 V and waits for ac removal.



Short Circuit Protection (B and D)

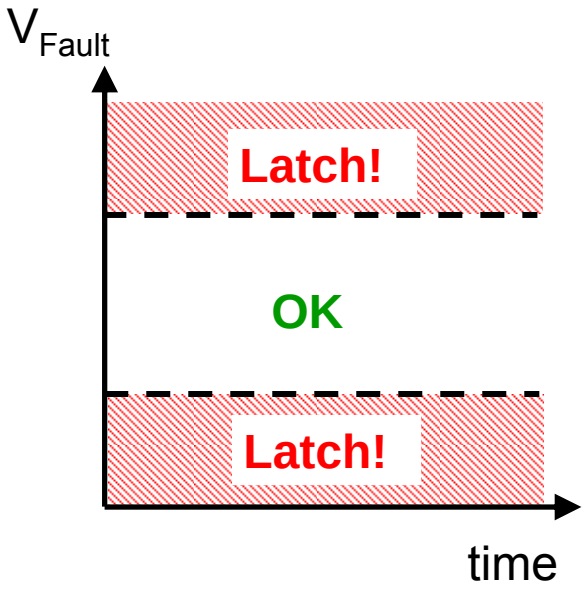
- Auto-recovery short circuit protection: the controller tries to restart
- Auto-recovery imposes a low burst in fault mode.

➡ Low average input power in fault condition

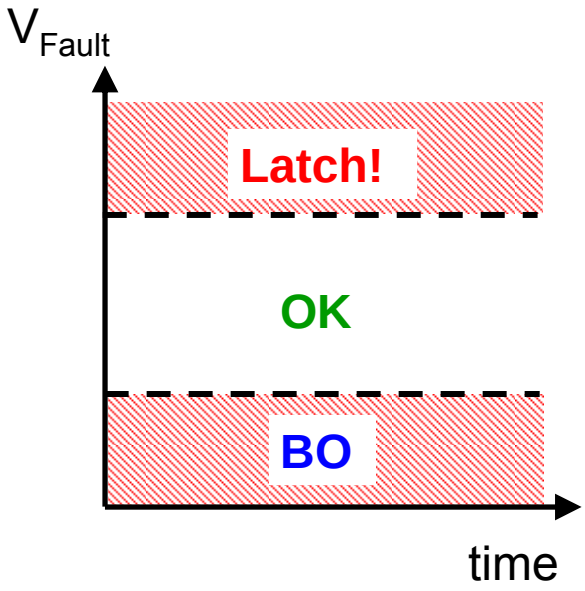


Fault Pin Combinations

- OVP / OTP
  - NCP1380 A & B versions



- OVP / BO
  - NCP1380 C & D versions, NCP1379



- OVP and OTP or OVP and BO combined on one pin.
- Less external components needed.

Agenda

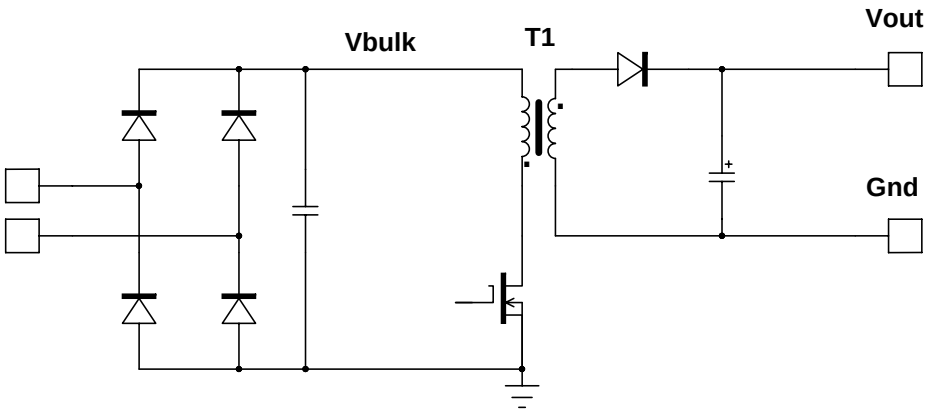
1. Quasi-Resonance (QR) Generalities
2. The Valley Lockout Technique
3. The NCP1379/1380
4. Step by Step Design Procedure
5. Performances of a 60 W Adapter Featuring Valley Lockout

Step by Step Design Procedure

- Calculating the QR transformer
- Predicting the switching frequency
- Implementing Over Power Compensation
- Improving the efficiency at light load with the VCO mode
- Choosing the startup resistors
- Implementing synchronous rectification

Design Example

- Power supply specification:
  - V_{out} = 19 V
  - P_{out} = 60 W
  - $F_{sw,min}$ = 45 kHz (at V_{in} = 100 Vdc)
  - 600 V MOSFET
  - V_{in} = 85 ~ 265 Vrms
  - Standby power consumption < 100 mW @ 230 Vrms



Turns Ratio Calculation

- Derate maximum MOSFET BV_{dss}:

$$V_{ds,max} = BV_{dss} k_D$$

k_D: derating factor

- For a maximum bulk voltage, select the clamping voltage:

$$V_{clamp} = V_{ds,max} - V_{in,max} - V_{os}$$

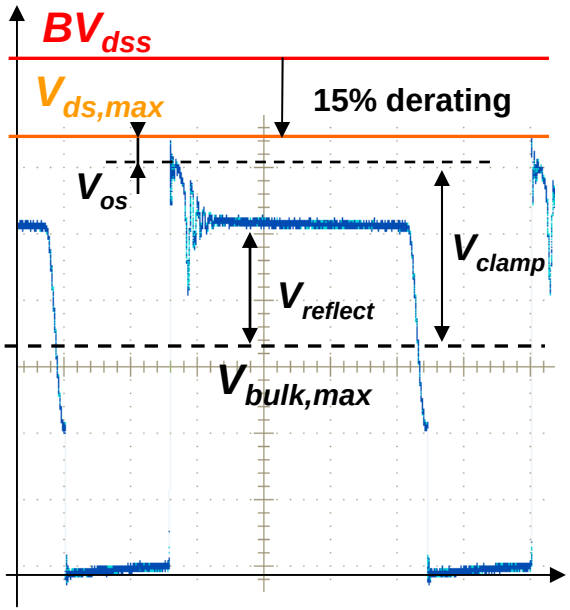
V_{os}: diode overshoot

- Deduce turns ratio:

$$N_{ps} = \frac{N_s}{N_p} = \frac{k_c (V_{out} + V_f)}{V_{clamp}}$$

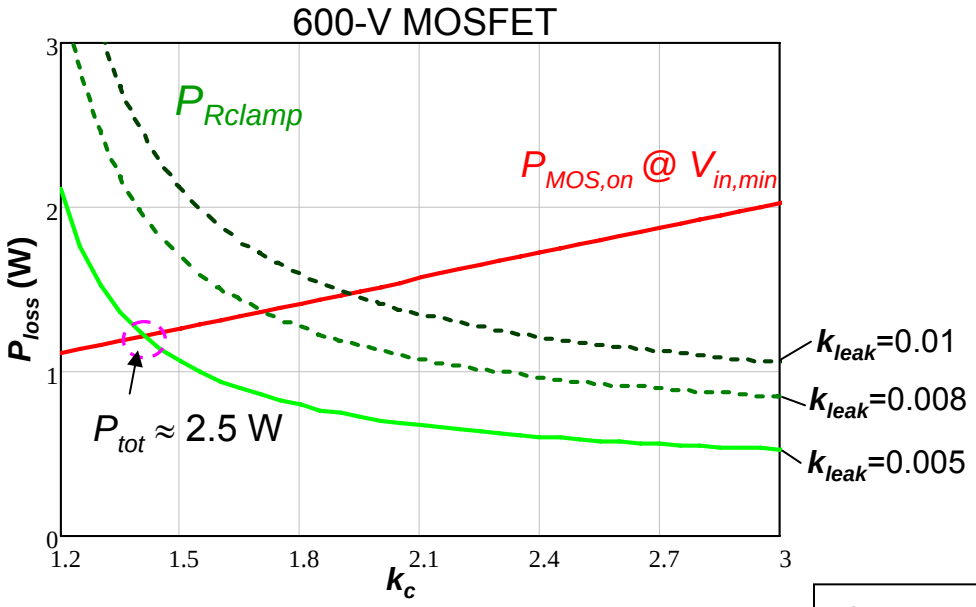
k_c: clamping coef.

$k_c = V_{clamp} / V_{reflect}$)



How to Choose k_c

- k_c choice dependant of L_{leak} (leakage inductance of the transformer)
- k_c value can be chosen to equilibrate MOS conduction losses and clamping resistor losses.



$$\begin{cases} P_{Rclamp} = k_{leak} \dfrac{P_{out}}{\eta} \dfrac{k_c}{k_c - 1} \\ P_{MOS,on} = R_{dson} \dfrac{4P_{out}^{\,2}}{3\eta^2 V_{in,min}} \left(\dfrac{1}{V_{in,min}} + \dfrac{k_c}{BV_{dss}k_D - V_{in,max} - V_{os}} \right) \end{cases}$$

Curves plotted for:

R_{dson} = 0.77 Ω at T_j = 110 °C

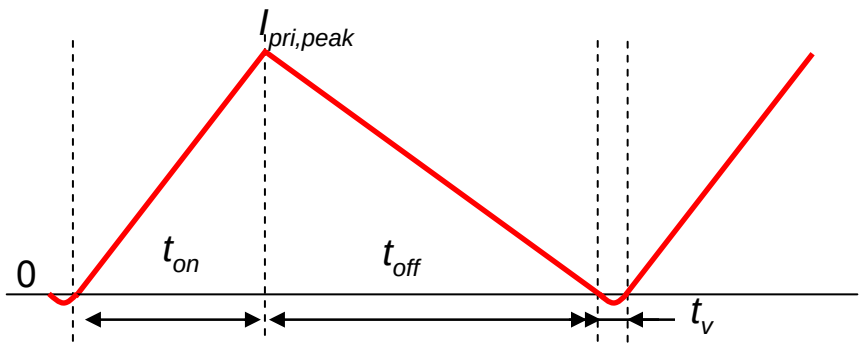
P_{out} = 60 W

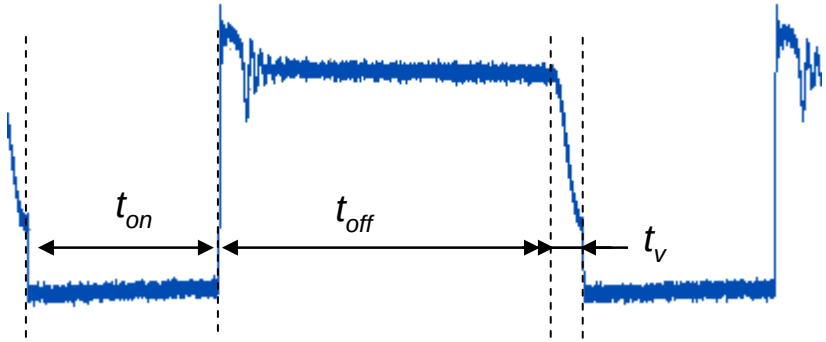
$V_{in,min}$ = 100 Vdc

Primary Peak Current and Inductance

- $P_{out} = \frac{1}{2} L_{pri} I_{pri,peak}{}^2 F_{sw} \eta$

DCM





- $T_{sw} = \frac{I_{pri,peak} L_{pri}}{V_{in,min}} + \frac{I_{pri,peak} L_{pri} N_{ps}}{V_{out} + V_f} + \pi \sqrt{L_{pri} C_{lump}}$ ← C_{oss} contribution alone.

$$I_{pri,peak} = 2 \frac{P_{out}}{\eta} \left(\frac{1}{V_{in,min}} + \frac{N_{ps}}{V_{out} + V_f} \right) + \pi \sqrt{\frac{2 P_{out} C_{lump} F_{sw}}{\eta}}$$

$$L_{pri} = \frac{2 P_{out}}{I_{pri,peak}{}^2 F_{sw} \eta}$$

RMS Current

- Calculate maximum duty-cycle at maximum P_{out} and minimum V_{in}:

$$d_{max} = \frac{I_{pri,peak} L_{pri}}{V_{in,min}} F_{sw,min}$$

- Deduce primary and secondary RMS current value:

$$I_{pri,rms} = I_{pri,peak} \sqrt{\frac{d_{max}}{3}}$$

$$I_{sec,rms} = \frac{I_{pri,peak}}{N_{ps}} \sqrt{\frac{1-d_{max}}{3}}$$

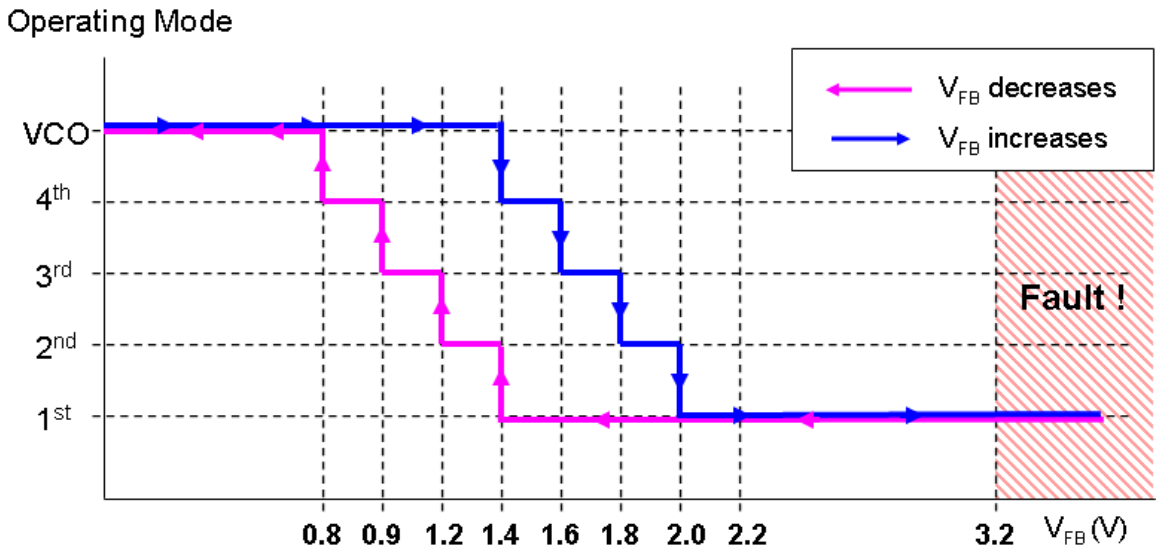
$I_{pri,rms}$ and $I_{sec,rms}$ ⇒ Losses calculation

Design Example

- Based on equations from slides 11 to 14:
  - Turns ratio: $$N_{ps} = \frac{k_c(V_{out}+V_f)}{B_{Vdss}k_D - V_{in,max} - V_{os}} = \frac{1.3\times(19+0.8)}{600\times0.85-375-10} \Rightarrow \boxed{N_{ps} \approx 0.25}$$
  - Peak current: $$I_{pri,peak} = \frac{2P_{out}}{\eta}\left(\frac{1}{V_{in,min}} + \frac{N_{ps}}{V_{out}+V_f}\right) + \pi\sqrt{\frac{2P_{out}C_{lump}F_{sw}}{\eta}}$$
    $$= \frac{2\times60}{0.85}\left(\frac{1}{100} + \frac{0.25}{19.8}\right) + \pi\sqrt{\frac{2\times60\times250p\times45k}{0.85}} \Rightarrow \boxed{I_{pri,peak} = 3.32\,A}$$
  - Inductance: $$L_{pri} = \frac{2P_{out}}{I_{pri,peak}{}^2 F_{sw}\eta} = \frac{2\times60}{3.32^2\times45k\times0.85} \Rightarrow \boxed{L_{pri} = 285\,\mu H}$$
  - Max. duty-cycle: $$d_{max} = \frac{I_{pri,peak}L_{pri}}{V_{in,min}}F_{sw,min} = \frac{3.32\times285\mu}{100}45k \Rightarrow \boxed{d_{max} = 0.43}$$
  - Primary rms current: $$I_{pri,rms} = I_{pri,peak}\sqrt{\frac{d_{max}}{3}} = 3.32\sqrt{\frac{0.43}{3}} \Rightarrow \boxed{I_{pri,rms} = 1.26A}$$
  - Secondary rms current: $$I_{sec,rms} = \frac{I_{pri,peak}}{N_{ps}}\sqrt{\frac{1-d_{max}}{3}} = \frac{3.32}{0.25}\sqrt{\frac{1-0.43}{3}} \Rightarrow \boxed{I_{sec,rms} = 5.8\,A}$$

Predicting the Switching Frequency

- The controller changes valley as the load decreases.
  => How can we predict the switching frequency evolution as the load varies ?



- Depending upon the power increase or decrease, the FB levels at which the controller changes valley are different => valley lockout

Predicting the Switching Frequency

- Knowing the FB threshold values, we can calculate F_{sw} evolution and the corresponding P_{out}.

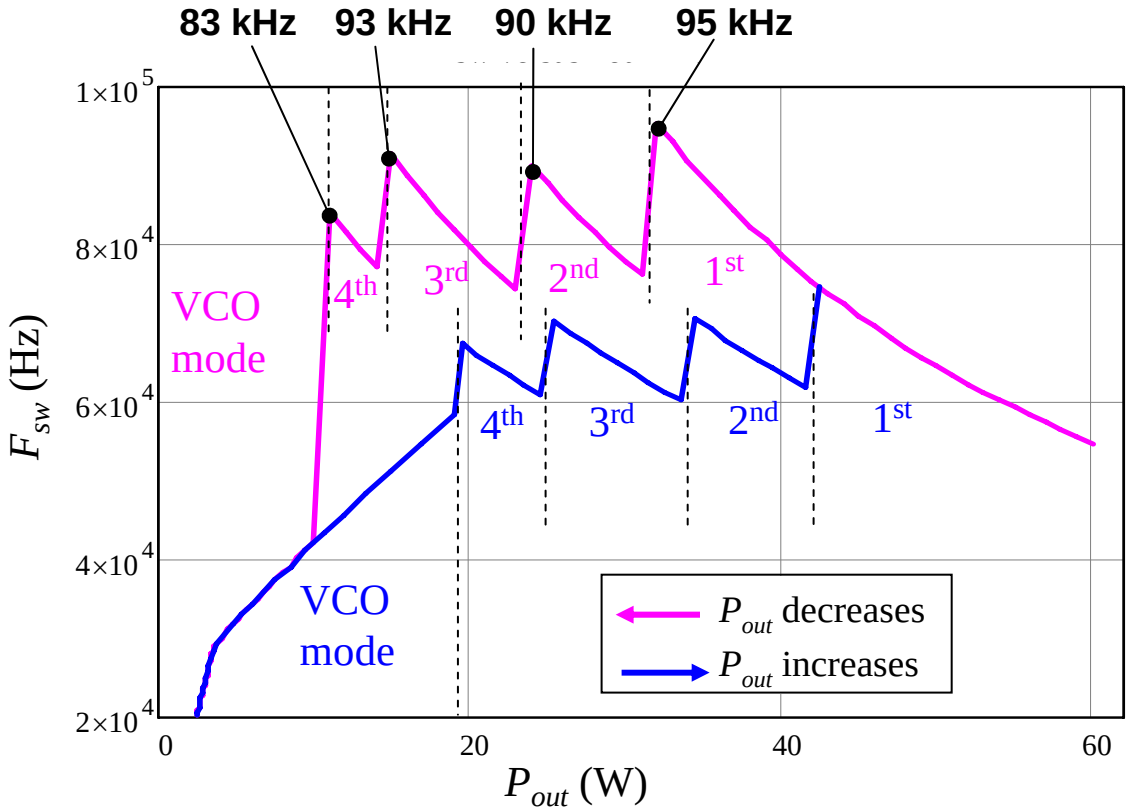
$$F_{sw} = \frac{1}{\left(\frac{V_{FB}}{4R_{sense}} + V_{in,dc}\frac{t_{prop}}{L_p}\right)L_p\left(\frac{1}{V_{in,dc}} + \frac{N_{ps}}{V_{out}+V_f}\right) + (1+2n)\pi\sqrt{L_p C_{lump}}}$$

$$P_{out} = \frac{1}{2}L_p\left(\frac{V_{FB}}{4R_{sense}} + V_{in,dc}\frac{t_{prop}}{L_p}\right)^2 F_{sw}\eta$$

Replace V_{FB} by the valley thresholds values in the previous slide

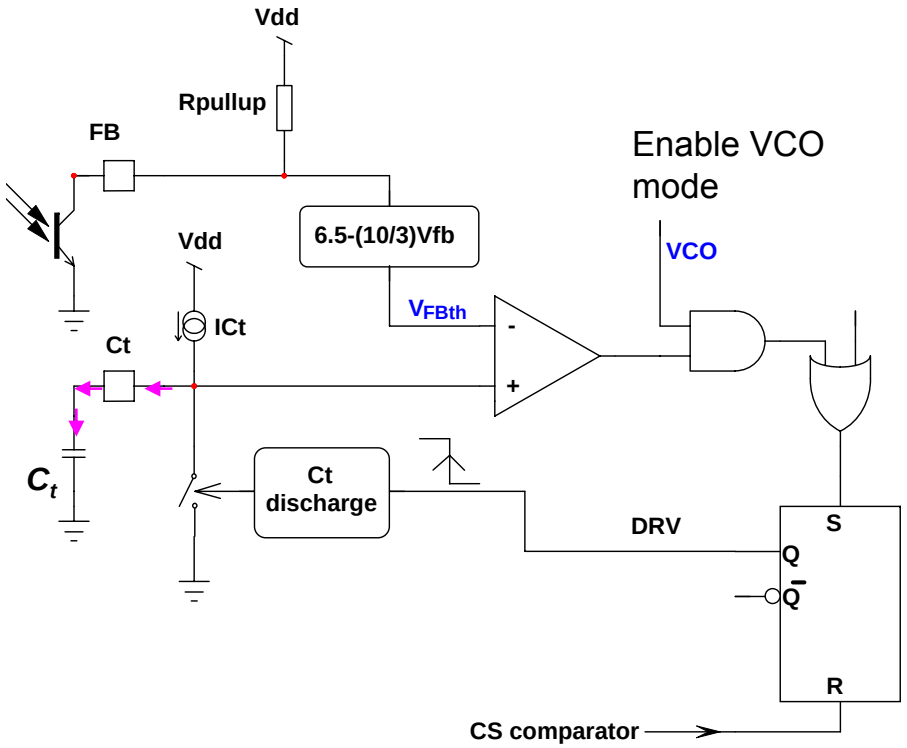
Predicting the Switching Frequency

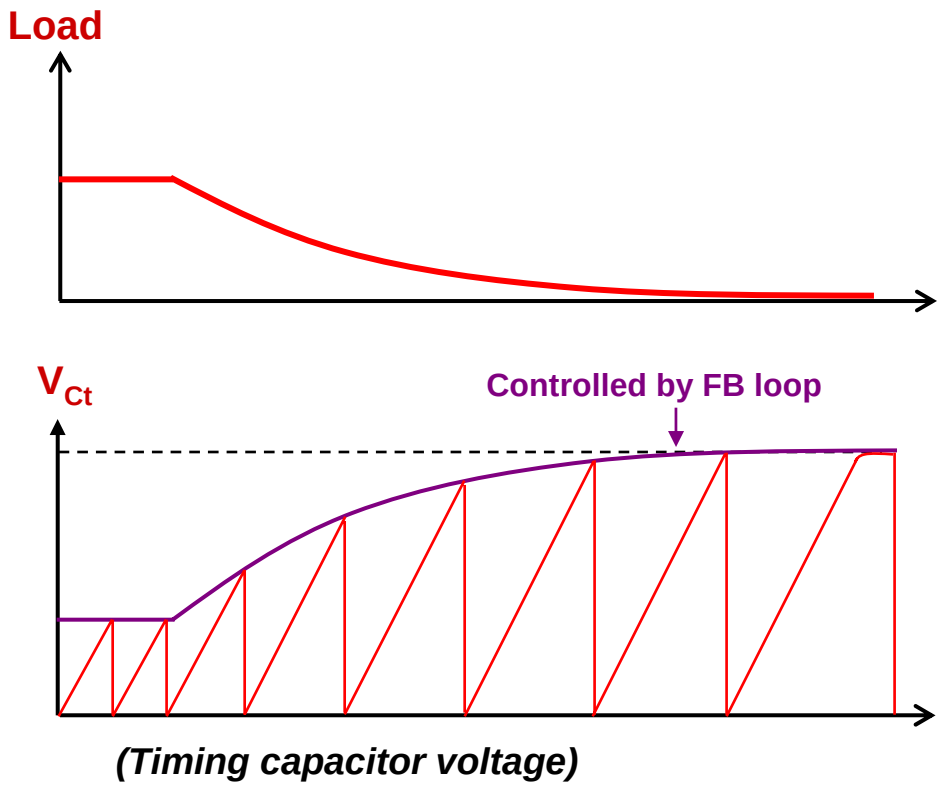
- Calculate by hand (using the previous equations) or use the Mathcad spreadsheet to deduce the maxima of the switching frequency => EMI



VCO Mode

- The switching frequency is set by the end of charge of C_t capacitor
- The end of charge of C_t capacitor is controlled by the FB loop

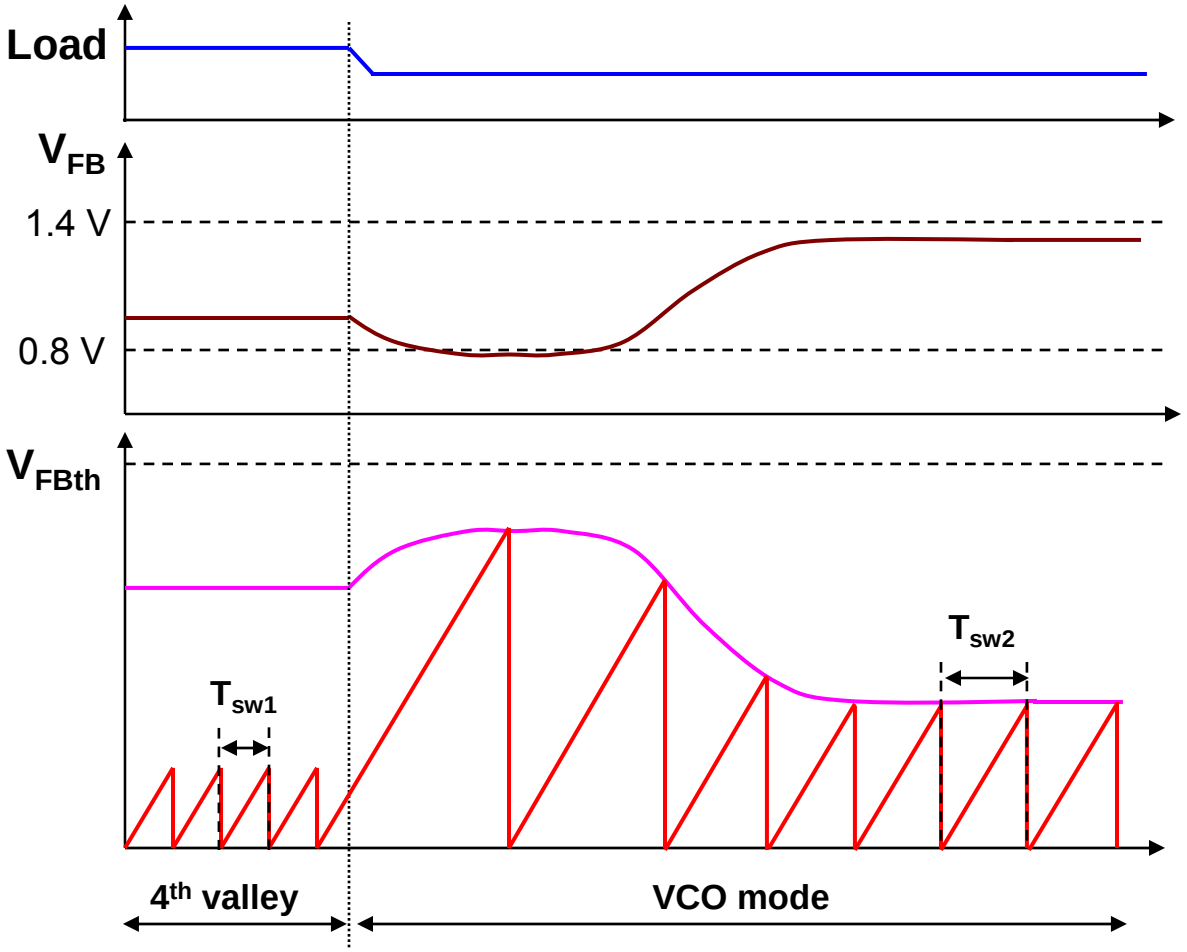




(Timing capacitor voltage)

4th Valley to VCO Mode Transition

- Output load slightly decreases:



How to Calculate C_t Capacitor ?

- Switching frequency at the end of the 4th valley operation (V_{FB} = 0.8 V):

$$T_{sw,4th-VCO} = \left(\frac{0.8}{4R_{sense}} + t_{prop} \frac{V_{in,max}\sqrt{2}}{L_p} \right) L_p \left(\frac{1}{V_{in,max}\sqrt{2}} + \frac{N_{ps}}{V_{out}+V_f} \right) + 7\pi\sqrt{L_p C_{OSS}}$$

- T_{sw} gap between 4th valley and VCO mode must not exceed **10 µs** (based on lab experiments) for V_{FB} = 1.4 V (hysteresis):

$$T_{sw,VCO} = T_{sw,4th-VCO} + 10\ \mu s$$

- The relationship between V_{FB} and V_{Ct} is:

$$V_{Ct} = 6.5 - (10/3)V_{FB} = 6.5 - (10/3) \times 1.4 = 1.83\,\text{V}$$

$$C_t = \frac{I_{Ct} T_{sw,VCO}}{1.83}$$

C_t Design Example

- Switching frequency at the end of the 4th valley operation :

$$T_{sw,4th-VCO} = \left(\frac{0.8}{4 \times 0.23} + 300n \frac{265\sqrt{2}}{285\mu} \right) 285\mu \left(\frac{1}{265\sqrt{2}} + \frac{0.25}{19 + 0.8} \right) + 7\pi \sqrt{285\mu \times 250p}$$

$$= 10.7\,\mu s$$

- T_{sw} gap between 4th valley and VCO mode must not exceed 10 µs (based on lab experiments):

$$T_{sw,VCO} = T_{sw,4th-VCO} + 10\ \mu s = 10.7\mu + 10\mu = 20.7\,\mu s$$

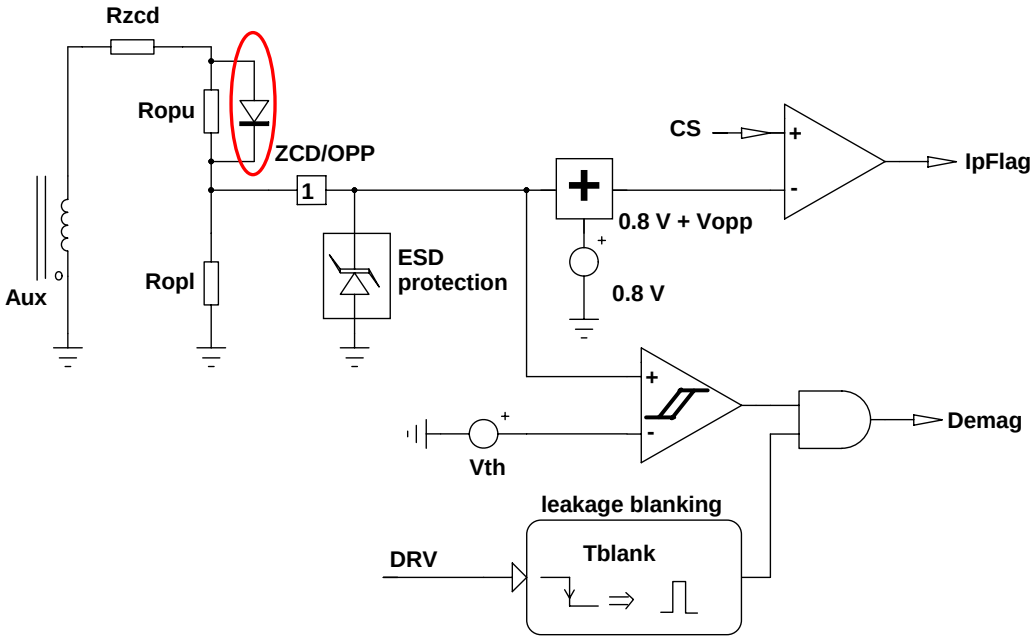
- The timing capacitor value is:

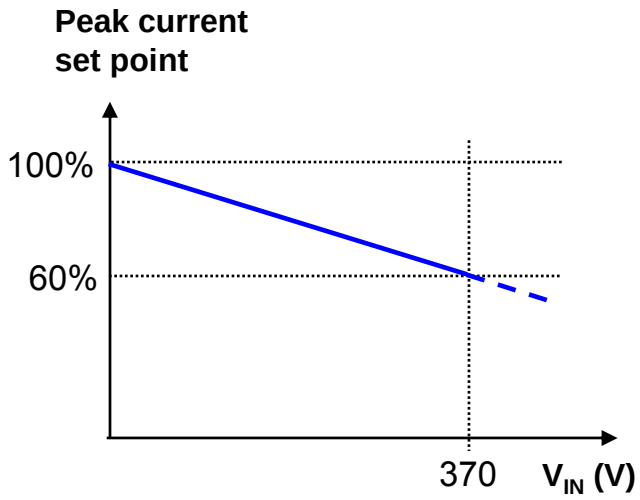
$$C_t = \frac{I_{Ct} T_{sw,VCO}}{1.83} = \frac{20\mu \times 20.7\mu}{1.83} = 226\,pF$$

- Finally, we choose C_t = 200 pF

OPP: How it Works ?

- L_{aux} with flyback polarity swings to $-NV_{IN}$ during the on time.
- Adjust amount of OPP voltage with $(R_{zcd}+R_{opu}) // R_{opl}$.
- $V_{CS,max} = 0.8\ V + V_{OPP}$
- The diode bypass R_{opu} during the off-time for optimum zero-crossing detection.





OPP Amount Needed for the Design

- Because of the propagation delay, at high line:

$$I_{pk(high)} = \frac{0.8}{R_{sense}} + V_{in,max}\sqrt{2}\frac{t_{prop}}{L_p} \quad \Rightarrow \quad I_{pk(high)} = \frac{0.8}{0.23} + 265\sqrt{2}\frac{600\times10^{-9}}{290\times10^{-6}} = 4.32\,A$$

- The switching frequency is:

$$T_{sw(high)} = I_{pk(high)}L_p\left(\frac{1}{V_{in,max}\sqrt{2}} + \frac{N_{ps}}{V_{out}+V_f}\right) + \pi\sqrt{L_pC_{lump}}$$

$$\Rightarrow \quad T_{sw(high)} = 4.32\times290\times10^{-6}\left(\frac{1}{265\sqrt{2}} + \frac{0.25}{19+0.8}\right) + \pi\sqrt{285\times10^{-6}\times250\times10^{-12}} = 19.5\,\mu s$$

- **The power capability at high line is**:

$$P_{out(high)} = \frac{1}{2}L_pI_{pk(high)}{}^2\frac{1}{T_{sw(high)}}\eta$$

$$\Rightarrow \quad P_{out(high)} = \frac{1}{2}290\times10^{-6}\times4.32^2\frac{1}{19.5\times10^{-6}}0.85 = 116\,W$$

Amount of OPP Voltage Needed

- Limit the output power to $P_{out(limit)}$ = 70 W at high line.
- What is the peak current $I_{pk(limit)}$ corresponding to $P_{out(limit)}$?

$$I_{pk(limit)} = \frac{L_p\left(\frac{1}{V_{in(max),dc}} + \frac{N_{ps}}{V_{out}+V_f}\right) + \sqrt{L_p{}^2\left(\frac{1}{V_{in(max),dc}} + \frac{N_{ps}}{V_{out}+V_f}\right)^2 - 2\frac{L_p\eta}{P_{out(limit)}}\pi\sqrt{L_pC_{lump}}}}{\frac{L_p\eta}{P_{out(limit)}}}$$

$$\Rightarrow I_{pk(limit)} = \frac{285\mu\left(\frac{1}{375} + \frac{0.25}{19+0.8}\right) + \sqrt{(285\mu)^2\left(\frac{1}{375} + \frac{0.25}{19+0.8}\right)^2 - 2\frac{285\mu\times 0.85}{70}\pi\sqrt{285\mu\times 250p}}}{\frac{285\mu\times 0.85}{70}} = 2.67\ A$$

- Amount of OPP voltage needed:

$$V_{OPP} = 0.8\left(1 - \frac{I_{pk(limit)}}{I_{pk(max)}}\right)$$

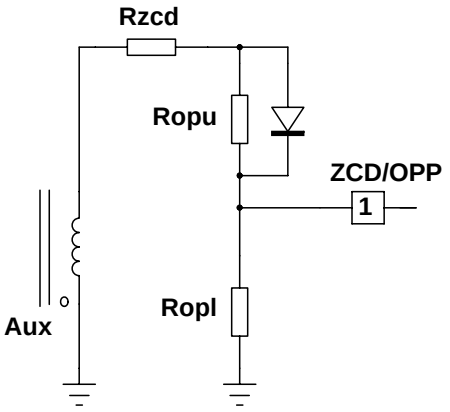
$$\Rightarrow V_{OPP} = 0.8\left(1 - \frac{2.67}{4.32}\right) = 300\ mV$$

Calculating the OPP Resistors

- The amount of OPP voltage needed to limit P_{out} to 70 W is : V_{OPP} = 300 mV

- Resistor divider law:

$$\frac{R_{opu}+R_{zcd}}{R_{opl}}=\frac{N_{p,aux}V_{IN}-V_{OPP}}{V_{OPP}}$$



$$\Rightarrow \frac{R_{opu}+R_{zcd}}{R_{opl}}=\frac{0.18\times 375-0.3}{0.3}=224$$

- We choose: R_{opl} = 1 kΩ and R_{zcd} = 1 kΩ

$$R_{opu}=221R_{opl}-R_{zcd}$$

$$\Rightarrow R_{opu}=223k\Omega$$

Why is the OPP Non Dissipative ?

- Input voltage information given by auxiliary winding
- In light load: VCO mode => T_{sw} expands, thus the average current in the resistor bridge decreases

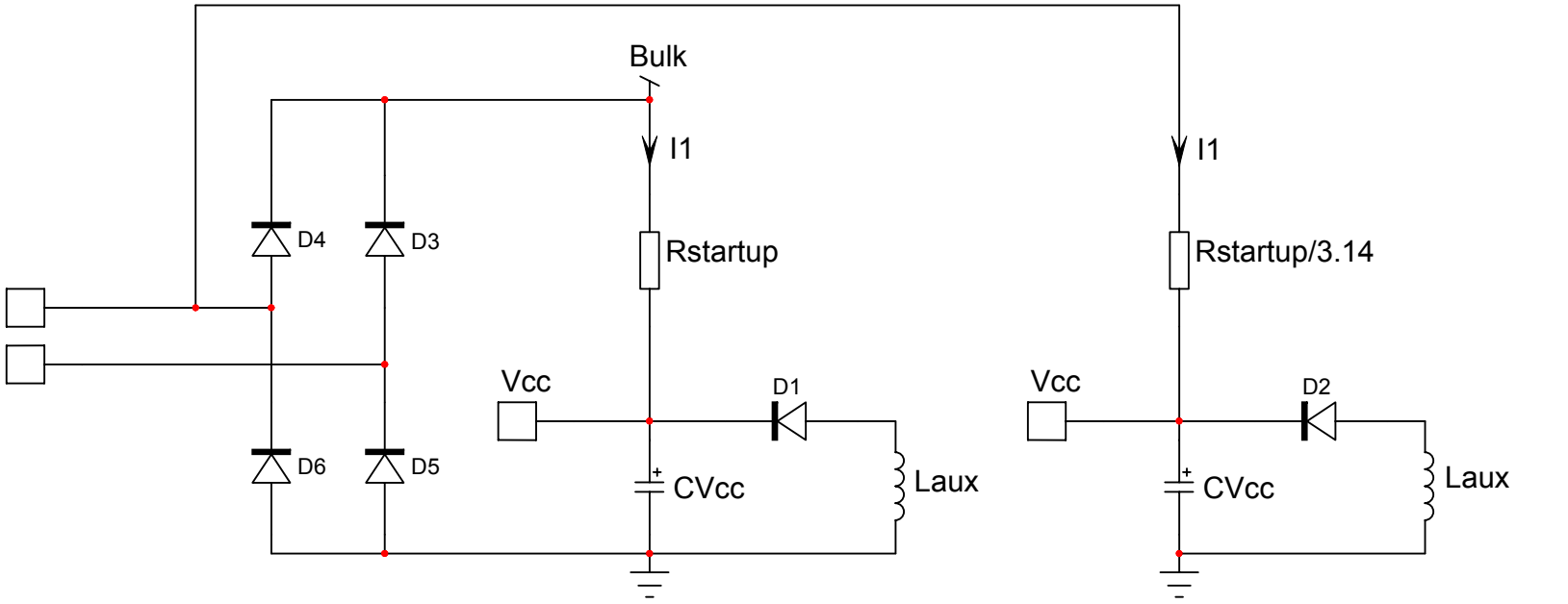
$$I_{bridge,avg} = \frac{1}{R_{zcd} + R_{opu} + R_{opl}} \frac{t_{on}}{T_{sw}} N_{p,aux} V_{IN} + \frac{1}{R_{opu} + R_{opl}} \frac{t_{off}}{T_{sw}} \left(V_{CC} + V_f \right)$$

➢ Previous example: R_{opu} = 220 kΩ, R_{opl} = 1 kΩ, R_{zcd} = 1 kΩ

At light load (P_{out} = 4 W), t_{on}= 1.2 µs, t_{off} = 3.6 µs, T_{sw} = 40 µs

$$I_{bridge,mean} = \frac{1}{220k + 1k + 1k} \frac{1.2\mu}{40\mu} \times 0.18 \times 375 + \frac{1}{220k + 1k} \frac{3.6\mu}{40\mu} 16 = 15\ \mu A$$

Startup Network



Classical configuration

Improved startup dissipation

- The startup resistor can either be connected:
  - To the bulk capacitor with $R_{startup}$
  - To the half-wave – for a similar charging current, take $R_{startup}$ /π

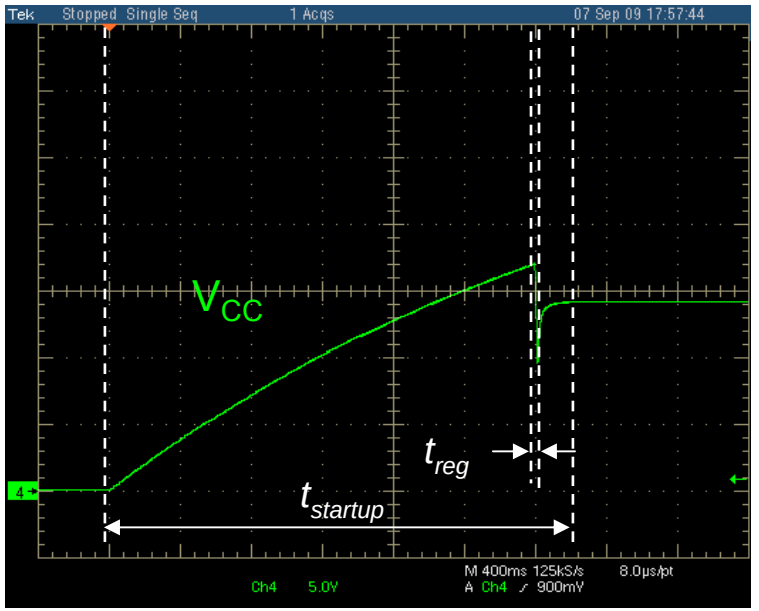
Startup Capacitor Calculation

- C_{Vcc} calculated to allow the power supply to close the loop before V_{CC} falls below $V_{CC(off)}$

$$C_{Vcc} = \frac{\left(I_{CC3A} + Q_g F_{sw}\right) t_{reg}}{V_{CC(on)} - V_{CC(off)}}$$

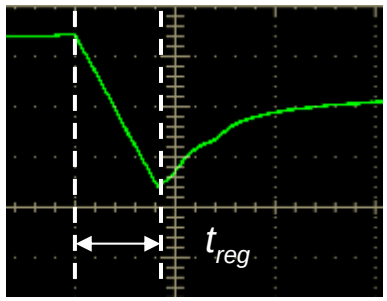
$$C_{Vcc} = \frac{\left(2.4m + 17n \times 45000\right) \times 10m}{17 - 9} = 3.9\,\mu F$$

We choose $\boldsymbol{C_{Vcc}}$ **= 4.7 µF**



- Needed startup current to charge C_{Vcc}:

$$I_{Cvcc} = \frac{V_{CC(on)} C_{Vcc}}{t_{startup}} \quad \Rightarrow \quad I_{Cvcc} = \frac{17 \times 4.7\mu}{2.8} = 28.5\,\mu A$$



Startup Resistor Calculation

- **Bulk capacitor connection**
  - Resistor calculation:

$$R_{startup} = \frac{V_{in,min}\sqrt{2}}{I_{Cvcc} + I_{CC(start)}}$$

$$R_{startup} = \frac{85\sqrt{2}}{28.5\mu + 15\mu} = 2.76\,M\Omega$$

  - Power dissipation:

$$P_{startup} = \frac{\left(V_{in,max}\sqrt{2} - V_{CC}\right)^2}{R_{startup}}$$

$$P_{startup} = \frac{\left(265\sqrt{2} - 16\right)^2}{2.68M} = 55\,mW$$

- **Half wave connection**
  - Resistor calculation:

$$R_{startup} = \frac{\frac{V_{in,min}\sqrt{2}}{\pi}}{I_{Cvcc} + I_{CC(start)}}$$

$$R_{startup} = \frac{85\sqrt{2}/\pi}{28.5\mu + 15\mu} = 880\,k\Omega$$

  - Power dissipation:

$$P_{startup} = \frac{\left(\frac{V_{in,max}\sqrt{2}}{\pi} - V_{CC}\right)^2}{R_{startup}}$$

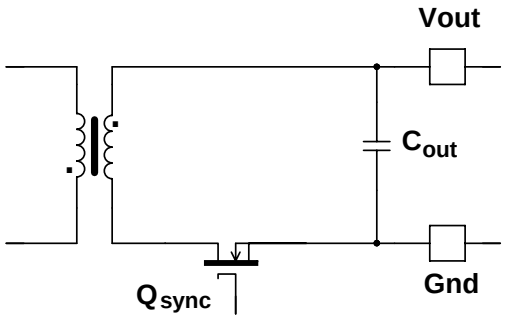
$$P_{startup} = \frac{\left(265\sqrt{2}/\pi - 16\right)^2}{880k} = 16\,mW$$

Half wave connection saves 39 mW !

Synchronous Rectification

- High rms currents in secondary side → increased losses in the output diode.
- Replace the diode with a MOSFET featuring a very low $R_{DS(on)}$.

+	-
Increased efficiency	Degraded light load and standby power consumption



Losses in the Sync. Rect. Switch

$$P_{Qsync} = P_{ON} + P_{Qdiode}$$

- Body diode conduction losses

$$P_{Qdiode} = V_f I_{out} F_{sw} t_{delay}$$

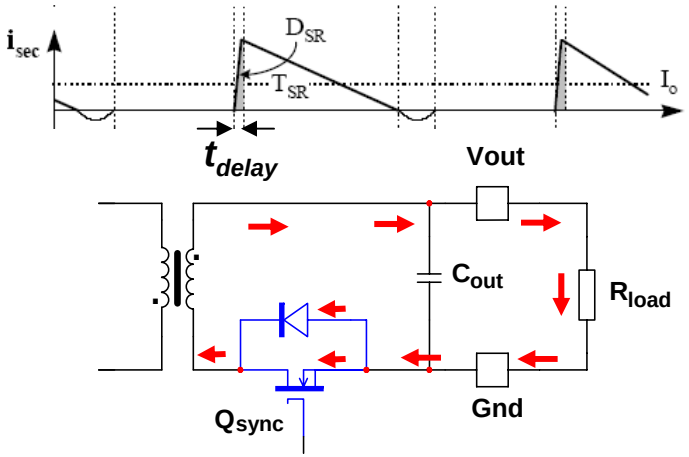
➡ Low if t_{delay} small

- MOSFET conduction losses

$$P_{ON} = R_{DS(on)120} I_{sec,rms}^{\ 2}$$

- Body diode conducts before the MOSFET is turned-on.

➡ No switching losses



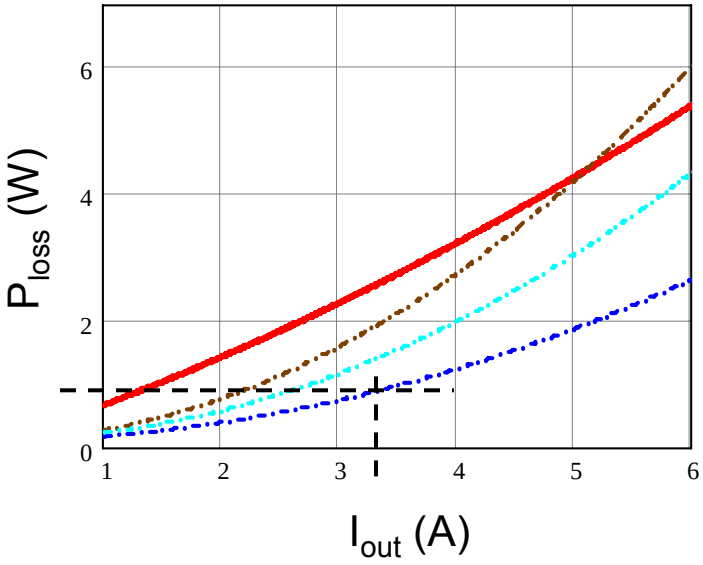
- **Losses in the Sync. Rect. switch are mainly conduction losses.**

Choosing the Sync. Rect. MOSFET

- Target around 1 W conduction losses in Sync. Rect. switch to avoid using an heatsink.

$$R_{DSon120} = \frac{1W}{I_{sec,RMS}^{\ 2}}$$

V_{out} = 19 V
$F_{sw,min}$ = 45 kHz
Universal mains



$R_{DSon110}$ = 70 mΩ

MBR20H150

$R_{DSon110}$ = 50 mΩ

$R_{DSon110}$ = 30 mΩ

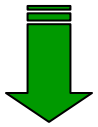
60 W QR Sync. Rect. Calculations

- Body diode losses: $P_{Qdiode} = V_f I_{out} F_{sw} t_{delay} = 0.7 \times 3.2 \times 45000 \times 70n$

  $P_{Qdiode} = 7\,mW$

- MOSFET losses: $P_{ON} = R_{DS(on)120} I_{sec,rms}{}^2 = 30m \times 5.8^2$

  $P_{ON} = 1W$



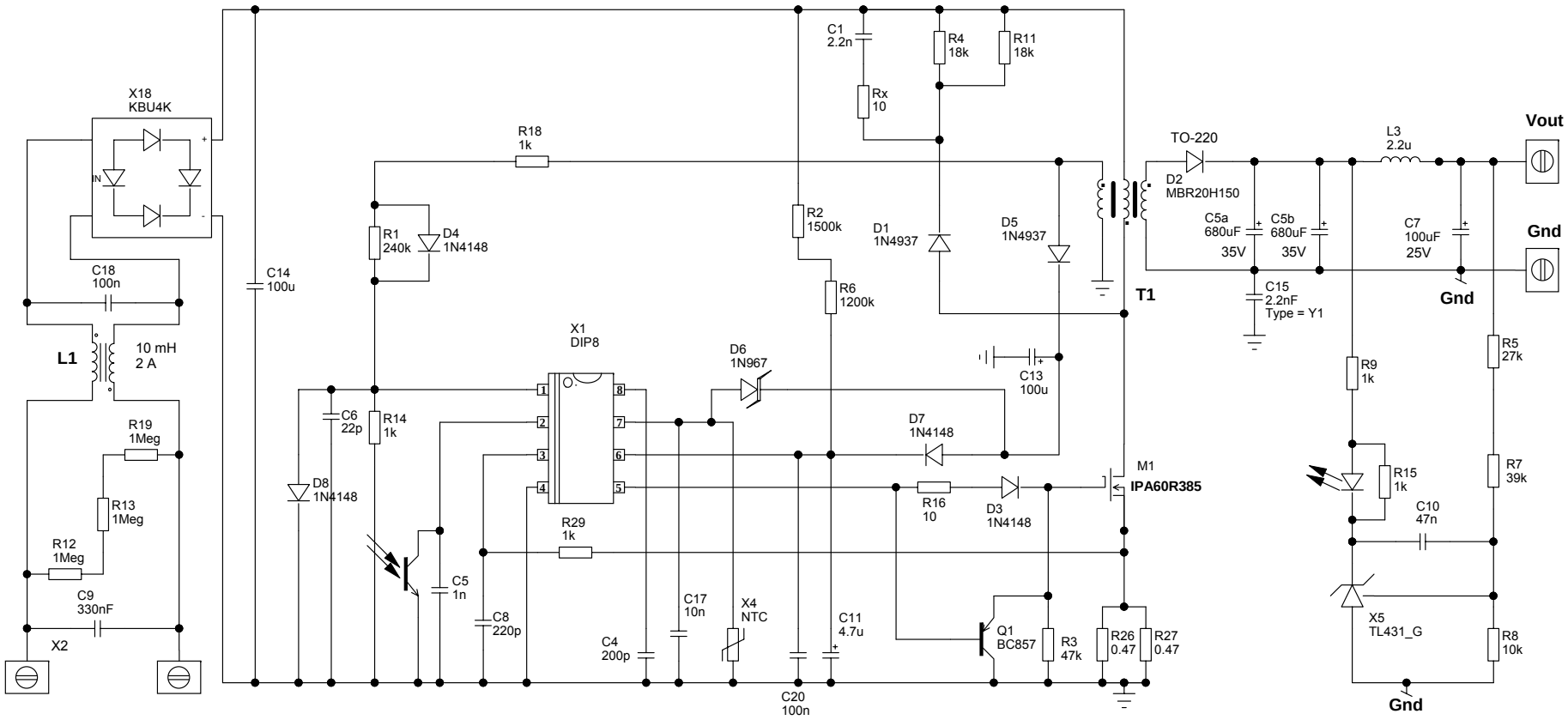
- Total Sync. Rect. switch losses: $P_{Qsync} = 1 + 0.007 \approx 1W$
- Losses into the MBR20200 diode: 2.6 W

Power loss saving: 1.6 W

Agenda

1. Quasi-Resonance (QR) Generalities
2. The valley lockout technique
3. The NCP1379/1380
4. Step by step design procedure
5. Performances of a 60 W adapter featuring valley lockout

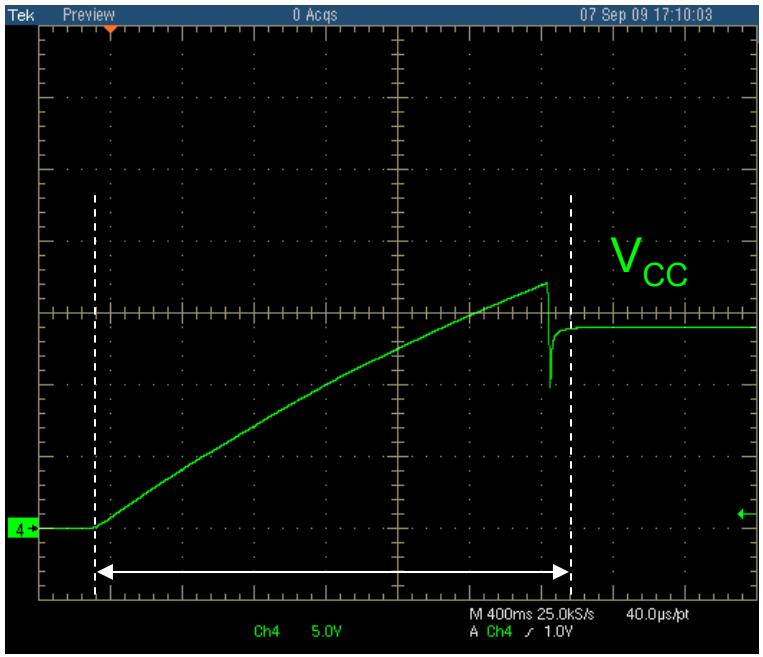
60 W Demo Board Schematic



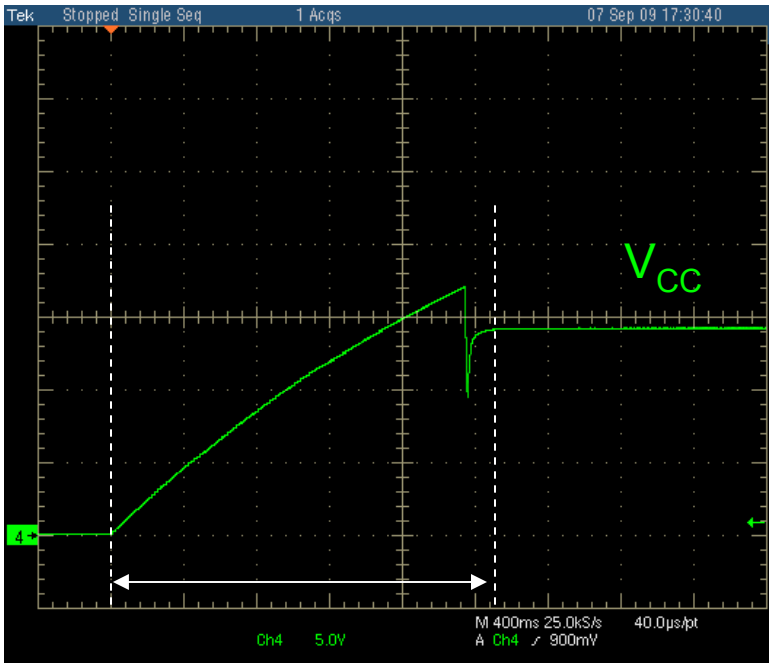
NCP1380B in a 19 V, 60 W adapter

Startup

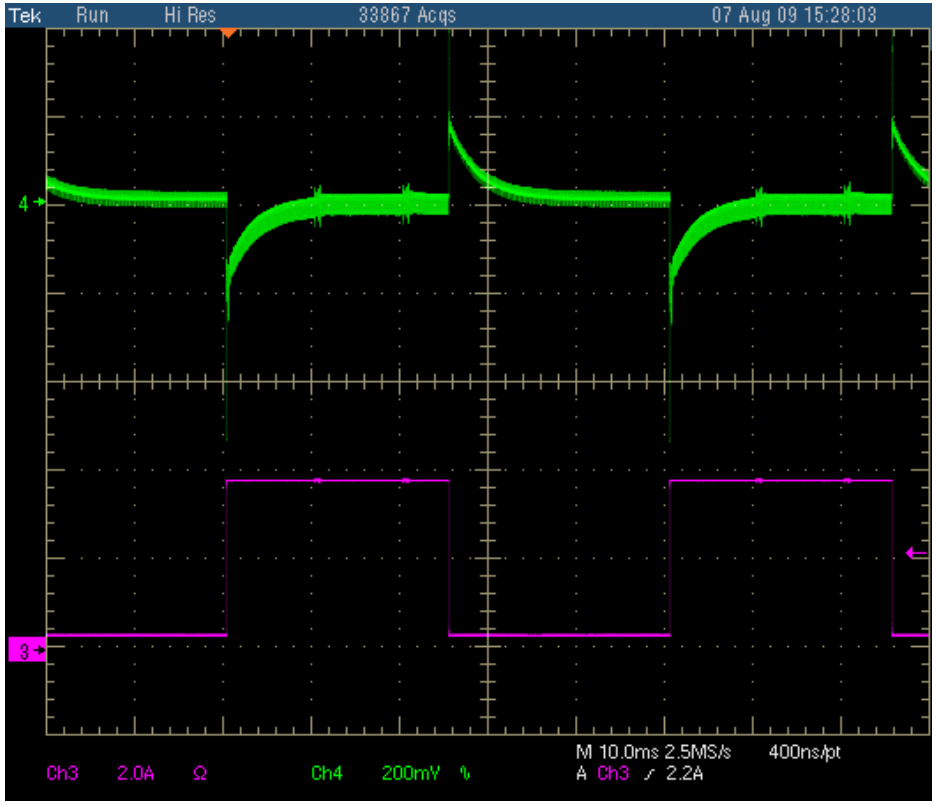
- Startup resistor connected to the **bulk rail** ($R_{startup}$ = 2.7 MΩ)
- $T_{startup}$ = 2.68 s



- Startup resistor connected to the **half-wave** ($R_{startup}$ = 910 kΩ)
- $T_{startup}$ = 2.1 s



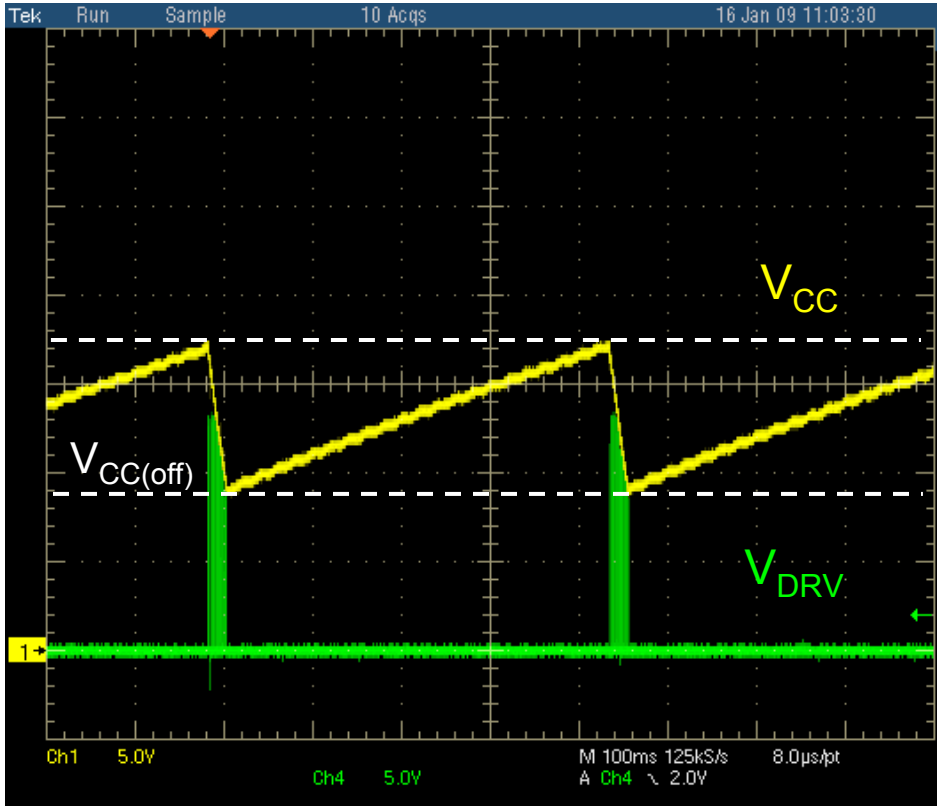
Transient Load Step



- Load step:
  3% to 100% of output load
  with a slew rate of 1 A / µs
- V_{in} = 230 Vrms

The overshoot / undershoot is 1% of the nominal value of V_{out}

Short-Circuit



- A short-circuit is made at the board output.
- The circuit pulses with a low burst (5%)
- The measured averaged input power is: P_{in} = 412.4 mW for V_{in} = 230 Vrms

Efficiency

115 Vrms			
P_{out} (W)	P_{out} (%)	P_{in} (W)	Eff. (%)
60.6	**100**	68.65	**88.3**
45.5	**75**	51.29	**88.7**
30.3	**50**	34.40	**88.2**
15.2	**25**	17.61	**86.4**
1.0		1.30	76.4
0.7		**0.94**	**74.5**
0.5		0.69	72.0

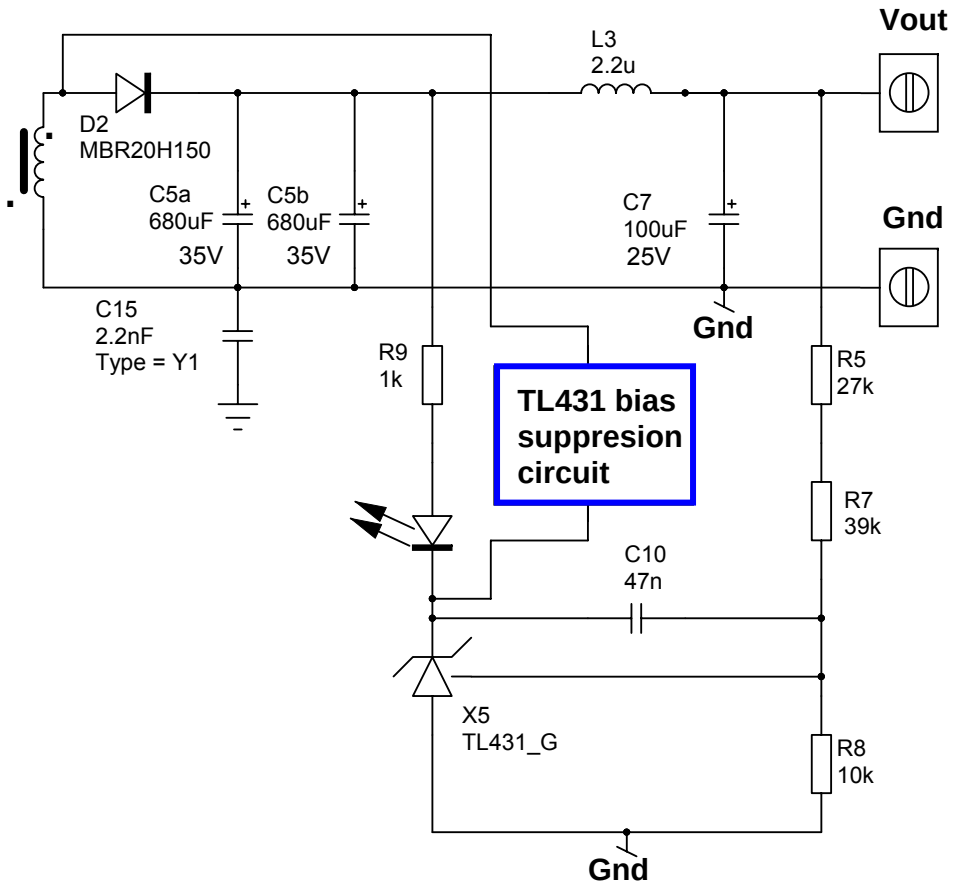
Average efficiency
(25, 50, 75, 100% of $P_{out,max}$): **87.9%**

230 Vrms			
P_{out} (W)	P_{out} (%)	P_{in} (W)	Eff. (%)
60.6	**100**	68.00	**89.1**
45.5	**75**	51.43	**88.4**
30.3	**50**	34.78	**87.3**
15.2	**25**	17.66	**86.1**
1.0		1.325	75.4
0.7		**0.958**	**73.0**
0.5		0.71	70.2

Average efficiency
(25, 50, 75, 100% of $P_{out,max}$): **87.7%**

Improving the No Load Consumption

- At very low output load, the TL431 bias is removed using a special circuit:



No Load Consumption

- $R_{startup}$ connected to the bulk rail:
  - Without TL431 bias:

	115 Vrms	230 Vrms
P_{out} = 0 W	P_{in} = **60** mW	P_{in} = **98** mW

  - With TL431 bias:

	115 Vrms	230 Vrms
P_{out} = 0 W	P_{in} = **98** mW	P_{in} = **128** mW

3 MΩ resistor to discharge X2 capacitor included

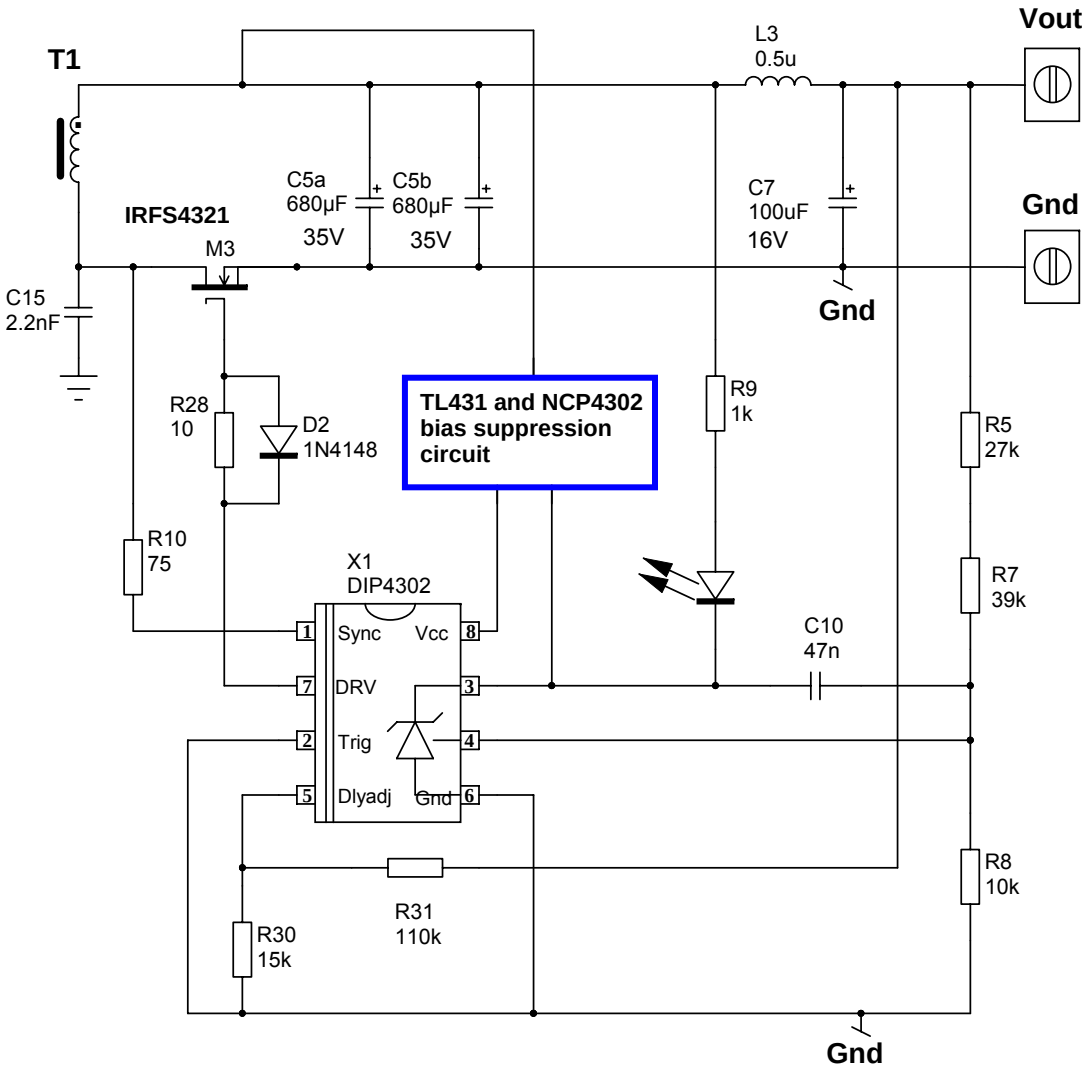
No Load Consumption

- $R_{startup}$ connected to the half wave:
  - Without TL431 bias, $R_{startup}$ = **1.1 MΩ** ($T_{startup}$ = 2.6 s @ 85 Vrms)

	115 Vrms	230 Vrms
P_{out} = 0 W	P_{in} = **55** mW	P_{in} = **90** mW

3 MΩ resistor to discharge X2 capacitor included

Synchronous Rectification Schematic



- TL431 and NCP4302 bias removed at light load.

Efficiency and No Load Consumption

115 Vrms			
P_{out} (W)	P_{out} (%)	P_{in} (W)	Eff. (%)
60.5	**100**	67.18	**90.1**
45.4	**75**	50.23	**90.5**
30.3	**50**	33.78	**89.8**
15.2	**25**	17.39	**87.4**
1.0		1.319	75.7
0.7		**0.945**	**74.0**
0.5		0.690	72.4

Average efficiency (25, 50, 75, 100% of $P_{out,max}$): **89.5%**

230 Vrms			
P_{out} (W)	P_{out} (%)	P_{in} (W)	Eff. (%)
60.5	**100**	66.48	**91.0**
45.4	**75**	50.38	**90.1**
30.3	**50**	34.2	**88.6**
15.2	**25**	17.48	**86.8**
1.0		1.368	72.9
0.7		**0.992**	**70.5**
0.5		0.737	67.6

Average efficiency (25, 50, 75, 100% of $P_{out,max}$): **89.1%**

❑ **No load consumption:**

	115 Vrms	230 Vrms
P_{out} = 0 W	P_{in} = **62** mW	P_{in} = **107** mW

Conclusion

- The valley lockout technique allows to solve the valley jumping problem in QR power supplies.
- NCP1380, NCP1379 features:
  - QR current-mode with valley lockout for noise immunity for high load.
  - VCO mode in light load for improved efficiency.
  - OPP, OVP, BO, OTP, soft-start for building safe power supplies
- A complete design method has been presented.
- It is possible to achieve standby power consumption below 100 mW at 230 Vrms with the NCP1380.
- Good efficiency at light load with Sync. Rect if the bias of the TL431 and the Sync. Rec. controller is removed.
- Mathcad spreadsheet and simulations models available.

For More Information

- View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com
- View reference designs, design notes, and other material supporting the design of highly efficient power supplies at www.onsemi.com/powersupplies