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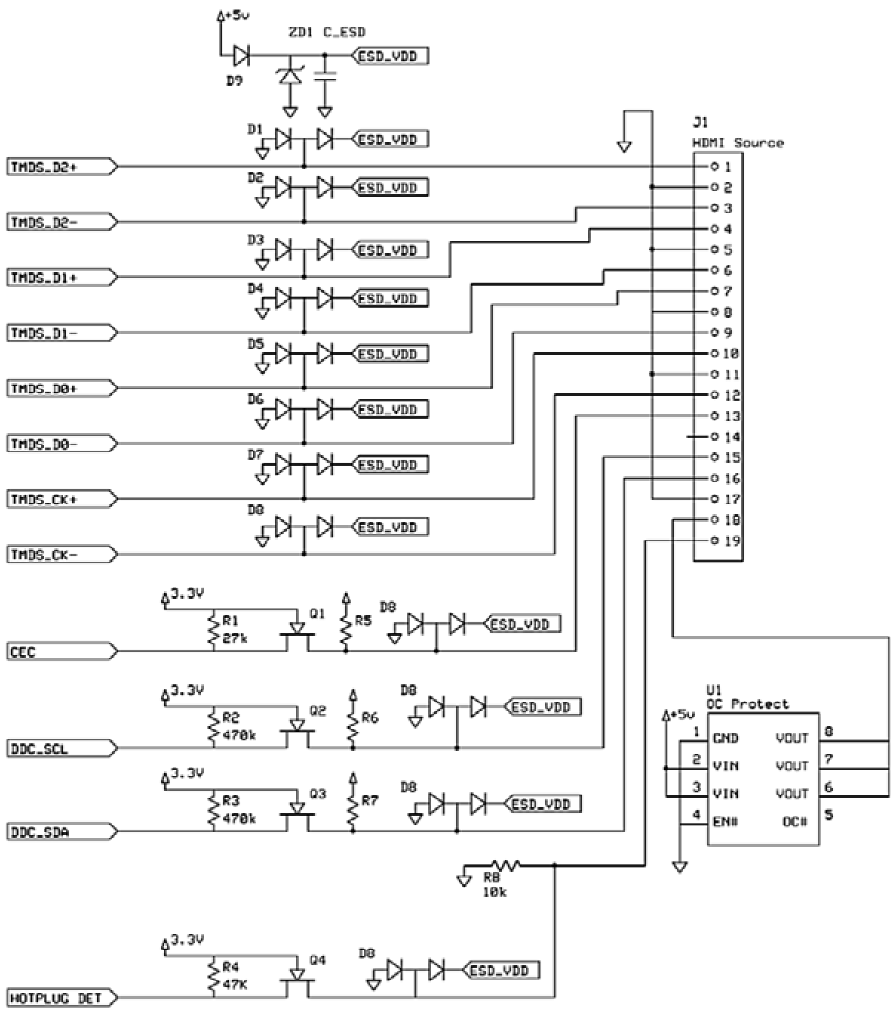
# Interface Protection for HDMI

## Introduction

The High-Definition Multimedia Interface (HDMI) combines a high-speed unidirectional TMDS data link with low speed, bidirectional control and status links (DDC and CEC) and configuration protocols in a single user-friendly high-performance connector.

"Ease of use" for such a complex interface implies a certain durability and ruggedness in the consumer electronics environment.  Delicate signaling and precise protocols must endure serious misuse without complaint.  For example, the "same connector on each end" implementation mimics the simplicity of RCA phono jacks, which can be plugged into illegal configurations via "adapter" cables, or can be used to connect two outputs together erroneously.  Additionally, for any I/O signal exposed to the outside world, ESD strikes are a constant danger during interconnection.  A single spark can render an entire entertainment system useless.

The high-performance digital imaging silicon ASICs required for these applications usually include some protection sufficient for a controlled manufacturing environment.  But the physics of their deep sub-micron fabrication geometry must be optimized for performance, not ruggedness, and is no match for the uncontrolled ESD environment of the end-user.  Therefore, even the most basic HDMI port implementation for these applications necessarily entails multiple external interface and protection circuits.  The diagram below shows a discrete implementation of all the necessary and desirable interface protection and isolation functions.



Here, each TMDS line is protected from ESD with a low-capacitance Dual Rail Clamp diode pair that routes negative ESD pulses directly into ground, and positive pulses back to ground through a zener diode.  Each of the signal lines exposed to the HDMI connector are protected in this manner.  All of these clamps are further prevented from providing a DC backdrive path through a blocking circuit from the biasing supply.

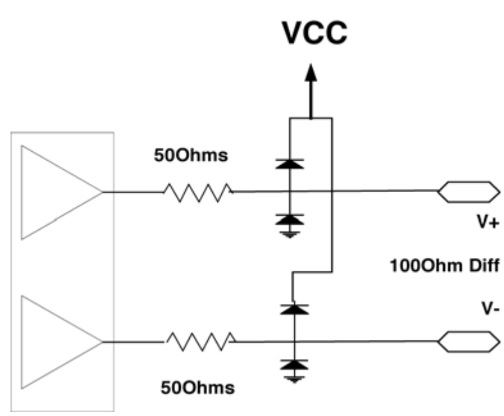
In the discrete schematic above, there are hidden implementation pitfalls that may not be initially obvious.  These potential hazards include impedance and layout tuning for TMDS lines, appropriate threshold voltages and RDS(on) characteristics of level shifting NFETs, ESD clamp levels, response times and matched parasitic inductance, overcurrent protection for outputs, and backdrive protection for all signals.

Successful high speed TMDS differential signal routing is a complex system design challenge in itself.  Adding even the most minute parasitic loading for ESD protection to these finely tuned transmission lines can often be the difference between pass or fail.  The resulting transmission line characteristics and impedance matching cannot be easily predicted from mere component level specifications, and indeed, some counter-intuitive results may be observed.  For example, adding trace inductance or stubs can, in certain cases, actually improve the characteristic impedance of the line while retaining optimal ESD clamping.

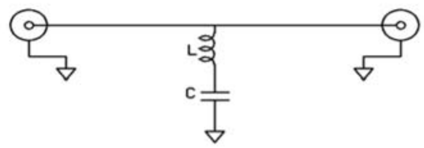
ESD protection and backdrive protection are important on each and every external signal line, especially with multiple power domain entertainment systems (DVD, HDTV, Satellite Receiver, Audio Decoders, etc.).  While the need for ESD clamps on exposed signal lines is obvious, the potential for backdrive and its ill effects is not always apparent, even with rigorous system testing.  Early PCs with CMOS parallel ports experienced this problem with certain printers upon the advent of soft power management.  Upon entering power-saving states, the PC would shut down its internal power planes while external peripherals - such as printers - were still powered from their own sources.  In some cases, often via output ESD clamps, a forward biased path was energized that could "charge" the bulk capacitance of the internal power planes with mere milliamperes.  This unexpected voltage level could cause problems with Power-On-Reset circuits causing the system to hang on recovery from standby states. Obviously, in the modular digital entertainment systems enabled by HDMI, this potential complication with independent power management also exists.

**TMDS Protection**

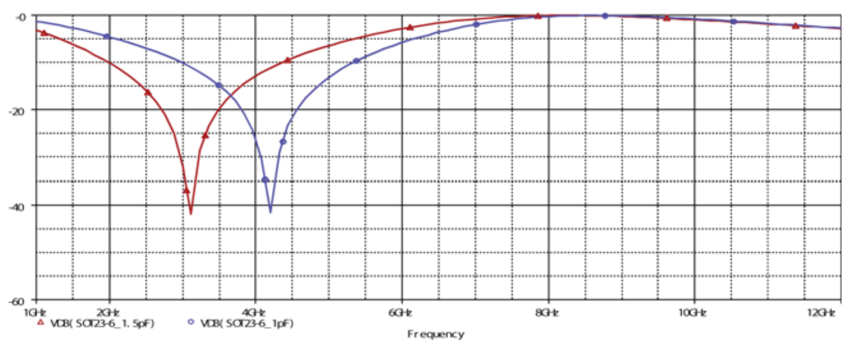
A dual-rail clamp ESD protector's primary function is to shunt high-voltage ESD pulses off of the TMDS node by presenting a very low impedance dynamic path to ground, away from the delicate HDMI or DVI PHY logic.  During normal operation, though, it is imperative that the impact of the parasitic inductance and capacitance of the ESD device be minimized.



The channel capacitance of the reverse biased ESD clamp diodes and the parasitic series inductance of the package leads and bond wires (shown below) create a lumped resonant LC tank circuit that creates a low impedance shunt at the natural self-resonance frequency of the device.

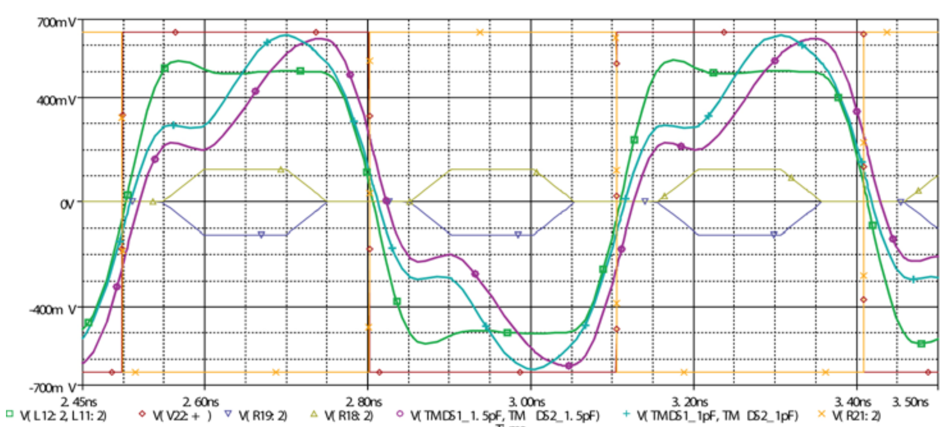



The impedance at this resonant frequency and the quality factor (Q) of the insertion loss notch determine how much this resonance point will distort the signal. The following plot shows the range of possible resonant frequencies for a SOT-23-6 package with 1.0 to 1.5 pF of channel capacitance (approximately 3.1 GHz with 1.5 pF to 4.2 GHz with 1.0 pF).

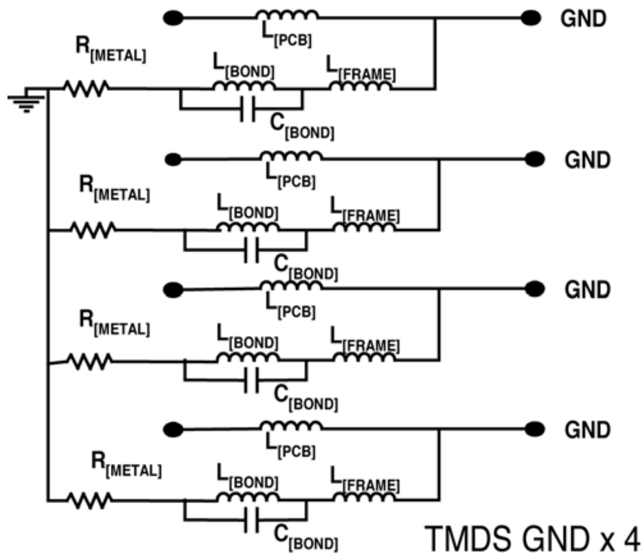



The maximum transition rate of the data on a TMDS pair at 165 MHz is 1.65 GHz (with a square wave having odd harmonics at 4.95 GHz, 8.25 GHz, and so on.)

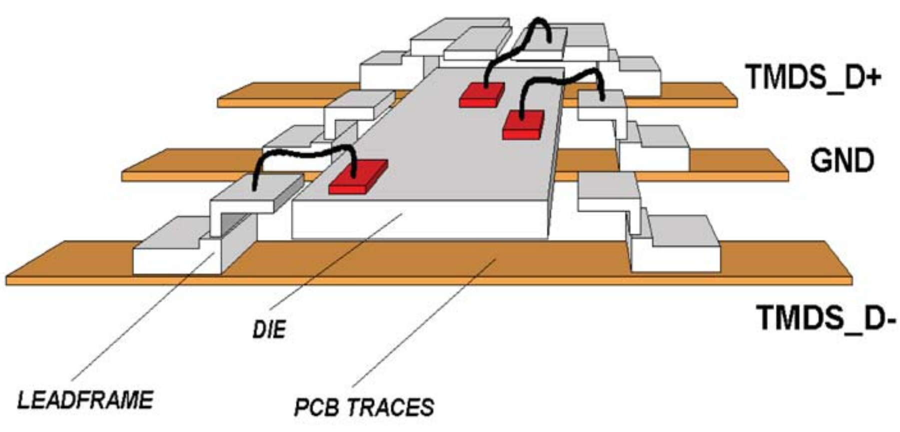
The extent to which the parasitic self-resonance notch attenuates the spectral components of the signal non-linearly determines the amount and shape of the deformation of the resultant waveform. (Increasing {GRN/BLU/AQUA} effect of parasitic capacitance shown below on a 1.65 GHz square wave.)



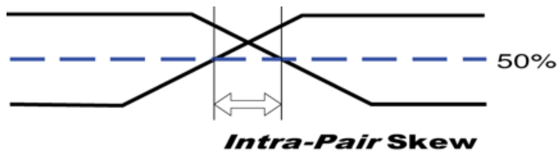
The actual parasitic model of a protection component has multiple elements, in addition to the complex and difficult to control PCB elements. The "GROUND" of the protection device is isolated from the "GROUND" on the PCB and is yet again isolated somewhat from the Return "GROUND" at the HDMI connector. The self-resonance frequency and thus the parasitic insertion loss notch can be moved higher by minimizing the inductance in this return path via optimization of the ground paths in the protection IC(s). Increasing the number of paralleled ground pins on a given package, for example, can help in this manner.

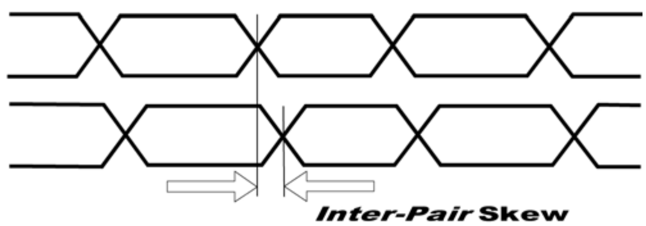



The complexity of these factors, hidden by the simplicity of a schematic diagram, are obviated in the following 3D depiction of a protection integrated circuit. The elevated lead frame shape, the permeability of the plastic molding, the height of the silicon die and of course wire bond diameter and length are all contributing factors to the resulting parasitic impedance and RF frequency response of the high-speed traces.



Minimizing parasitic effects by reducing their magnitude is a priority in HDMI interface protection design, but matching the parasitics can often be even more important. Slight variations in parasitic inductance or capacitance, can create critical phase distortion in the parallel TMDS signals. While the clock recovery system is more forgiving for inter-pair skew, the intra-pair skew is specified very tightly. Intra-pair skew shifts the crossing level of the D+/D- lines away from the optimal 50% level, thus reducing available margin in the recoverable signal eye-diagram.



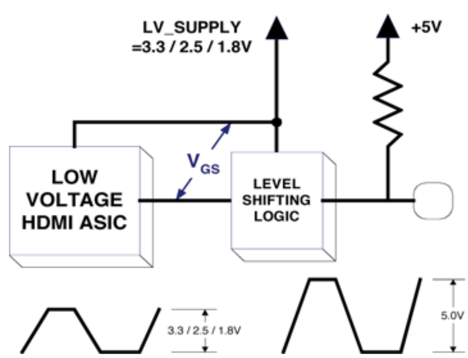

The HDMI Specification, Version 1.1 specifies "Intra-Pair Skew at Source Connector," at a maximum of 0.15*Tbit, or less than about 90 ps @ 1.65 GHz. "Inter-Pair Skew at Source Connector" is a more "relaxed" 0.20*Tpixel, or less than about 1.2 ns @ 165 MHz.

In a sample package, a variance of 0.02 pF channel-to-channel, can produce negligible variations in both inter- and intra-pair skew on the order of 5-6 ps. A variance of 0.2 pF (min-to-max or sample-to-sample) can introduce more than 60 ps of fixed skew on a given design, independent of connector and PCB considerations. Detailed attention to matching protection device parasitics at the component level enhances the performance margins as well as the robustness and durability of the design.

**Level Shifting**

Many advanced HDMI/DVI controller chips provide "5 Volt Tolerant" inputs. These controllers use advanced high-speed sub-micron CMOS processes, especially when they are integrated with the physical layer transceivers of the TMDS links, and the physical implementation of the I/O structures are not capable of withstanding the abuse present in the demanding consumer electronics environment.

These devices may be very capable of shifting 5 V and 3.3 V levels between the ASIC and other internal circuitry, but connecting the DDC, CEC, or even Hotplug Detect I/O signals directly to external HDMI pins subjects the respective controller ASIC to a much more rigorous and uncontrolled environment. Even when the ASIC provides tolerant I/O cells, it can be beneficial to use an external level shifter for further isolation and backdrive protection.

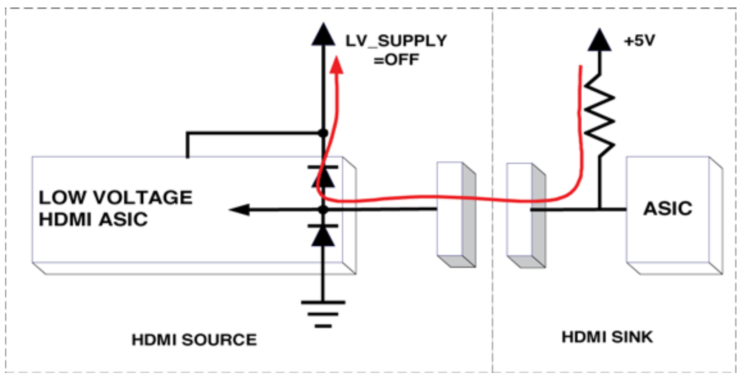


Simple NFET level translation techniques use the bidirectional nature of the FET and the low threshold voltage to "clamp" the lowside of the protection block to a reference voltage, such as the VDD of the low-voltage ASIC. Unexpected glitches and peaks that might normally destroy these integrated "tolerant" structures are easily absorbed by the relatively higher power external devices.

**Backdrive Protection**

Every external signal is a potential backdrive problem, especially output signals with pullups at the other end of the cable. For bidirectional DDC and CEC lines, the backdrive condition is a potential problem on both the HDMI Source and Sink side.

Internal ESD clamp diodes (provided in ASICs for typical 2 kV manufacturing ESD protection) can provide a direct path for pullups on the other end of the cable to "seep" current into the local LV VDD rail, possibly causing Power-On-Reset issues if the "off" rail starts at a higher voltage than expected when turned "on."




Additionally, the HDMI Specification demands a fairly broad level of robustness beyond this potential functional anomaly.

> **Section 4.2.11 Robustness Requirements**
> *No damage to the HDMI Source or Sink can result from the shorting of any combination of signals on any connector. If two HDMI Sources are connected together with a single cable, no damage can occur to either of the Sources. If two HDMI Sinks are connected together with a single cable, no damage can occur to either of the Sinks.*

Two sources plugged into each other, or an HDMI source being driven by a non-standard DVI-HDMI adapter cable/repeater might cause actual damage to the unprotected design. An external interface protection and isolation device can usually dissipate much more energy than the tiny structures available on a dense ASIC, and may mean the difference between a survivable user error and a merchandise return.

**Source +5VOUT Overcurrent Protection**

Section 4.2.7 of the HDMI Specification defines maximum and minimum bounds for output current from the HDMI Source. Not only is the 500 mA max specification important for compliance, but most HDMI connectors may not be able to handle much more than half an ampere without permanent damage. Again, backdrive current is also a critical issue on this pin, even though it is not specifically outlined other than in Section 4.2.11.

It may be tempting to connect the local +5 V supply rail in the Source directly to this output pin, or through a shunt resistor or other passive device, but great care must be taken to meet the minimum output voltage requirements of the HDMI specification. A semiconductor current limit device using a low Rds(on) pass FET and precision low-ohm current sense resistor can provide an accurate current limit as well as a low, and well defined, series voltage drop.

Passive current limit devices, like PTC polyfuses can have high series resistances with wide variances in drop and limit, complicating +5 V supply tolerance requirements.

Other implementations use a separate discrete linear regulator to generate this output, counting on the thermal shutdown circuit to control *output* current. This may be workable in most cases, but some discrete implementations (regulator+ESD) may allow very high backdrive currents (i.e. when two Sources are connected) that may be outside of the dissipation path in a regulator, and thus unable to control or even specify the actual backdrive current through the connector. Again, while a mis-connected opposing Source *should* be compliant and thus limited from overdriving the local Source output, with all of the possible adapter and other possible cables in circulation, a designer cannot always assume full compliance on the other end of the cable.

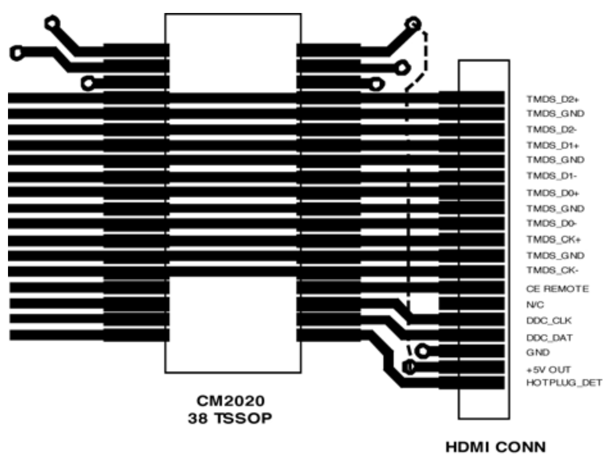
**Summary**

Compliance to the minimum HDMI specification requirements does not ensure a sufficiently durable and reliable consumer electronic design. Meticulous care must be given to the ESD protection of the TMDS interface lines without degrading the signal performance, and without introducing new potential backdrive paths. DDC, CEC, and Hotplug Detect inputs must also provide robust ESD protection, backdrive protection, and especially voltage shifting isolation circuitry that can protect delicate I/O buffers of high performance ASICs. And finally, 5 V output supply circuitry must provide well defined tolerances on low dropout at maximum specified current as well as accurate current limits to protect the current capacity of the connector.

**Integrated Solution**

The CM2020 and CM2021 comprise a complete HDMI port interface protection solution for the Source (CM2020) and Sink (CM2021) sides of the interface. Careful attention to component parasitics and PCB matching for all four TMDS pairs are coupled with enhanced RF return paths for the parasitic elements through packaging and layout tailored specifically for surface mount HDMI connector geometries. The result is a superior self-resonance point with minimized signal distortion on the TMDS pairs, with minimized intra-pair skew.

DDC, CEC, and Hotplug Detect level shifting, isolation and backdrive protection, overcurrent protection and +/-8 kV *contact* ESD protection on all external pins complete the ideal integrated solution for HDMI port protection.




The sample layout shown above demonstrates the ultra-compact nature of the solution in relation to the size of a typical SMT HDMI connector (CM2020 Source side shown here.) The 0.5 mm pitch of the TSSOP-38 package lines up directly with the connector, and provides 10 short ground return paths from TMDS diode clamps to minimize total inductance. This close proximity to the connector also maximizes ESD protection by shunting the harmful pulses before they travel through the PCB.

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