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Solving the Hearing Aid Platform Puzzle

Seven Things Hearing Aid Manufacturers Should Think About

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TECHNICAL NOTE

INTRODUCTION

When it comes to developing a silicon strategy, few applications present a tougher challenge than modern hearing aids. Similar to smartphones and other mobile devices, there is a constant drive to improve performance and battery life, add new features, and retain a compact size or even reduce it.

Unlike other applications, hearing aid integrated circuit designers are faced with a very low supply voltage and a power consumption requirement that is much more stringent. Often the designers must compromise between size, power consumption and performance.

Figure 1. Hearing Aids

SO WHAT IS DRIVING INNOVATION IN THE HEARING AID INDUSTRY?

Market Trends

- The sophistication and complexity of **new algorithm concepts** requires increased computational capabilities and more memory.
- So-called **“invisible” form-factors** placed deep in the ear canal are driving the need for further miniaturization.
- End users want seamless **connectivity** with smartphones and other electronic devices without the need for relay devices or other accessories.
- To remain competitive, manufacturers are introducing new algorithm feature sets more frequently, **shrinking product life cycles** and compressing development cycles.
- Manufacturers are exploring **field upgradeability** of algorithms enabling users to experience different feature sets in the same device during the evaluation phase, and enabling multiple upgrades after the initial purchase.
- **Rechargeable battery technology** continues to evolve as manufacturers strive for simplicity and user convenience.
- Low cost **Personal Sound Amplification Products (PSAPs)** are blurring the line between devices intended to compensate for hearing impairment and those intended for environmental sound amplification, possibly disrupting the market.
- **New business models** including direct-to-consumer may possibly intensify price competition and drive component cost reduction.

Time for a Strategic Rethink

Clearly the current environment is dynamic. This significantly complicates the hardware platform decision and also increases the strategic importance of that decision. What may have worked in the past may no longer be the right approach for the future.

In this technical note we identify and discuss seven key things that hearing aid manufacturers should ponder when thinking about the silicon strategy for their hardware platform:

1. **Overall system challenges:** Are the primary system challenges likely to change?
2. **Digital signal processing architecture:** Which architecture enables a quick response to shifting market needs?
3. **Chip-level integration:** What should be integrated on a single chip? Grouped in a package? Or kept as separate components?
4. **Semiconductor process:** What factors should be considered when moving to a smaller node?
5. **Adopting standard processors in multi-core architectures:** Is it now possible? What are the benefits?
6. **Wireless technology options:** Will Made for iPhone change the game? Will a standard emerge?
7. **System-level integration:** Are there ways to achieve further miniaturization?

Read on for a discussion on each of these areas and the questions they raise. We also provide our view on how to solve the hardware platform puzzle.

While the focus is on air and bone conduction hearing aids, the discussion is also applicable to manufacturers of cochlear implants and middle-ear devices.

1 − OVERALL SYSTEM CHALLENGES

The integrated circuits and associated silicon technology that form the hardware platform are responsible for the customized amplification and manipulation of sound. The chips may also serve user interface and wireless communication functions in more advanced designs.

While some designs only require processor and memory chips, some manufacturers use as many as six, seven or even more chips (such as a wireless controller, wireless radio, power management, analog front end and other sensors) to achieve the functional requirements. They may also require discrete semiconductor components, such as capacitors and electrostatic discharge protection devices, to be included in the overall design. Other key system components include microphones, receivers, antennas and telecoils.

As a complete system, there are three primary challenges for hearing aid designers:

1. Achieve good **performance** in terms of sound quality and computational capability
2. Minimize **power consumption** given a very low supply voltage (as little as ~1.0 V)
3. Minimize physical **size**

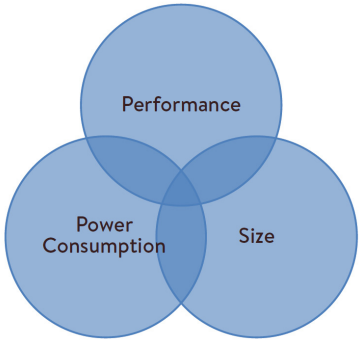


Figure 2. Three Primary Challenges

A decision on one impacts the others, and often compromise is necessary. Balancing these needs is what makes designing hearing aids extremely complex and challenging. It is unlikely that this will change in the foreseeable future.

2 − DIGITAL SIGNAL PROCESSING ARCHITECTURE

Manufacturers have a number of choices when deciding on the digital signal processing architecture for their hardware platform. At the two extremes, these range from a closed approach to a general-purpose open-programmable approach, with some alternative approaches in between. The more “open” an architecture is, the greater the software flexibility a manufacturer has. Naturally, there are tradeoffs depending on the chosen approach.

Closed platform architectures, also known as “fixed-function”, have the signal processing scheme hardwired or hardcoded into the chip. While some parameters can be adjusted, the basic function of the chip cannot be changed without a costly and time-consuming redesign. The dedicated architecture generally results in lower energy requirements, but flexibility is sacrificed.

At the other end of the extreme is the **general-purpose open-programmable** approach. With this architecture signal-processing algorithms can be modified or updated. Since the exact software scheme is unknown, the architecture is designed to accommodate a wide range of signal processing possibilities such as sound, images and sensor data across many applications. The compromise for this flexibility is increased size and power consumption. Given the stringent low voltage and power consumption requirements, general-purpose open-programmable chips are not suitable for hearing aids.

Why MIPS is Mostly Meaningless

Million Instructions Per Second (MIPS) is a measure of processor speed where a higher number implies better performance. Many factors influence the metric, including the type of instructions being executed, the order of instructions, the system’s clock frequency and method of execution. A million instructions in one architecture may accomplish significantly more than the same number of instructions in a different architecture.

Since different architectures are used across the hearing aid industry and a standard benchmark test does not exist, a meaningful comparison cannot be made. MIPS can, however, be useful for comparing the relative performance of processors from the same manufacturer when the processors support the exact same instruction set.

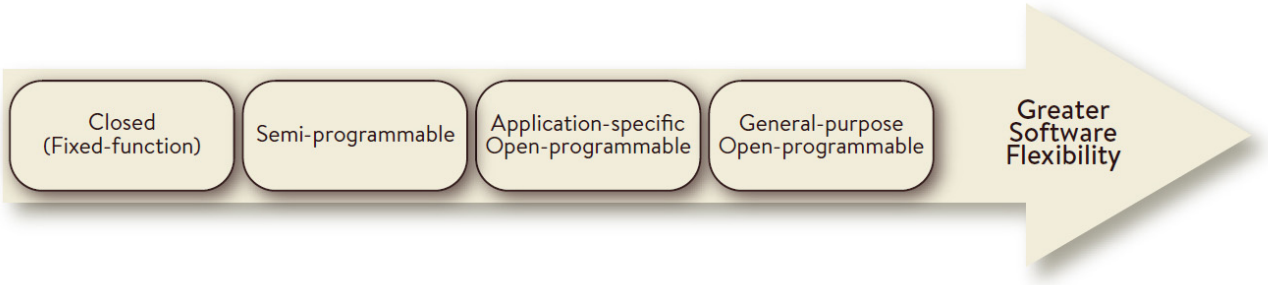


Figure 3. Digital Signal Processing Architecture

Between the two extremes is a **semi-programmable** architecture that attempts to overcome the disadvantage of closed platforms by enabling some programmability. Major signal processing capabilities are hardwired in logic blocks, while a programmable digital signal processor (DSP) is also included in the architecture. This enables additional signal processing capabilities to be implemented in software without the need to design a new chip. However, if significant changes are required to the hardwired blocks, or a completely new algorithm concept cannot be addressed by the programmable processor, then a new chip is required. While some flexibility is gained, the semi-programmable approach still sacrifices power efficiency.

Another approach is an **application-specific open-programmable** architecture. It is designed and optimized for the signal processing needs of a very specific application while offering the software flexibility of a general-purpose architecture. Though not as power efficient as closed architectures, most of the power efficiency disadvantage can be eliminated through efficient chip design and choice of process node, as we will explore later in this white paper.

Table 1. COMPARISON OF DIGITAL SIGNAL PROCESSING ARCHITECTURES

	Closed (Fixed-function)	Semi-programmable	Application-specific Open-programmable	General Purpose Open-programmable
Description	Signal processing hardwired or fixed in logic blocks	Major signal processing is hardwired or fixed in logic blocks Some signal processing defined by a programmable DSP	Degree of openness is optimized specifically for hearing aids All signal processing defined by programs running on a programmable DSP	Fully programmable and intended for a broad range of applications
Degree of Flexibility to Change Signal Processing	Least flexible Some parameters can be adjusted, but not basic functionality	Semi-flexible Can solve some signal processing issues or changes on programmable DSP	Extremely flexible within realm of specific application New algorithms or modifications implemented in software	Most flexible New algorithms or modifications implemented in software
Power Efficiency	Most power efficient since exact processing requirements are known	Moderate power efficiency	Not as optimized as semi-programmable or closed architectures Most of the power efficiency disadvantage can be eliminated through design and choice of process node	Relatively power hungry given need to accommodate a wide range of signal processing possibilities across many applications
Summary	Chip re-spin required for modifications	Some flexibility, but chip re-spin required if hardwired signal processing blocks need modification or changes cannot be addressed with programmable DSP	Maximizes flexibility as completely new concepts can be implemented without a chip re-spin Compromise in power efficiency can be mitigated	Not suitable for hearing aid applications: exceeds power budget

Software Flexibility Enables Innovation

The advantages of software flexibility and the ability to leverage hardware investment across many products and brands greatly outweigh the advantages of a closed architecture. This is particularly true given the shorter product-life cycles, tiered performance/price points, and micro-segmentation that is now required to offer a broad and quickly refreshed product portfolio.

The software flexibility provided by open-programmable architectures designed specifically for hearing aids enables algorithm innovation to flourish. Entirely new concepts can be implemented on the same hardware platform, unrestrained by the hardwired limitations of semi-programmable or closed platforms.

This added flexibility opens up new possibilities including in-the-field upgrades of algorithm feature sets and even the opportunity of users downloading enhancements, much like apps available for a smartphone or tablet.

These possibilities, and those yet to be imagined, underscore the value of flexibility. Manufacturers that adopt this approach are able to respond quickly to shifting market needs and changes in the competitive environment without having to spin new silicon. This clearly provides a competitive advantage.

3 − CHIP-LEVEL INTEGRATION

With the digital signal processing architecture approach decided, the next decision revolves around how to partition the circuitry. This involves careful consideration of which functional blocks and components should be combined and integrated on a single chip, grouped and encased in a package or kept as separate components.

Main Functional Blocks

Analog Front End (AFE) – After sound has been converted to an electrical signal by the microphones, the AFE is responsible for conditioning and converting the signal from analog to digital so that it can be analyzed and manipulated by the processor.

Processor – The “brain” of the hearing aid performs the signal processing and controls the various tasks within the overall hearing aid system. Given the computational-intensive needs of hearing aids, a specialized microprocessor called a DSP is used along with additional computational units in multi-core architectures.

Output stage – Pulse width modulation (PWM) technology is used as a digital amplifier technique to provide normal or high audio output to a receiver.

Memory – Volatile memory such as Random-Access Memory (RAM), typically integrated on the same chip as the processor, does not store its contents when the system is powered down. Non-volatile memory in the form of Electrically Erasable Programmable Read-Only Memory (EEPROM), retains its contents when powered down. It can be programmed multiple times and is where the algorithms, fitting parameters and data logs are stored.

Power management – Optimizes and conserves the use of power provided by the battery.

User interface – Interface blocks enable input from a volume control, push buttons or sensors allowing the user to control the device, such as increase volume and change programs.

Wireless communication – Enables communication between the hearing aid and external devices used to control the hearing aid, or send data between hearing aids or other devices.

In addition to these functional blocks, there are other components such as capacitors and electrostatic discharge (ESD) protection circuits that are typically included in a hearing aid system.

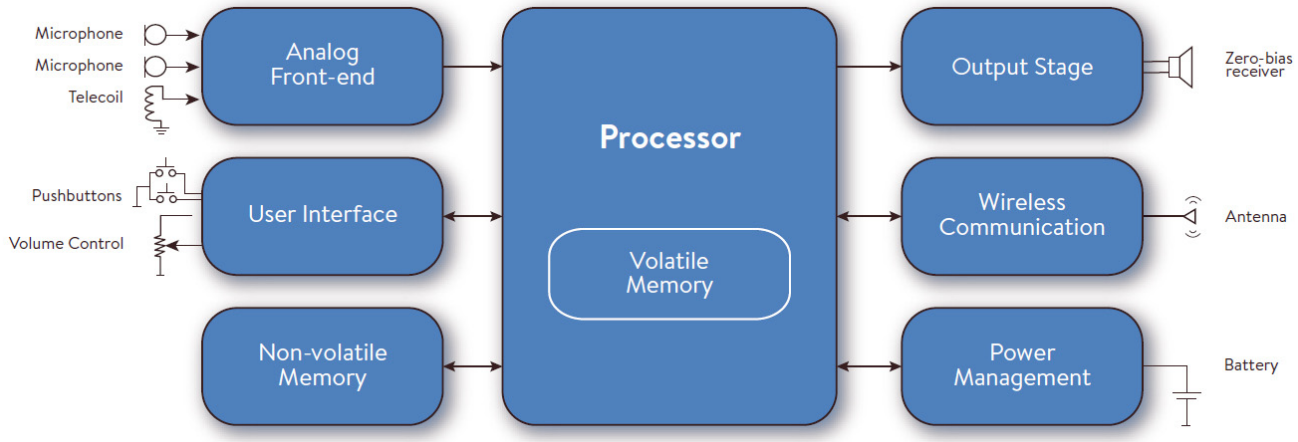


Figure 4. Main Functional Blocks Diagram

Design Partitioning Factors

Flexibility is a key factor when making design partitioning decisions. If blocks are integrated on a single die as a system-on-a-chip (SoC), the ability to change a single functional block is lost and the entire chip must be revised. This can potentially be both time consuming and costly. For example, if the wireless communication functionality is combined with the processor into an SoC, the system is locked into a specific wireless technology.

So why not just keep all of the key functional blocks as separate chips to maximize flexibility? Quite simply, size. There is a limited amount of available area within a hearing aid, and given the trend towards “invisible” devices, the available area is getting smaller and smaller. This is further complicated as new requirements are added, such as communication with multiple wireless technologies and the adoption of rechargeable battery technology. Designers are then challenged to find ways to shrink the electronics and route the signals and power supplies between the different chips.

A logical approach is to integrate as many blocks as possible. While there are many advantages to integrating functionality as summarized in Table 2, there are also risks and business factors that need to be considered carefully. Designers also need to keep in mind the stringent size, power consumption and performance requirements of hearing aids.

Table 2. FACTORS TO THINK ABOUT WHEN MAKING A DESIGN PARTITIONING DECISION

System Requirements	Integration Advantages	Integration Risks	Business Considerations
Good sound quality and computational performance Minimize power consumption Minimize physical size	Less power consumption Greater efficiency Increased signal integrity Smaller footprint Simplified manufacturing (fewer components)	Increased design complexity Higher chip manufacturing complexity may impact yield Loss of flexibility in changing functional blocks	Increased design costs versus manufacturing cost savings Time to market

With the increasing complexity of hearing aids and demand for smaller devices, a greater need exists to create a more integrated platform. In the past, hearing aid manufacturers were reluctant to integrate the highly noise-sensitive AFE circuitry with the digital circuitry that is comparatively “noisy”. This was a concern when migrating to smaller silicon manufacturing processes. However, through clever chip design and selection of the appropriate semiconductor manufacturing process, this challenge can be overcome. This unlocks the potential for smaller hearing aid designs or further integration of additional functionality.

A Complex Decision

There is no simple answer to design partitioning and chip-level integration. The key is to find the optimal balance between all of the factors. Some blocks are relatively mature in their functionality and are prime candidates for integration. Others, such as wireless communication, may change depending on which technology or technologies are adopted. When this is the case, keeping the block on a separate chip is desirable, making it easier to modify the overall system if required.

4 − SEMICONDUCTOR PROCESS

Another important factor to consider when solving the hardware platform puzzle is the semiconductor process that will be used to create the integrated circuits. This decision is both influenced by the design partitioning approach discussed previously, as well as design challenges of certain functional blocks in smaller process nodes.

The desire for smaller, faster, cheaper and more reliable integrated circuits with lower power consumption drives the development of new semiconductor tools and technologies. Primarily the market demands of mobile devices and high-volume consumer electronic applications have motivated semiconductor manufacturers to seek new ways to shrink transistors the basic building blocks of an integrated circuit.

Transition to Smaller Nodes

In the case of hearing aid platforms, the increasing sophistication of signal processing algorithms is driving the need for greater computing capability. Transitioning to a smaller process geometry also helps address the stringent power consumption and size constraints.

However, there are several catches.

First, **design and manufacturing complexity** increases significantly with smaller process nodes. There are layout-dependant implications and strict design rules that must be adhered to and the number of rules increases as the nodes get smaller.

Although shrinking digital circuitry is relatively straight forward, redesigning AFE circuitry for a smaller process node is much more challenging given the sensitivity to noise.

The second catch is **cost**. The full cost for design, verification, layout, mask sets, and design tools must be factored in. As shown in Figure 5, these costs significantly rise, making the smallest nodes feasible only for extremely high-volume chips. While chips designed for the 90 nm node may have cost approximately $10 million to develop, the overall cost more than doubles for 45/40 nm designs and approaches $40 million at the 28 nm node.

Moore’s Law

Gordon Moore, co-founder of Intel, predicted in what became known as “Moore’s Law” that the number of transistors that can be placed on an integrated circuit doubles approximately every two years. The trend has largely held true, made possible by a continuing migration to lower process nodes, for example, from 90 nm to 65 nm to 40 nm and so on.

The smaller the numerical value of the process name, the shorter the distance between the transistors within an integrated circuit. Shorter distances enable faster switching and require less energy, which leads to higher performance, greater complexity and smaller die size when compared to larger nodes.

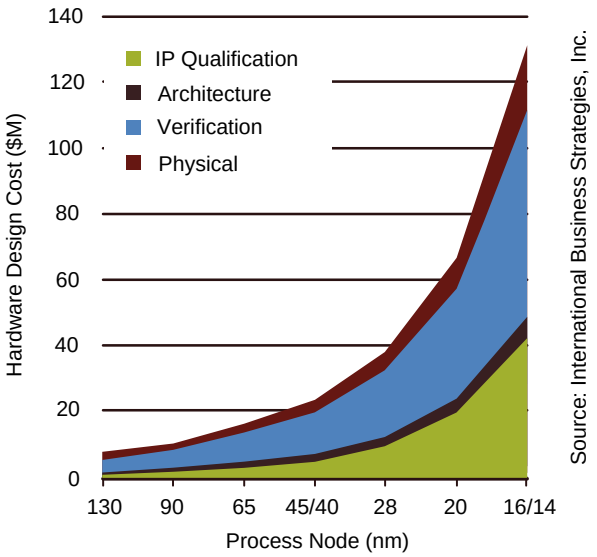


Figure 5. Development Costs Increase Significantly for Smaller Process Nodes

Naturally, a design team that is new to a process node requires more time to design the chip and is more likely to require more design cycles or spins to perfect the chip, adding to development time and cost.

Determine the Process "Sweet Spot"

So what is the semiconductor process "sweet spot" for hearing aid platforms? That can only be decided after weighing all of the benefits and implications as summarized in Table 3. The partitioning of key functionality must be considered, and as always, the overall system requirements for performance, power consumption and size.

Currently, some manufacturers design chips for the 65 nm process, but few integrate the analog front-end with the processor at this process node. With increasing algorithm complexity demanding greater computational capabilities, and the addition of new functionality putting added pressure on power consumption and miniaturization, further migration to smaller geometries is likely. However, the economics will become significantly more challenging for smaller-volume manufacturers designing their own chips.

Table 3. FACTORS TO THINK ABOUT WHEN MOVING TO A SMALLER SEMICONDUCTOR PROCESS NODE

Pros	Cons
Higher Performance	Design complexity (more design rules, layout-dependant implications, greater schedule unpredictability)
Lower Power Consumption	Costs (design time, verification & layout, mask sets, design tools)
Miniaturization	

5 − ADOPTING STANDARD PROCESSORS IN MULTI-CORE ARCHITECTURES

Many of today's hearing aid platforms are based on multi-core architectures. This is not just a trend in hearing aids, but for numerous embedded systems that are challenged to increase performance and reduce power.

With multiple cores, different computational units including DSPs, general-purpose processors and hardware accelerators, often referred to as coprocessors, carry out multiple instructions at the same time, increasing overall speed. This becomes necessary when a single type of processor is less efficient at managing a wide variety of diverse tasks. When combined in a single chip, higher performance at lower power consumption can be achieved.

There are two primary drivers for the adoption of multi-core architectures in hearing aids:

1. Need for increased **computational performance** to support more advanced algorithms based on new audiological concepts from evidence-based research; and
2. Introduction of **wireless functionality** for data transfer between hearing devices, remote control, and connectivity with other electronic devices.

A widely-held misconception is that standard processing cores are not suitable for use in hearing aids. This is primarily due to the stringent power dissipation requirements. This has led to proprietary or custom-designed cores being used almost exclusively.

While it is true that proprietary cores will have size and power efficiency advantages, those advantages are becoming smaller with deeper sub-micron technologies. Standard cores offering programmable flexibility have evolved to where they can be used in conjunction with specialized cores for certain processing tasks, such as running proprietary wireless baseband functionality to optimize power consumption.

As summarized in Table 4, the adoption of standard cores not only reduces overall design time-an advantage with ever-shortening development schedules-but also reduces the technical risk. With the adoption of a standard core, design resources can be redirected to other areas that deliver the most value.

Just as other applications with stringent power constraints have adopted standard cores as part of their multi-core architecture, hearing aid platforms, logically, will likely follow the same adoption path given the significant advantages. The ARM® Cortex™−M3 processor is one example of a standard core now being used in the industry.

Table 4. ADVANTAGES OF USING A STANDARD CORE

Programmable flexibility for customization
Reduced development time
Reduced technical risk: design is verified
Available ecosystem of third-party tools and technical support
Existing technical documentation
Design reuse: portability to subsequent platforms

6 − WIRELESS TECHNOLOGY OPTIONS

Analog wireless technologies in the form of telecoil or FM systems have been used in hearing aids for many years. More recently, near-field magnetic induction (NFMI) and radio frequency (RF) technologies have been introduced. Table 5 summarizes the main advantages and disadvantages of these two technologies.

NFMI is limited to a range of less than 1 meter (3 feet). Therefore hearing aids using this technology must also use an intermediary relay device to wirelessly communicate across greater distances. Typically, Bluetooth® technology is used for the communication link between relay device and a Bluetooth-compatible audio source. This was the design approach first adopted by manufacturers.

Subsequently, RF technology was introduced with ranges of approximately 7 to 9 meters (23 to 30 feet). This eliminates the need for relay devices to be worn around the

user's neck or kept in close proximity. While range is extended, unless the sound source is capable of transmitting the same frequency, an adapter must be connected to the source to convert the signal to the appropriate frequency.

Table 5. COMPARISON OF WIRELESS TECHNOLOGIES

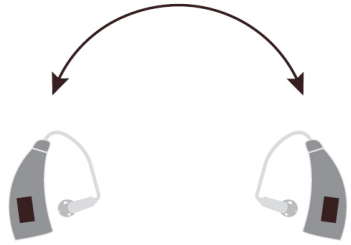
	NFMI	RF
Advantages	Lower power consumption Signal easily propagates through and around the human head and body enabling ear-to-ear communication	Long range of approximately 7−9 meters (23−30 feet) Relay device not required for far-field wireless communication Low transmission delay from far-field sound sources
Disadvantages	Limited transmission range of approximately 60−90 cm (2−3 feet) Requires a relay device for far−field wireless communication Transmission delay when receiving sound from far-field sources via a relay device	Higher power consumption 2.4 GHz signal does not propagate well around the human head and body Sub 1 GHz require larger antennas Only a few frequency bands are available for world-wide license-free use

Unfortunately, neither technology is ideal for every use case.

Table 6 summarizes existing and potential use cases for wireless technology. While not all inclusive, the list captures a range of possibilities. The use cases have been grouped into two categories: wireless communication between hearing aids, and wireless communication between the hearing aids and other electronic devices.

Each of the use cases presents their own set of unique challenges such as range, data rate, sound quality, delay or latency and the ever present nemesis-power consumption.

Table 6. WIRELESS USE-CASES

Between Hearing Aids	Between Hearing Aids and Other Devices
	
Transfer of data from one hearing aid device to another to coordinate parameters such as program mode and volume Transfer of data back and forth between hearing aids to collaborate on signal processing Streaming of audio captured by one device to another in cases where the user has unilateral hearing loss (CROS/BiCROS) Streaming of telecoil signal from one device to another when using a telephone	Remote control device to operate hearing aid (e.g. change programs and adjust volume) Streaming of audio from a remote microphone Streaming of audio from electronic devices such as smartphones, televisions, stereos, personal music players and computers Streaming of audio bilaterally between a phone or similar device Wireless data transmission during fitting session (configuration and program data sent to hearing aid) Streaming of audio during a fitting session (to enable user to assess different sound scenarios) Distributed processing: transfer of audio to an external device for additional processing; processed data sent back

"Made for iPhone" Changes the Game

Up to this point, hearing aid manufacturers have produced wireless accessories such as relay devices, remote microphones, and other intermediary devices to enable wireless connectivity. In 2012, hearing aid manufacturers began announcing "Made for iPhone" hearing aids that utilize 2.4 GHz radio technology built into iPhones. Through the use of apps developed by manufacturers, compatible hearing aids can be controlled and adjusted by the user. They may also receive streaming audio, and the smartphone's microphones can also be used for directionality when the smartphone is used as a remote microphone.

This is an exciting development for users. It eliminates the need for multiple accessories, provides greater customization, and opens up new possibilities in how they interact with their hearing aids. While Apple is the first smartphone manufacturer to integrate this enhanced hearing aid interoperability, it is likely that other smartphone manufacturers will follow suit. Not to be placed into a competitive disadvantage, hearing aid manufacturers need to consider how best to address this trend.

Will a Wireless Standard Emerge?

Manufacturers have adopted a variety of digital wireless technologies. Some have adopted NFMI at various frequencies while others have adopted proprietary RF technology in the 900 MHz and 2.4 GHz spectrums. So far, the industry has not converged on a single wireless standard.

Clearly there are benefits and trade-offs with the existing technologies. Whether the “Made for iPhone” trend leads to a single standard adopted by the industry remains to be seen. In the meantime, a logical question is, can multiple technologies be used in the same set of hearing aids?

One possible approach is a dual-radio solution. This is a significant challenge given the additional silicon content and need for multiple antennas especially when faced with the ever-present power and size constraints. But through clever engineering and advanced chip packaging techniques, it is possible.

Yet another possibility is the adoption of ultra-low-power wireless technology that may overcome existing shortcomings. If the technology reliably delivers high data rates, ear-to-ear and long-range direct audio streaming, all with low power consumption, it may become broadly adopted across the industry.

Why Wireless Flexibility is Key

So what does this all mean for a hardware platform today? Things are changing quickly and the technology is still evolving. Given the uncertainty, it makes sense to build in as much flexibility as possible for interfacing with and controlling different technologies, and even multiple wireless technologies. By doing so, manufacturers can easily implement new technology as it emerges or offer multiple wireless solutions optimized for different use cases.

7 − SYSTEM-LEVEL INTEGRATION

Integrated circuits are only one piece of the puzzle in hearing aid design. Electro-acoustics and mechanical design also play an important part.

Electro-acoustics

Hearing aid transducer components-microphones and receivers-face the same miniaturization challenges as integrated circuits. They must deliver the highest reliability and electro-acoustic performance as they scale down in size. Electro-acoustic system designers need to ensure the optimal selection of transducers and their placement within the casing to minimize sound leakage and vibrations that may compromise sound quality.

Mechanical Design

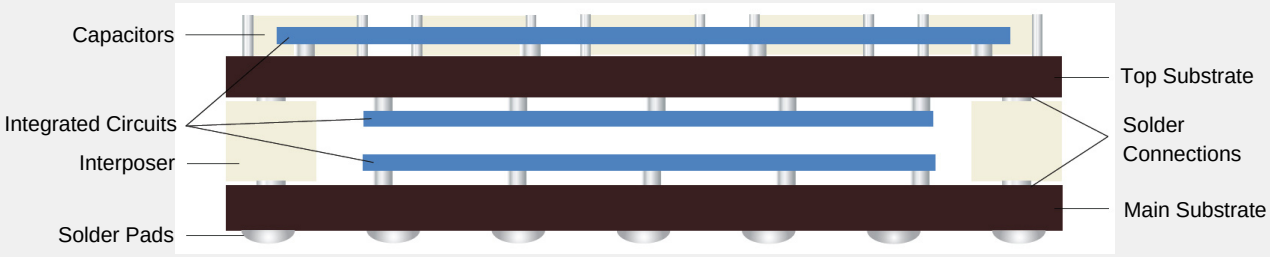
Meanwhile, the mechanical design team is challenged with taking all of the components-transducers, telecoil, battery, buttons and PCBs-and using their specialized knowledge of mechanics, electronic engineering and materials to figure out the optimal placement within the casing or shell. They are constantly challenged to push technological boundaries to create smaller form factors, yet maintain manufacturability and robustness.

Advanced Packaging Enables Further Miniaturization

One recent development in advanced packaging techniques is chip stacking. By utilizing 2.5D and 3D approaches for connecting integrated circuit die and passive components in the same package, significant space savings can be achieved.

Advances in die thinning combined with integrated passive device (IPD) technologies also help to reduce size. Vertical connection techniques such as through-silicon vias (TSVs) also promise even further degrees of miniaturization in multi-chip stacked architectures.

Within these ultra-small packages, signal distances are decreased and passive devices can be strategically placed within the stacked architecture, improving electrical performance. This is particularly of interest to hearing aid manufacturers seeking additional miniaturization and power reduction techniques.



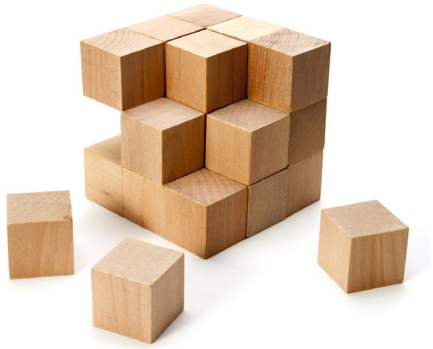
Putting the Pieces Together

It is clear that the hearing aid hardware platform cannot be designed without considering the entire hearing aid system. Electro-acoustic and mechanical design factors must be contemplated to ensure that the overall functionality, performance, power consumption and size objectives are met. Design teams must also be well versed in existing and emerging methods for packaging electronic components.

To create the optimal product, the hardware platform should:

- Be designed with system flexibility in mind;
- Integrate with a broad array of existing and emerging transducers; and
- Be compatible with advanced packaging technologies to further reduce size and power consumption.

A comprehensive systems level design approach allows for innovative mechanical design while ensuring compatibility with manufacturing and assembly processes. This is critical in order to keep pace with the latest innovations and to ensure an efficient design flow.



8 − A PIECE OF THE PUZZLE SOLVED

Developing a hardware platform strategy is a challenge. Much like solving a puzzle, it requires imagination, analytical thinking, patience and persistence.

We have identified seven things that we think hearing aid and hearing implant device manufacturers should think about to solve the hardware platform puzzle.

ON Semiconductor has solved a piece of that puzzle with the wireless-ready Ezairo 7100 DSP-based system, meeting the stringent requirements and advanced performance needs of hearing aids and hearing implant devices. When combined with non-volatile memory and wireless radios, it forms a complete hardware platform.

The hearing aid market is dynamic and the technology is ever evolving. Given the emerging trends and level of uncertainty, flexibility is a must.

As an integrated system, Ezairo 7100 provides built-in flexibility to support evolving algorithm, wireless and system-level needs. It includes an analog front-end, multi-core processing, wireless control and power management functionality, all on a single chip.

The new series builds on the company's successful open-programmable DSP-based systems, including the Ezairo 5900 and Ezairo 6200 series. Ezairo 7100 systems are available as die or as packaged integrated circuits.

Table 7. SOLVING THE HARDWARE PLATFORM PUZZLE

Seven Things to Think About		Ezairo 7100 Solves a Piece of the Puzzle
1	Overall System Challenges	Delivers on performance, size and power consumption: the industry's most integrated, most power efficient (< 500 μW) chip with 5X the performance of the previous generation
2	Digital Signal Processing Architecture	Open architecture specifically designed for hearing aid and hearing implant devices to maximize programmable flexibility for evolving algorithm features
3	Chip-level Integration	AFE, processing, wireless control and power management integrated on a single chip
4	Semiconductor Process	Manufactured in 65 nm process to produce the industry's smallest and most power efficient integrated chip
5	Adopting Standard Processors in Multi-core Architectures	Utilizing ARM® Cortex™ −M3 processor−an industry first
6	Wireless Technology Options	Built-in wireless flexibility to control different kinds and even multiple wireless radios
7	System-level Integration	Built-in flexibility to interface with a wide range of transducers and other components that may be included in the overall system, or may be adopted in the future

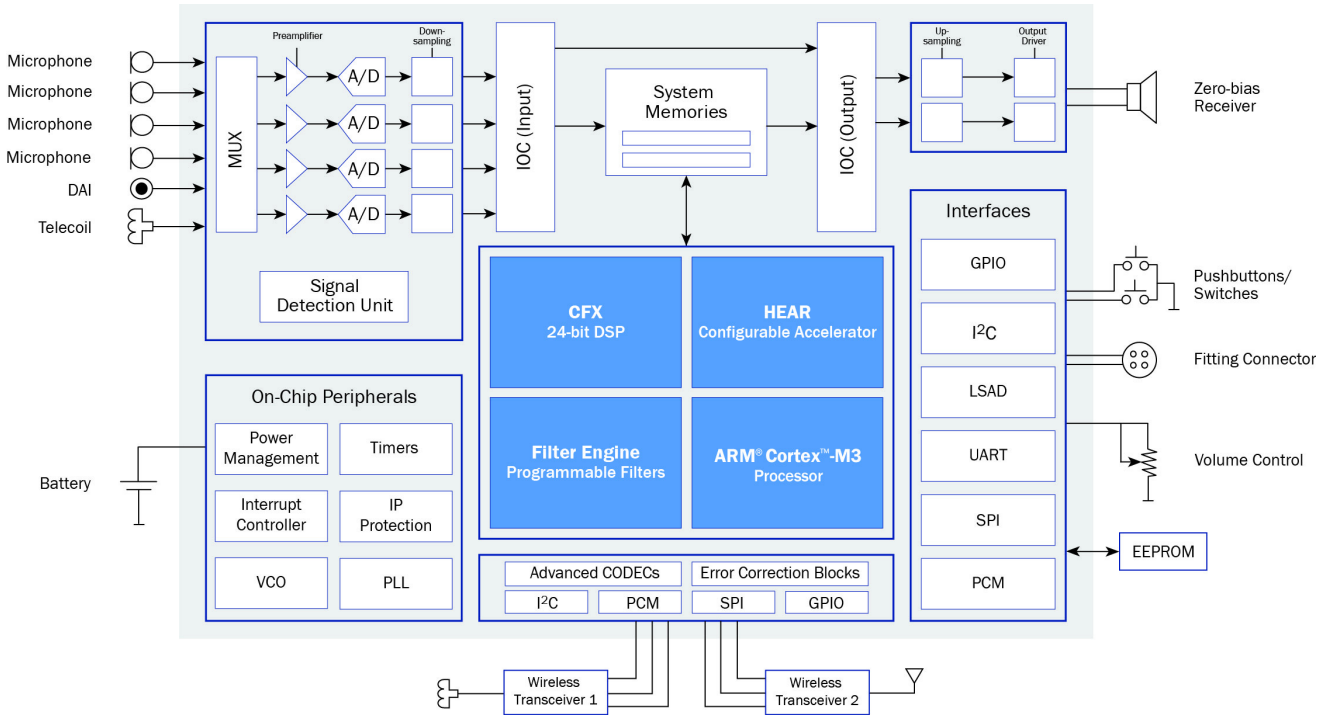


Figure 6. Ezairo 7100 Arch Diagram

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