ON Semiconductor®

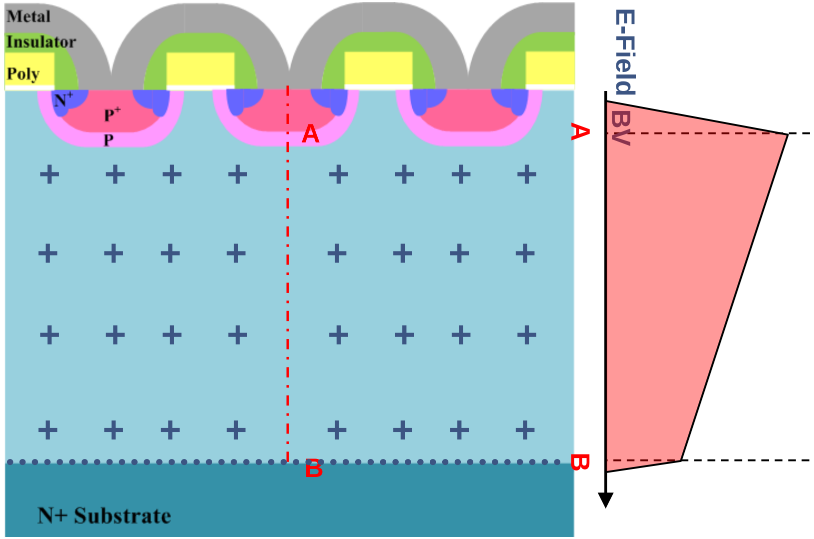
Drive and Layout Requirements for Fast Switching High Voltage MOSFETs

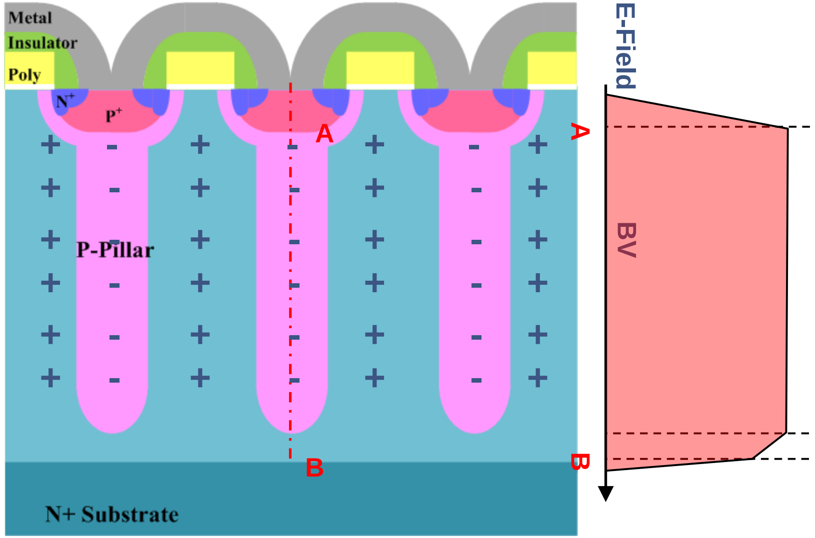
Contents

E-Field Distribution of SJ Technology

SJ Technology Allows Twice BV for Same Doping

- Planar MOSFET
- Super-Junction MOSFET





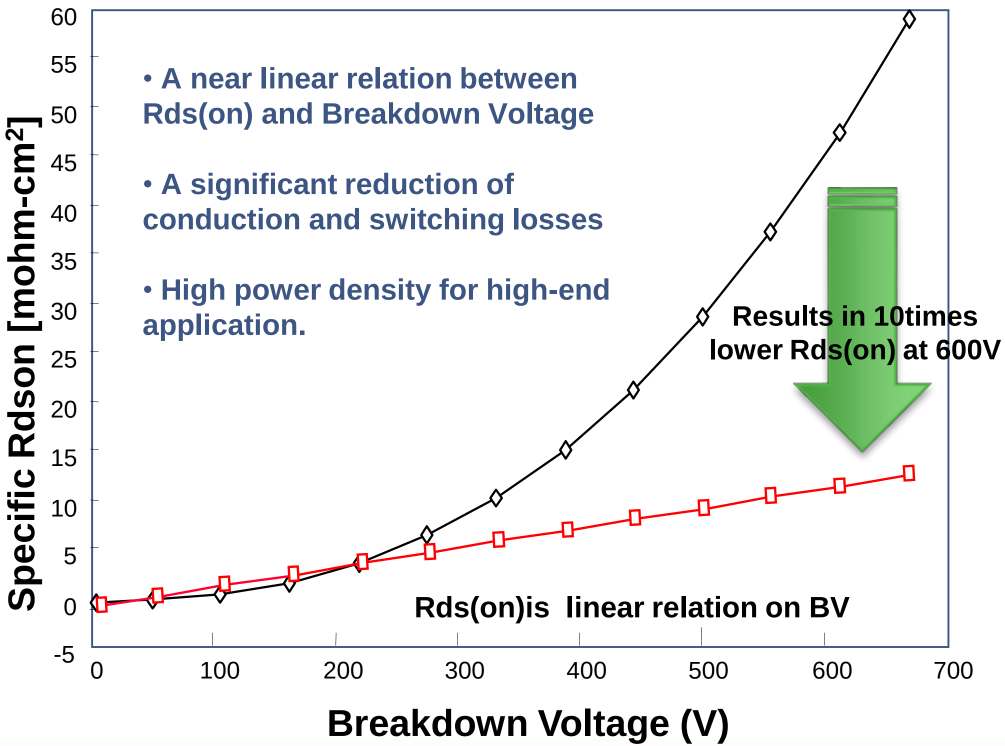
Area is proportional to BV

Area is twice so BV is twice for same doping thanks to charge balance

- Si limitation : On resistance and BV is trade-off
- On resistance is in linear relation on BV

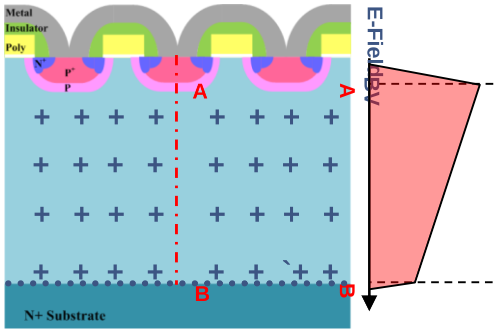
Silicon Limit of HV MOSFETs ?

$$Ron, sp = 6\times10^{-9} BV^{2.5}$$



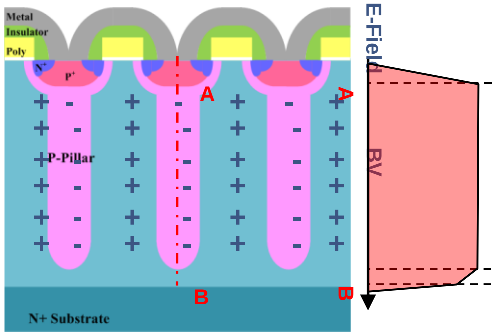
- A near linear relation between Rds(on) and Breakdown Voltage
- A significant reduction of conduction and switching losses
- High power density for high-end application.

- Planar MOSFET



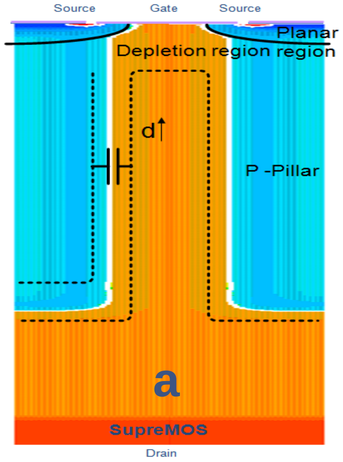
Area is proportional to BV

- Super-Junction MOSFET

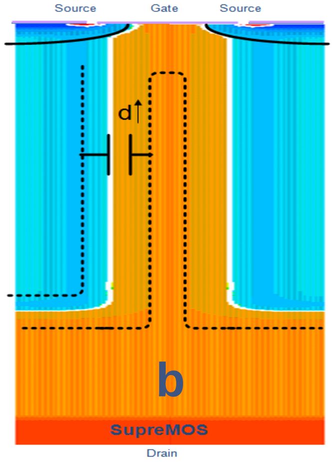


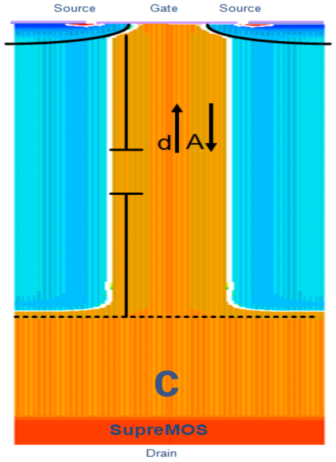
Area is twice so BV is twice for same doping thanks to charge balance

Non-linear Coss in SJ MOSFET

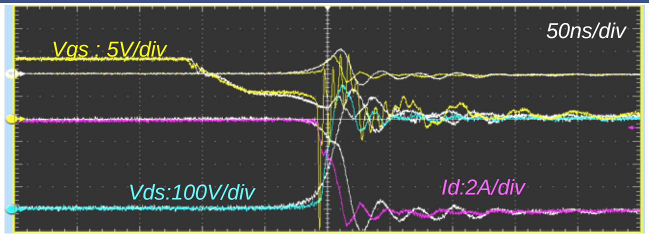


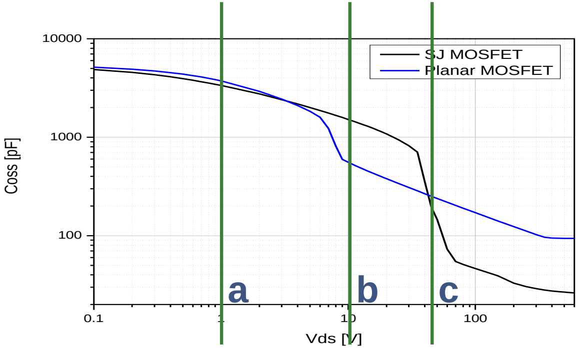
$$C = \frac{\varepsilon_o \cdot \varepsilon_r \cdot A}{d}$$





- Coss curve of super-junction MOSFET is highly non-linear
  → Extremely fast dv/dt and di/dt and voltage and current oscillation





SJ MOSFET @ Ron=120Ω, Roff=30Ω vs Planar MOFET @ Ron=22Ω, Roff=10Ω(Ref.)

SuperFET3 vs SuperFET2

DUTs	SuperFET 3	SuperFET 2
	FCH040N65S3	FCH041N60E
BV_{DSS} @ T_J=25℃	650 V	600 V
I_D@ T_C=25℃	68.0A	77.0 A
$R_{DS(ON)}$ max. I_D=34A	40mΩ	41mΩ
$V_{GS(th)}$	2.5V ~ 4.5V	2.5V ~ 3.5V
V_{GSS} @ DC	±30V	±20V
*Q_g @ V_{dd}=400V, I_D=34A, V_{gs}=10V	* 158 nC	* 330 nC
*R_g @ f = 1 MHz	* 0.7 Ω	1.2 Ω
*E_{OSS} @ 400V_{DS}	* 13.7 uJ	* 25.7 uJ
*Q_{OSS} @ 400V_{DS}	* 521 nC	* 596 nC
Peak diode recovery dv/dt	20V/ns	20V/ns
MOSFET dv/dt	100V/ns	100V/ns

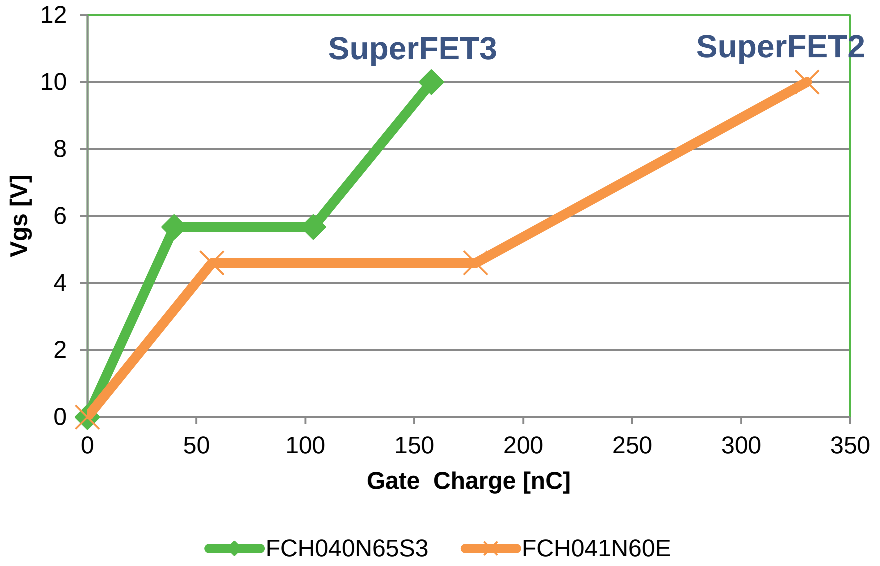
-52%

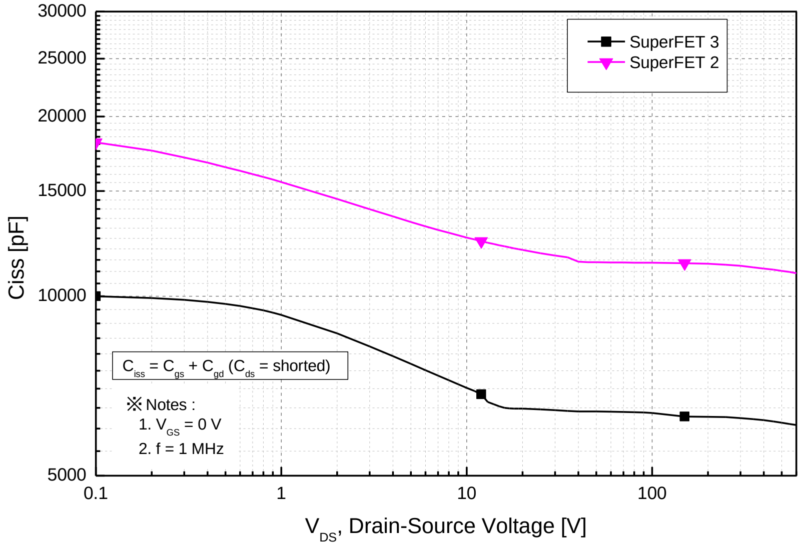
-47%

-13%

Gate Charge Characteristic

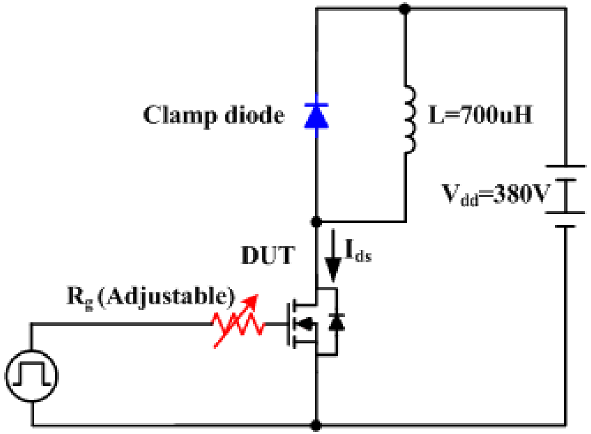
SuperFET3 - Low Gate Charge and Input Capacitance

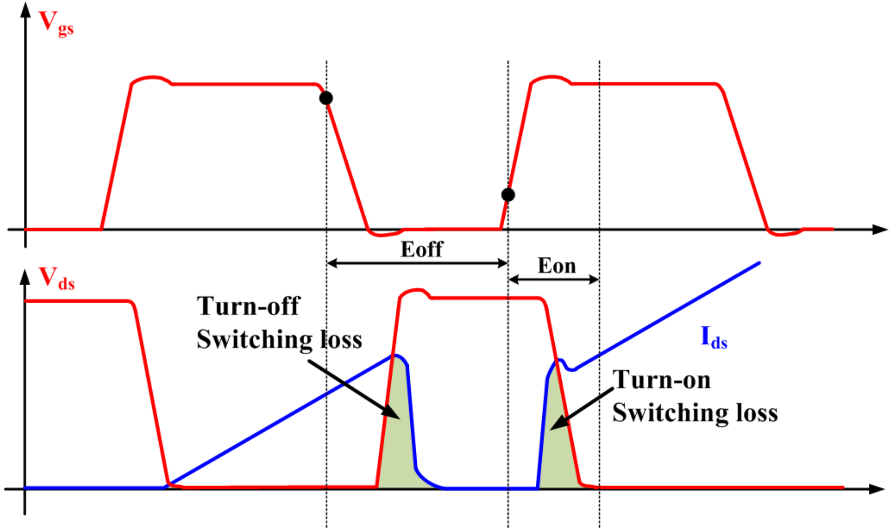




DUTs	FCH040N65S3	FCH041N60E
Q_{gs}	39.8	57.1
Q_{gd}	63.8	121.0
Q_g	157.9	330.2

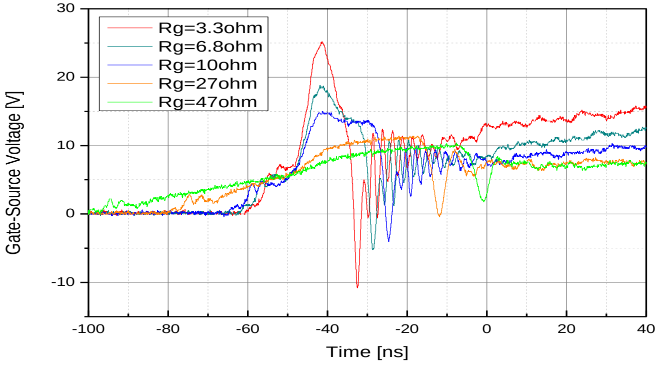
Clamped Inductive Switching Circuit & Waveforms and Loss Definition

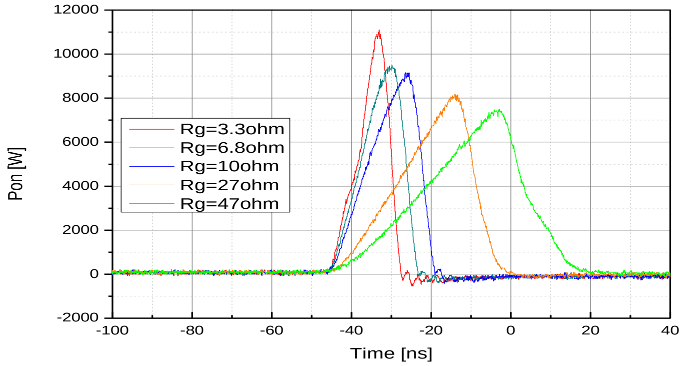


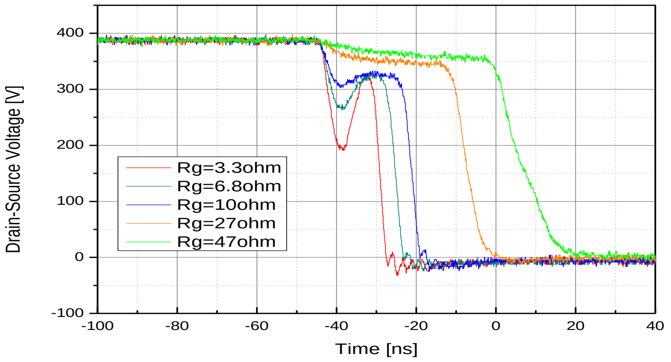


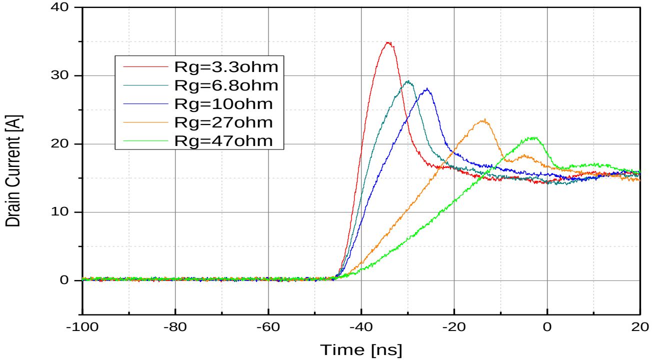
- Test Circuit which is used for the following measurements.

Effects of Gate Resistance at Turn On Transient

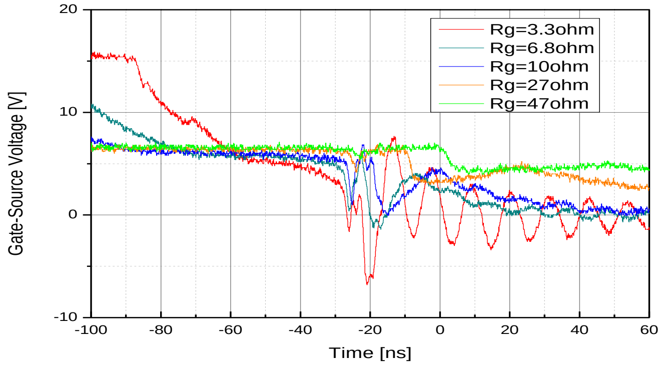


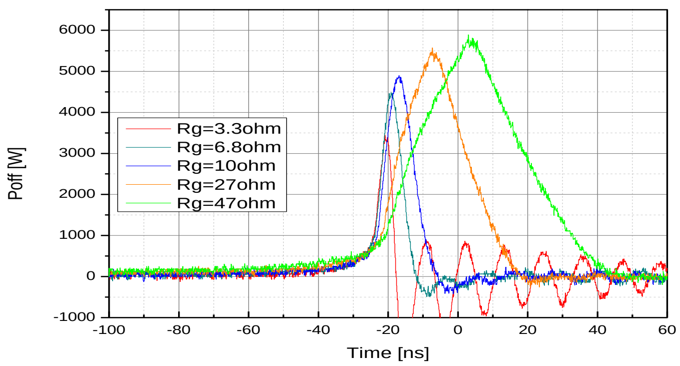


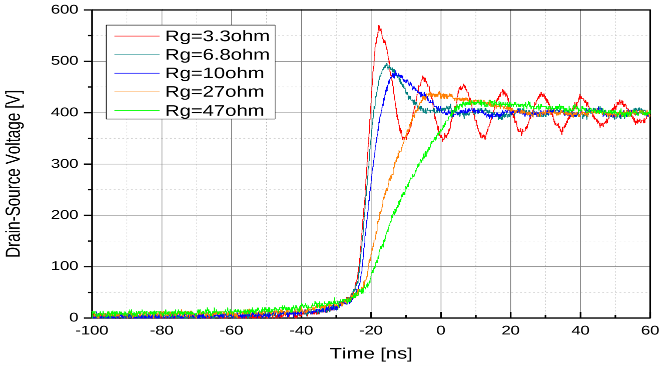


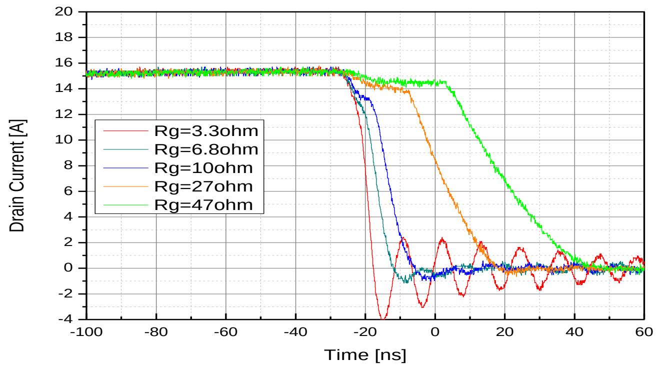


Effects of Gate Resistance at Turn Off Transient

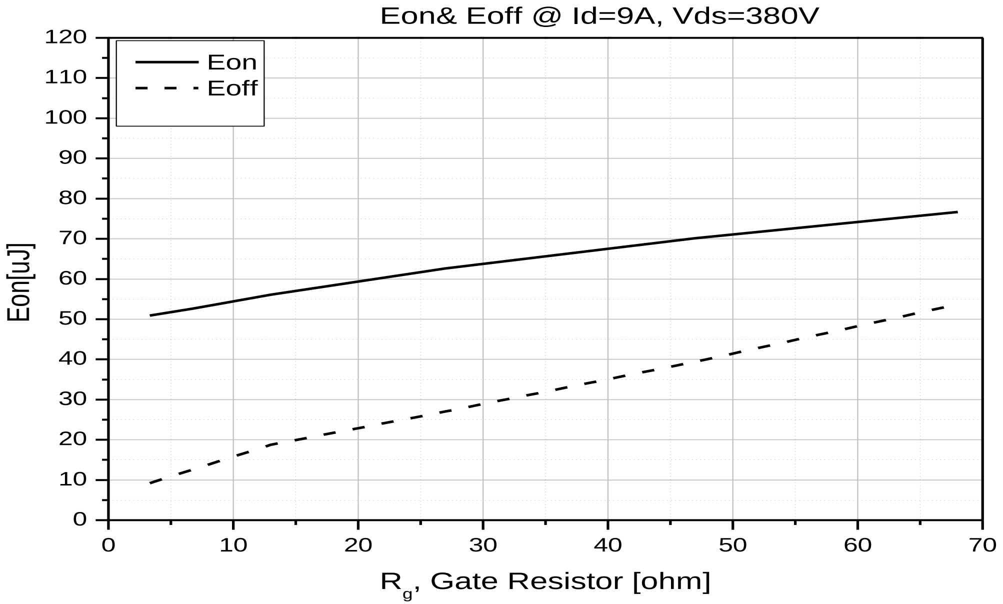








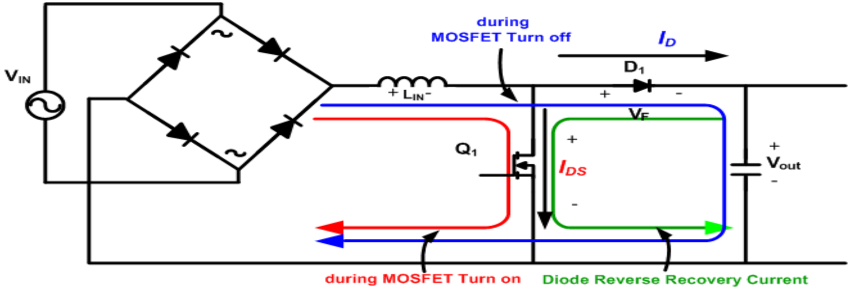
Effects of Gate Resistance

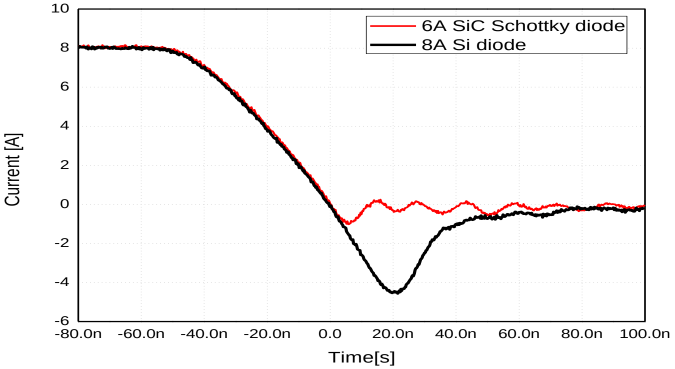


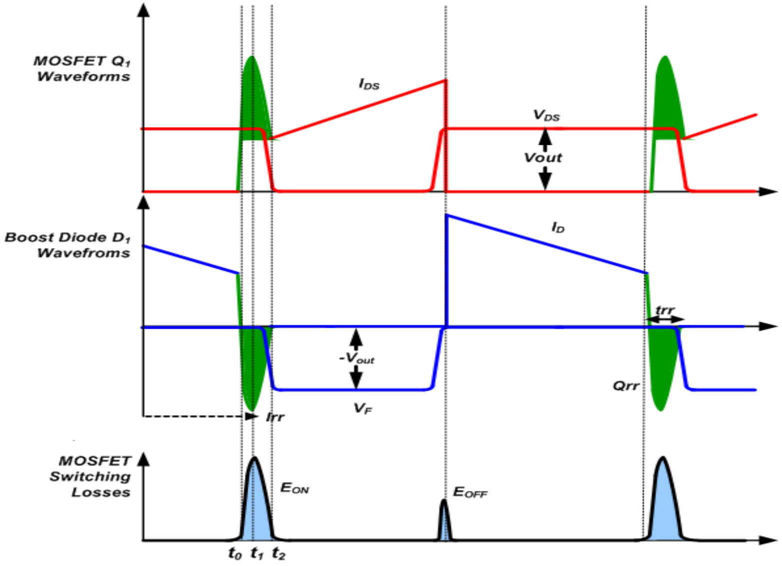
- Critical control parameter in gate-drive design is external series gate resistor (Rg).
- From an application standpoint, selecting the optimized Rg is very important.

  - Efficiency vs dv/dt or voltage spikes.

Reverse Recovery Effect
Si Diode vs SiC Schottky Diode

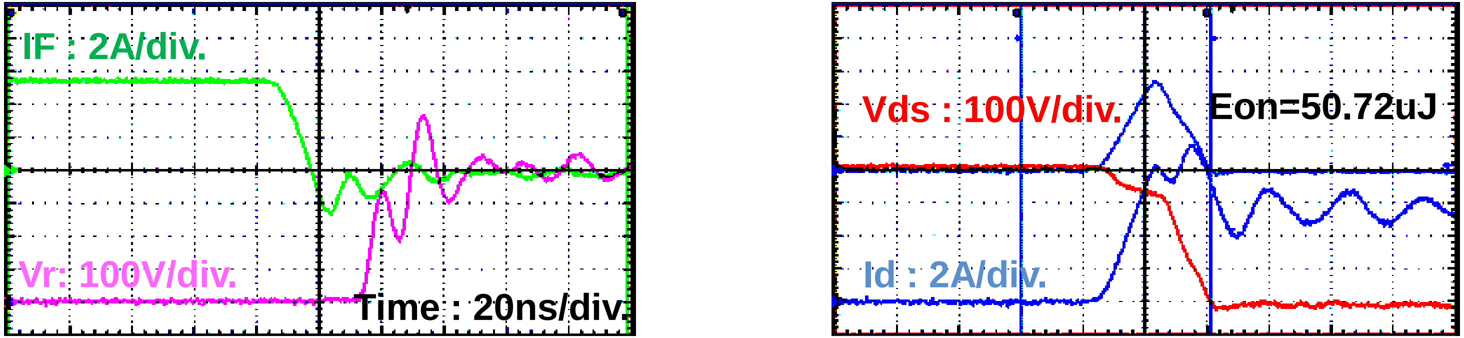




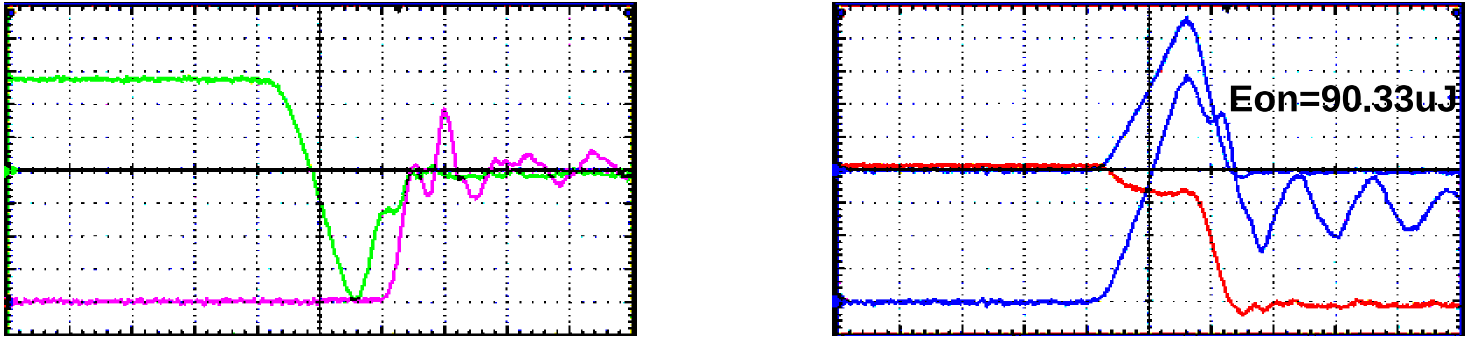


Effect of Clamp Diodes at Turn On

Si Diode vs SiC Schottky Diode



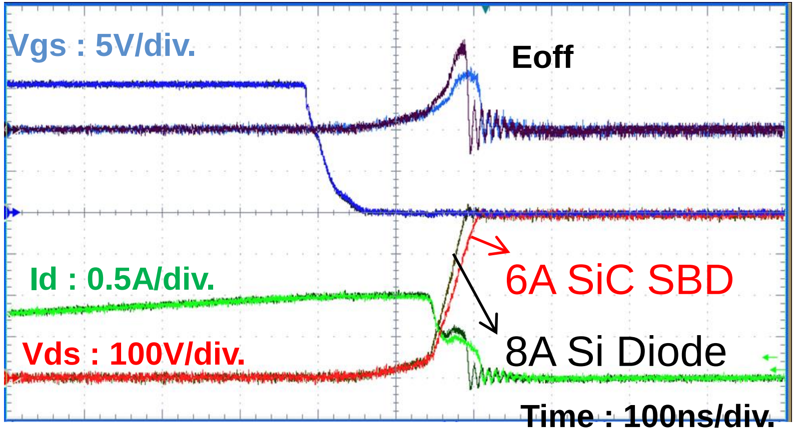
Diode & MOSFET waveforms @ Turn-on with SiC Schottky diode



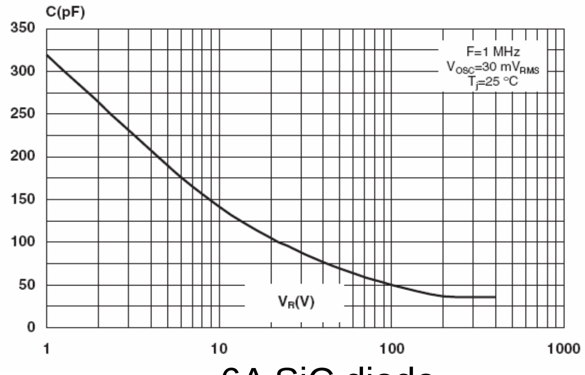
Diode & MOSFET waveforms @ Turn-on with Si diode

Effect of Clamp Diodes at Turn Off

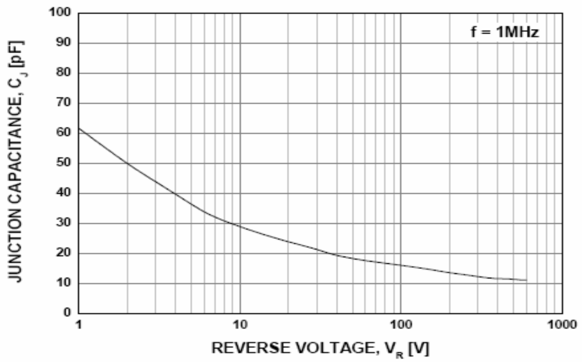
Si Diode vs SiC Schottky Diode



Turn off @ Id=1A, Rg=4.7 Ω with 6A SiC SBD (Ref : 8A Si Diode)

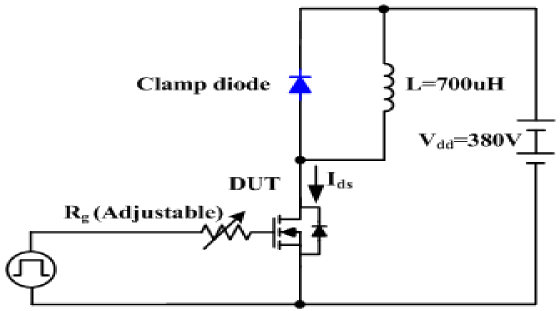


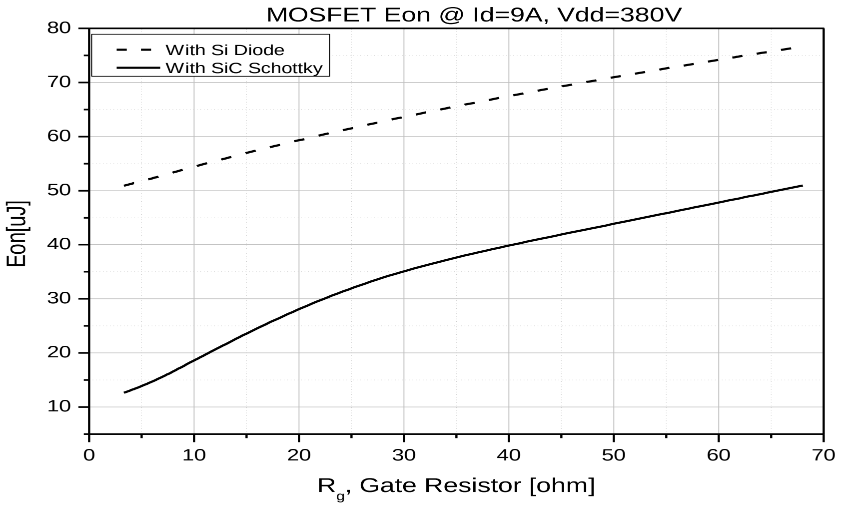
6A SiC diode

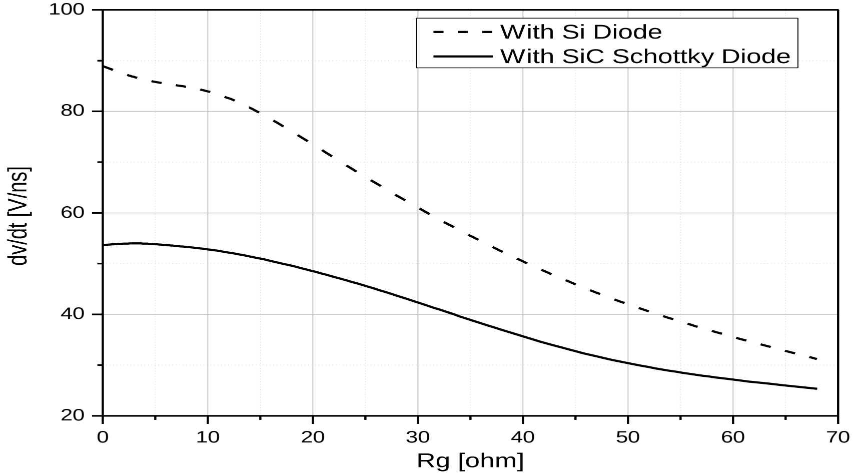


8A Si Diode

Effect of Clamp Diodes
Si Diode vs SiC Schottky Diode

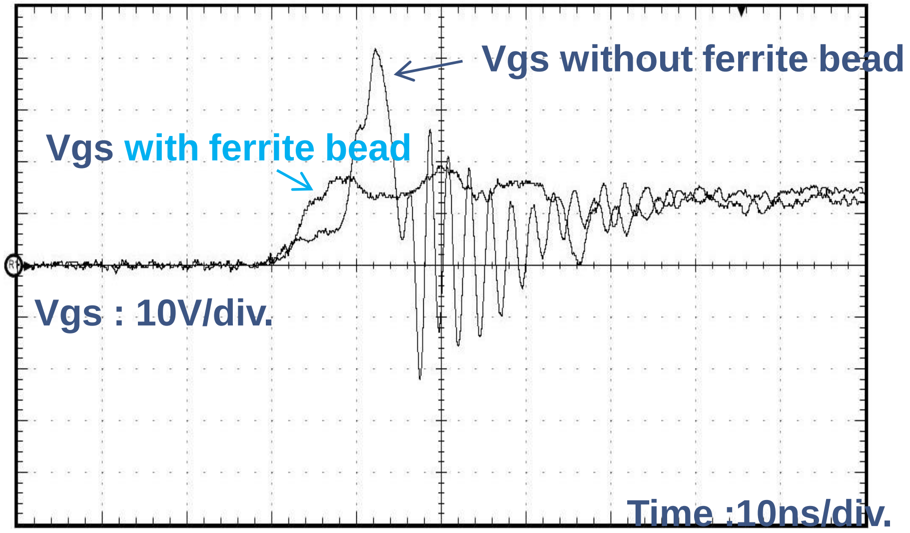




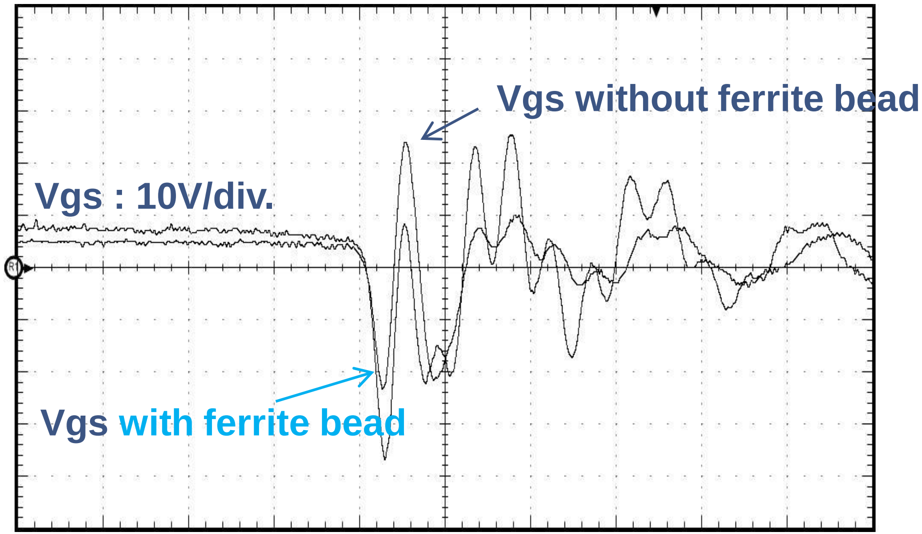


- SiC Schottky diode is optimized device for extremely fast switching MOSFET.

Effects of Ferrite Bead

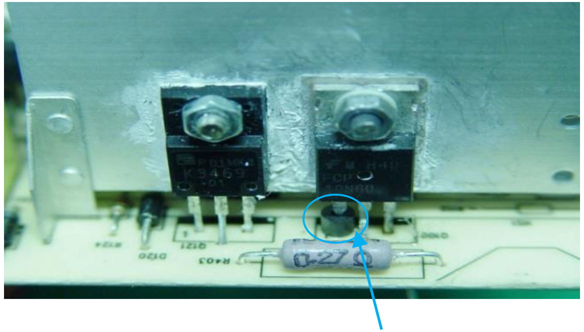


(a) Vgs at Turn-on Transient

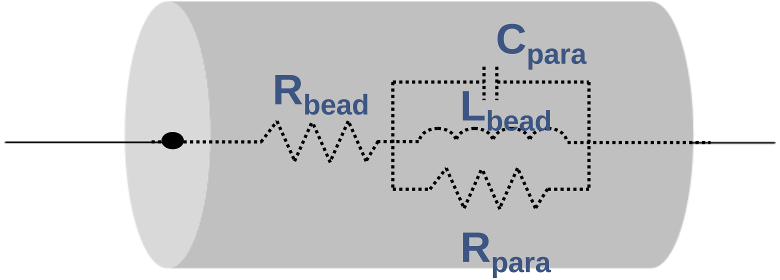


(b) Vgs at Turn-off Transient

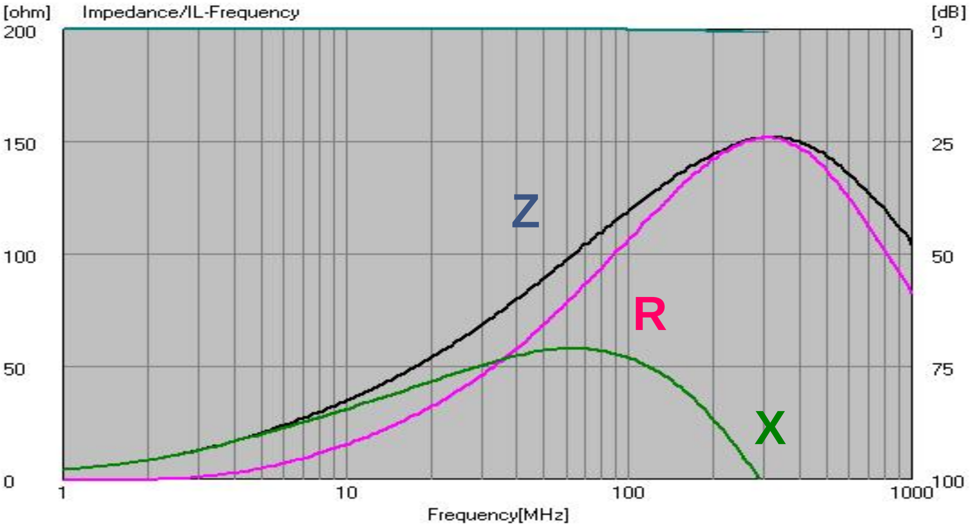
Equivalent Circuit of Ferrite Bead



Gate Ferrite Bead



$$Z = R + jX$$

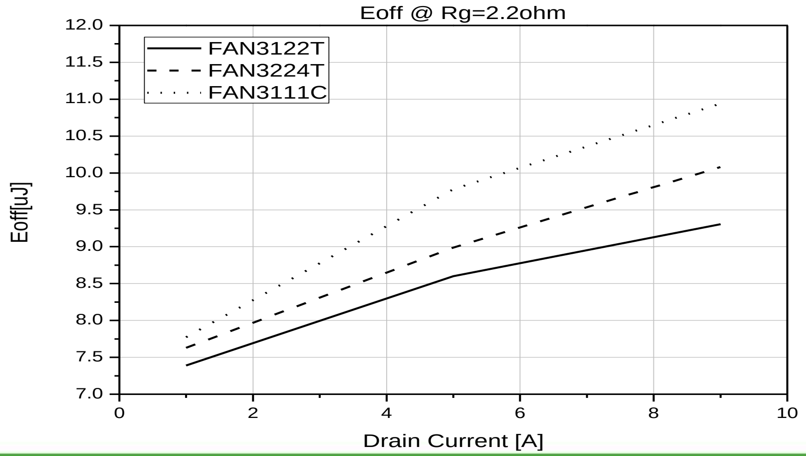


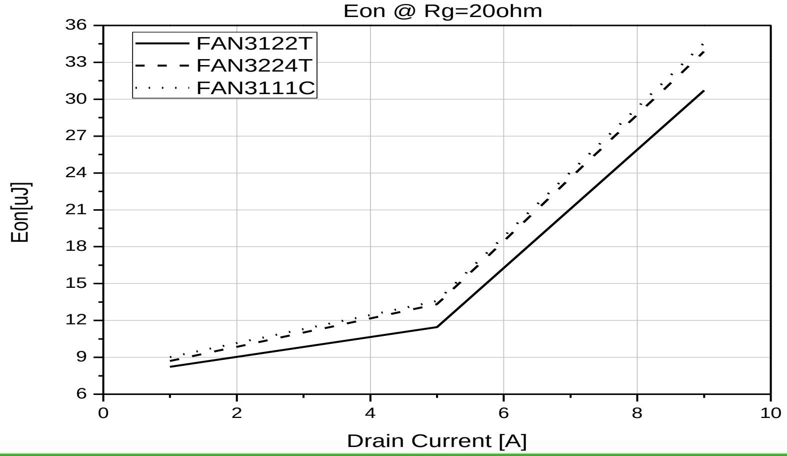
Effects of Current Capability of Driver IC

TABLE I. Comparisons of Critical Specification of Gate Drivers

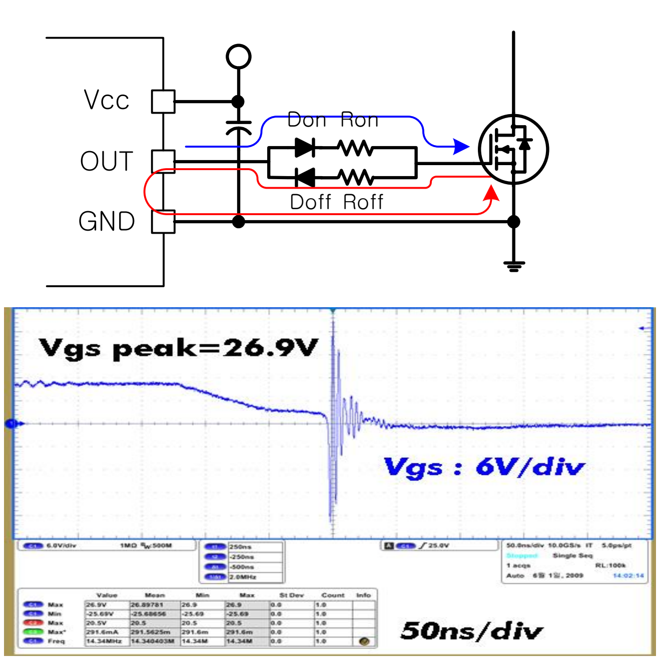
DEVICE	CONDITION	I_{PK_SINK}	I_{PK_SOURCE}
FAN3122T	C_{LOAD}=1.0uF,f=1kHz,Vdd=12V	11.4[A]	-10.6[A]
FAN3224T	C_{LOAD}=1.0uF,f=1kHz,Vdd=12V	5.0[A]	-5.0[A]
FAN3111C	C_{LOAD}=1.0uF,f=1kHz,Vdd=12V	1.4[A]	-1.4[A]

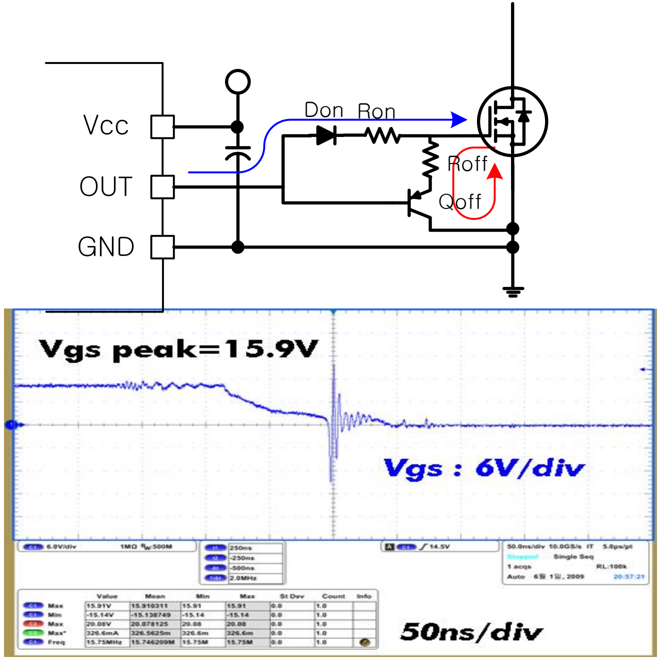
* DUT : FCP16N60N with 6A SiC SBD





Effects of Gate Drive Circuit

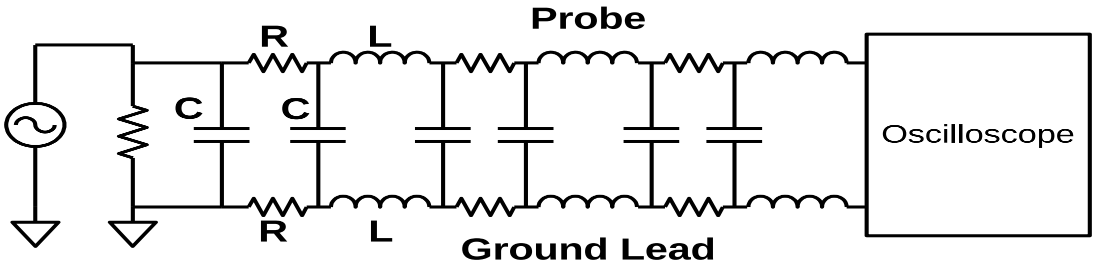




- PNP Tr turn-off can reduce gate ringing.
- It's possible to reduce parasitic components in PCB.
- Keep loop area as small as possible to avoid worse EMI and switching behavior.

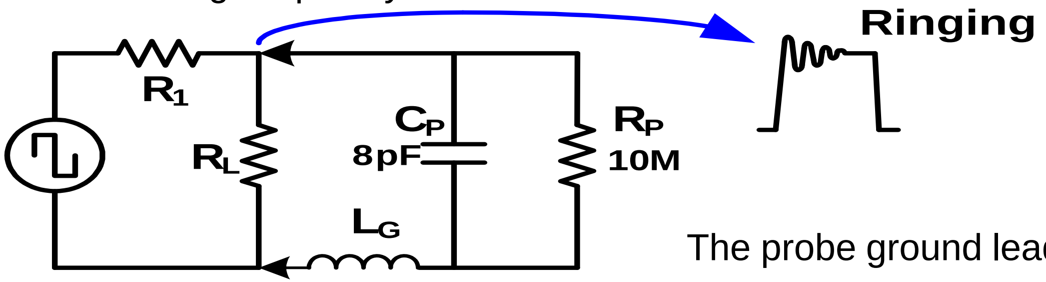
* Ron=10hom, Roff=4.7ohm

Measurement Technique



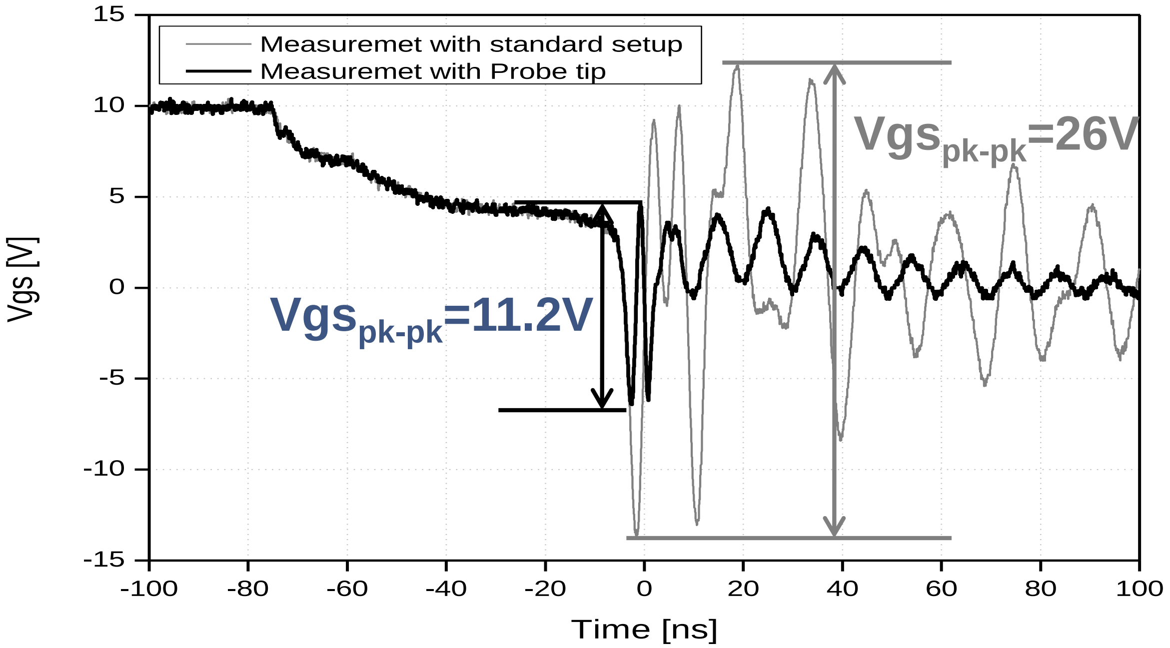
Standard gate probing

Probes are circuits composed of distributed R,L, and C for AC signals. → A total probe impedance varies with switching frequency.

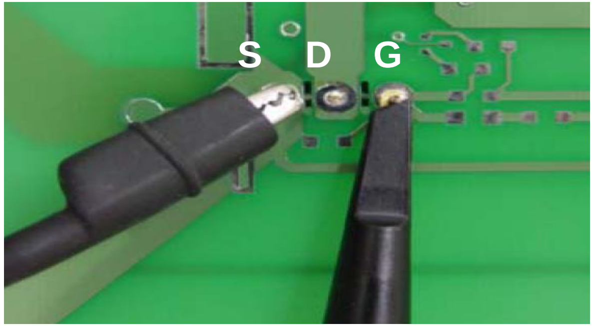


The probe ground lead adds inductance to the circuit.

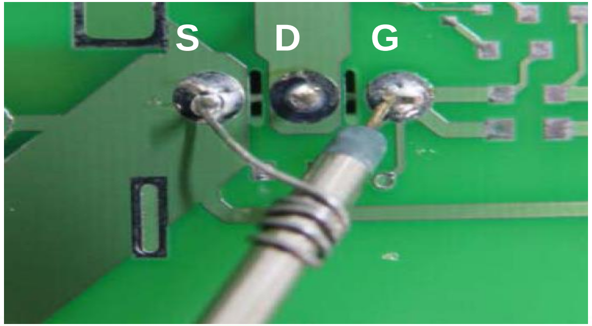
Keep the Loop Probe Small!



- Measurement with standard setup

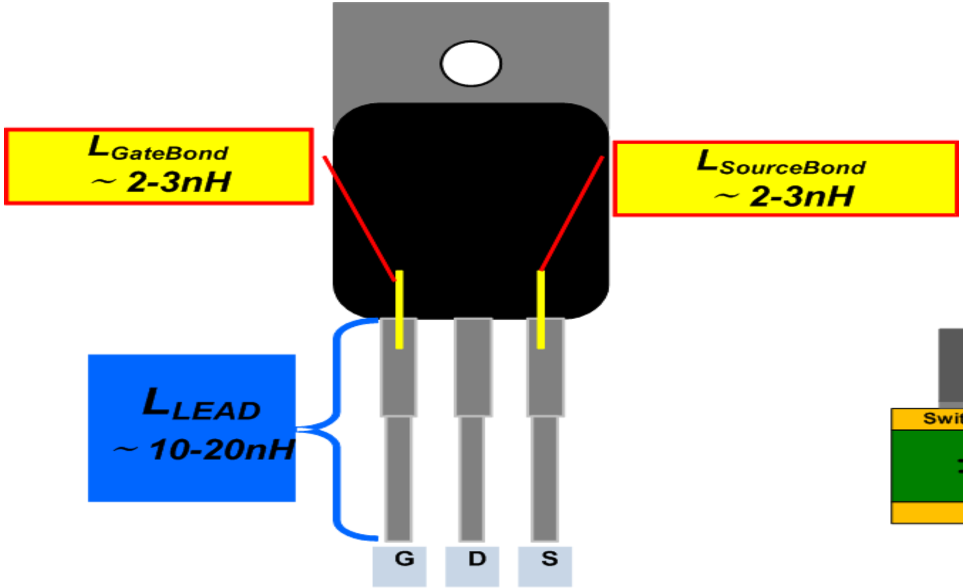


- Measurement with Probe Tip



Package and Layout Parasitics

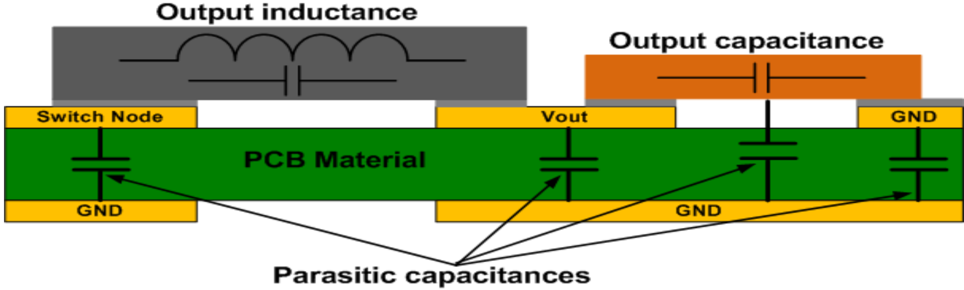
Package parasitics



1cm / 0.25mm trace (L/W) ≈ 6-10nH

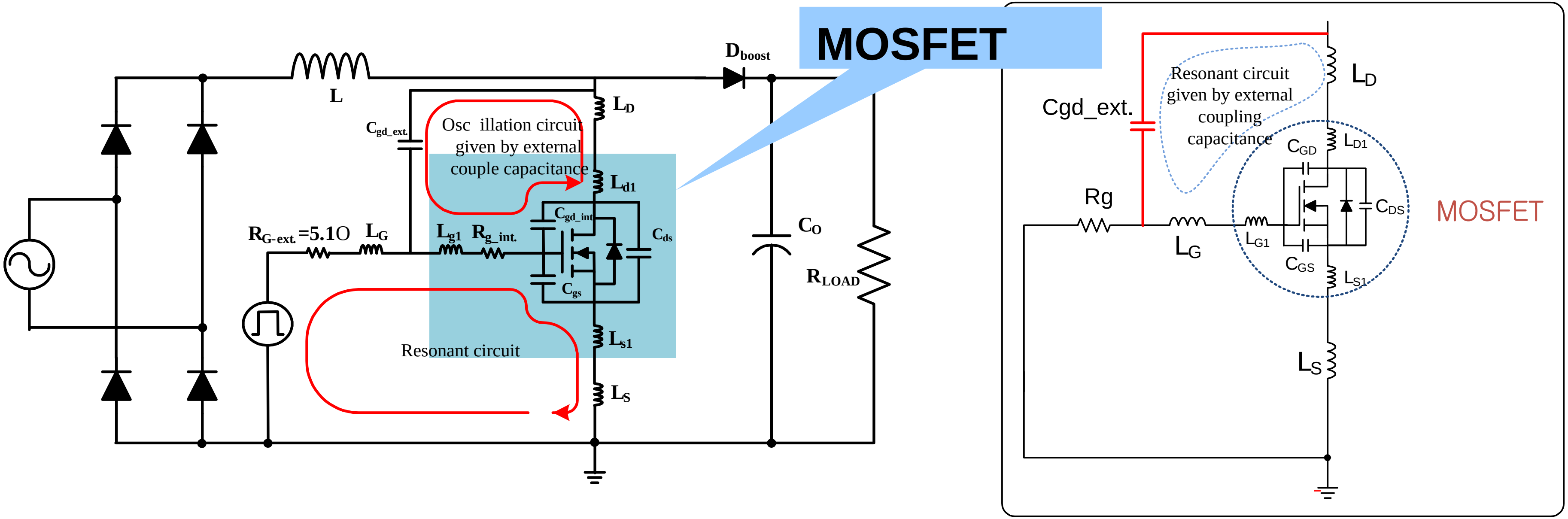
L=10nH, di/dt=500A/µs → V_{ind}=5V
L=10nH, di/dt=1,000A/µs → V_{ind}=10V

Layout parasitics



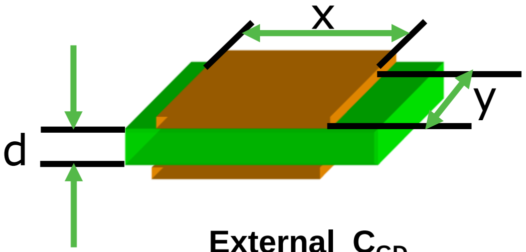
A lot of layout parasitic has to be considered!

MOSFET Oscillation Circuit



A lot of layout parasitic has to be considered!

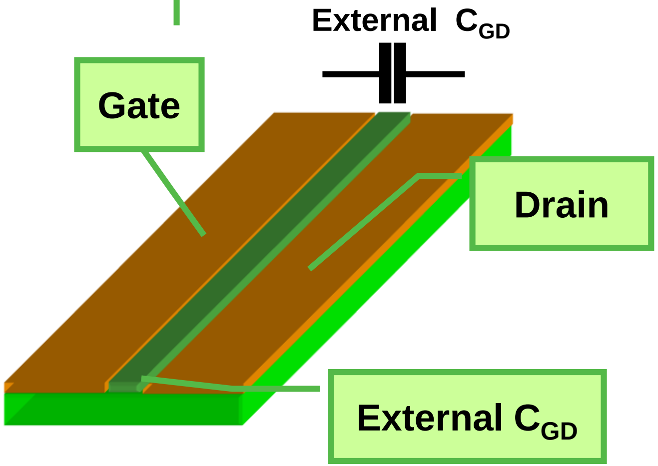
Layout Capacitance
Example with High External C_{GD}



$$A = x \cdot y$$

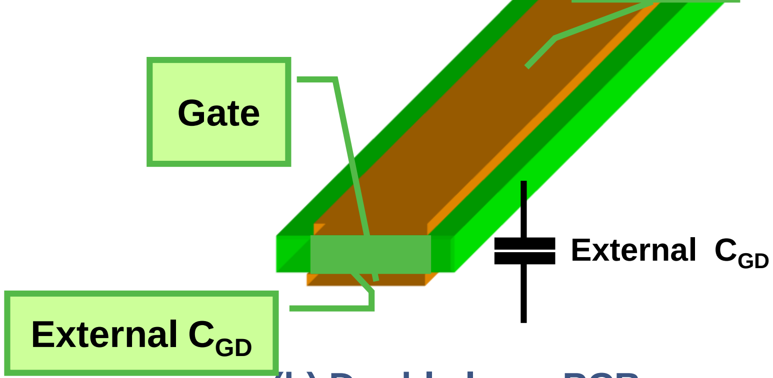
$$C = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot A}{d}$$

Capacity between trace pitches



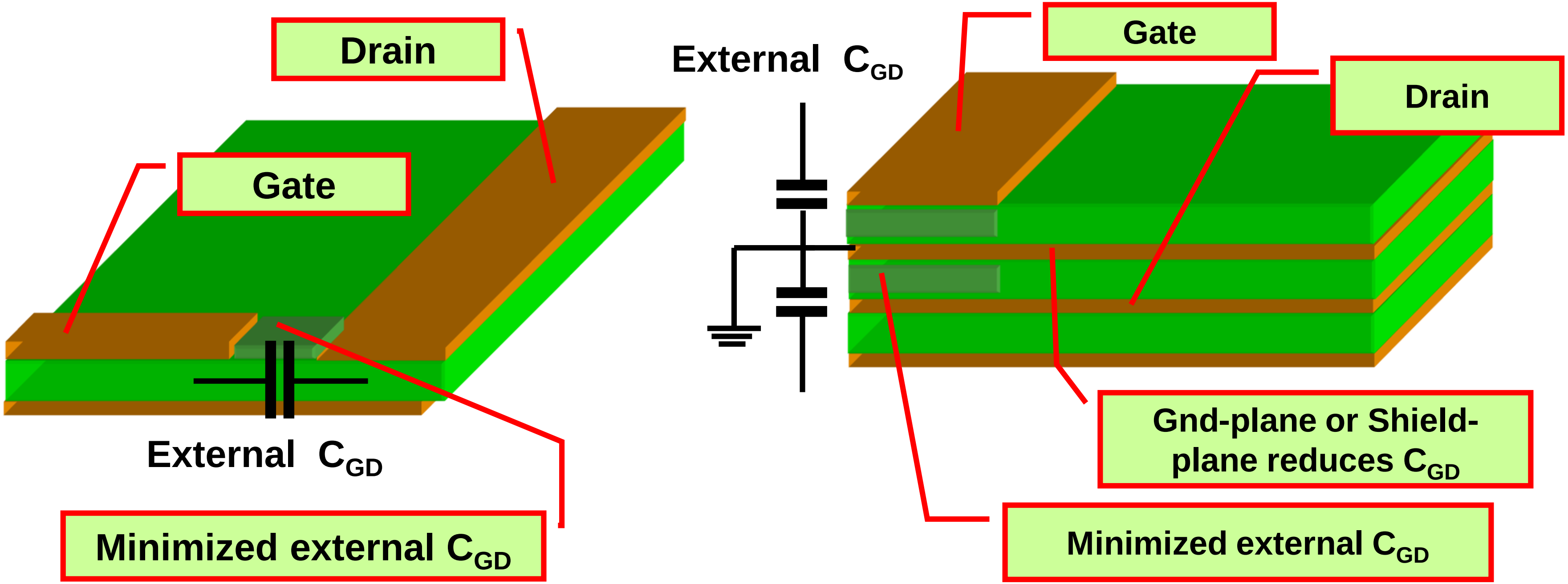
(a) Single layer PCB

External C_{GD} too high!!



(b) Double layer PCB

Layout Capacitance
Examples with Reduced External C_{GD}



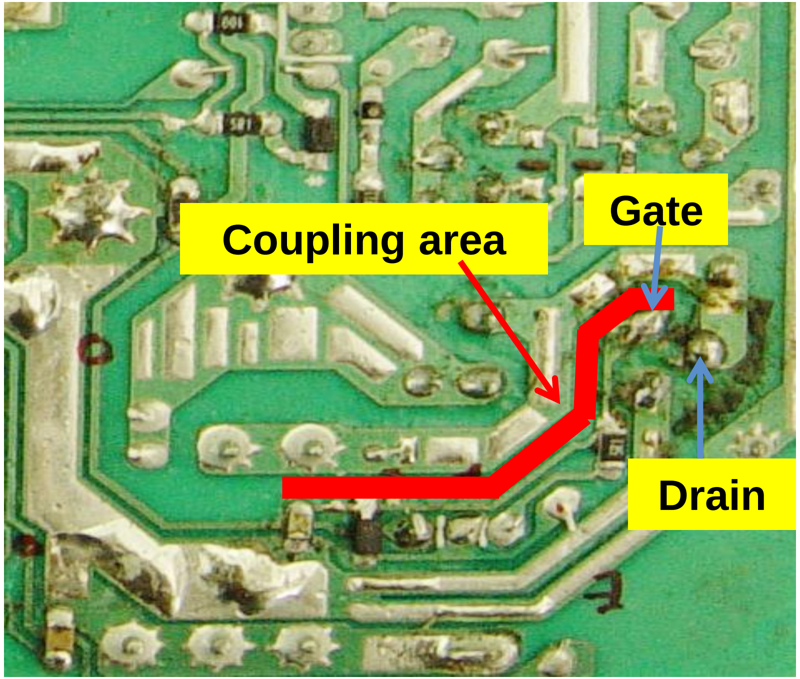
(a) double layer PCB

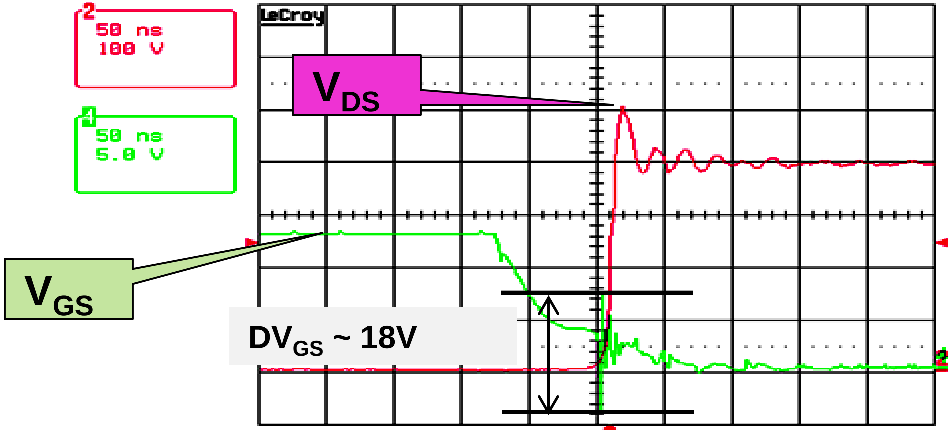
Both solutions allow use of SJ Devices

(b) multi layer PCB

Layout Example Large External C_{GD}
Vgs Shows Higher Spikes During Turn Off

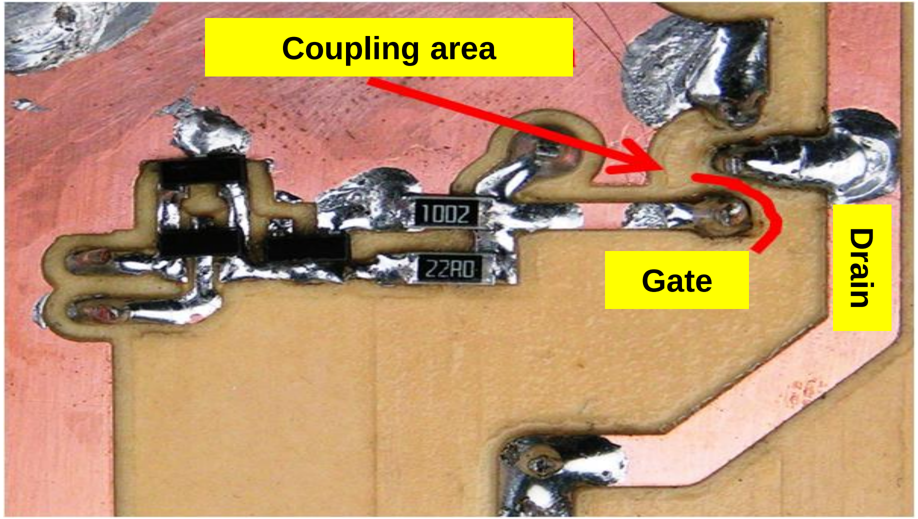
PCB example with large external C_{GD}

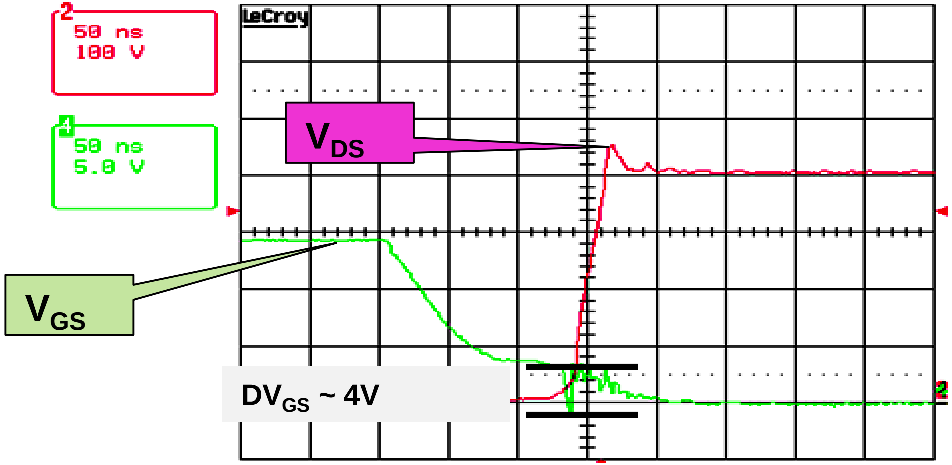




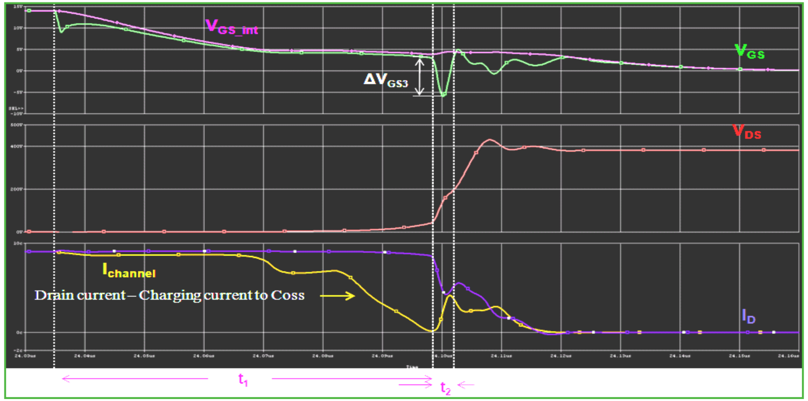
Layout Example Small External C_{GD}
Vgs Shows Lower Spikes During Turn Off

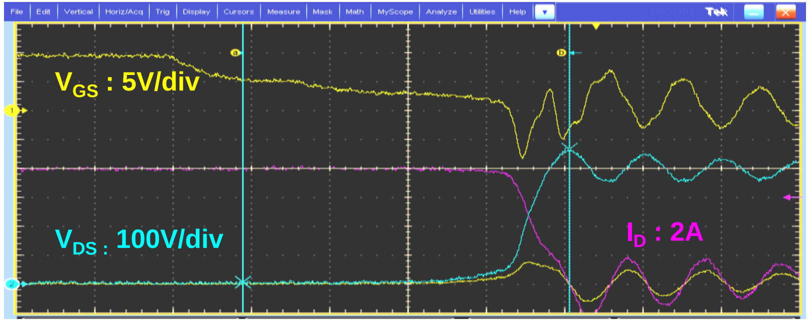
PCB example with small external C_{GD}

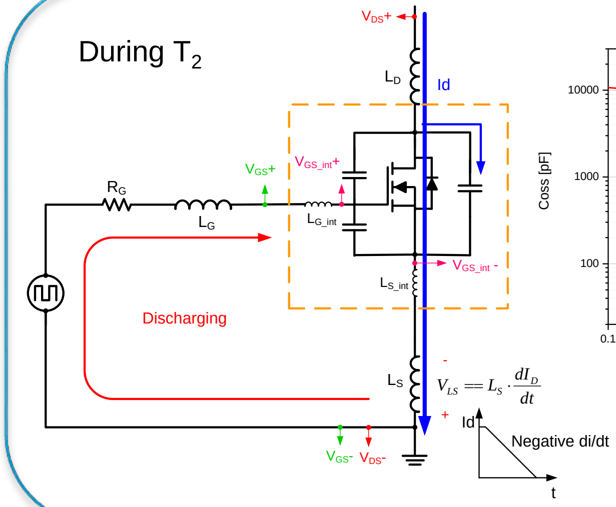


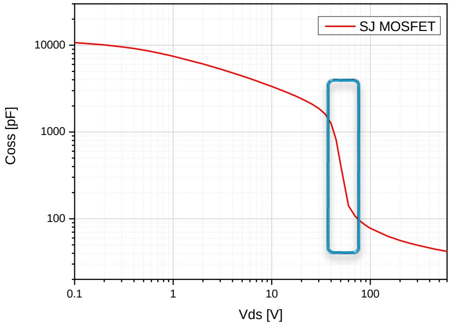


Turn-off Gate Oscillation Mechanism



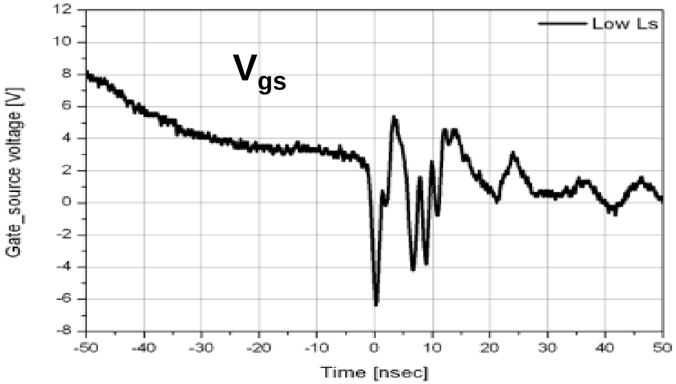




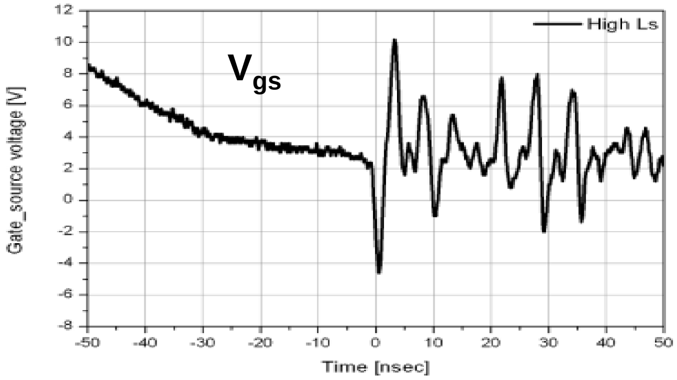


- **Keep the commutation loop as small as possible!**
- **Minimize the source inductance and sensing resistor inductance**

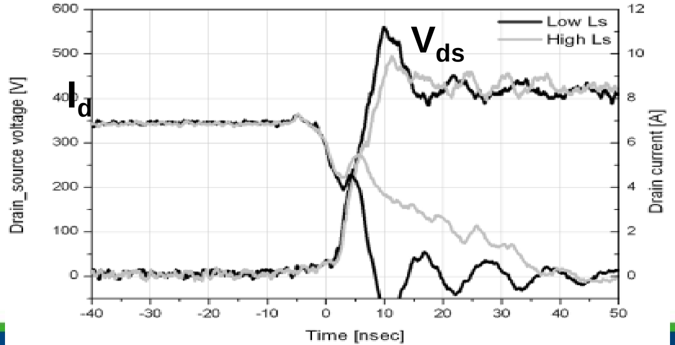
Effects of Source Inductance
LS=1n and 10nH



(a) V_{gs} waveform for low L_S



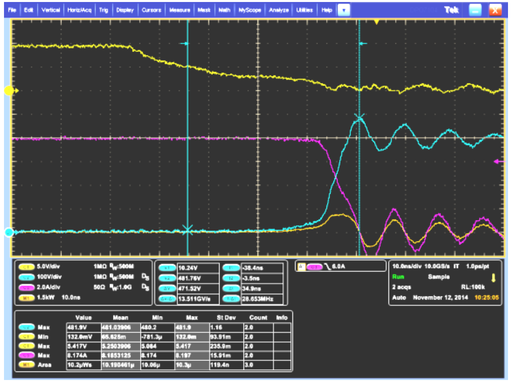
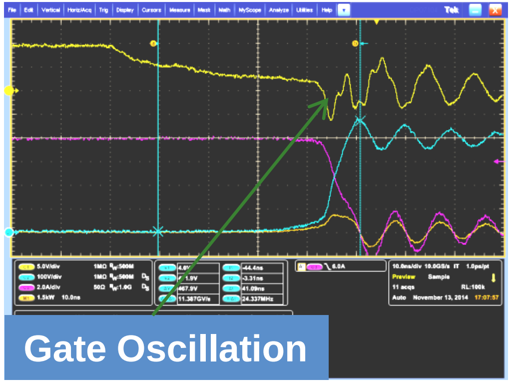
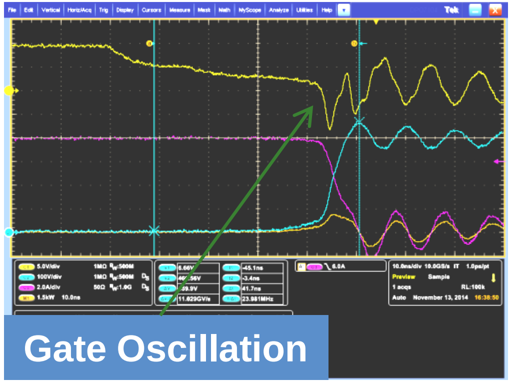
(b) V_{gs} waveform for High L_S



(c) V_{ds} and I_d waveform

* Topology : 500W Interleaved CRM PFC
* MOSFET : FCPF13N60N
* Diode : FFPF20UP60DN
* Gate Resistor : Ron=51ohm, Roff=10ohm

Gate oscillation vs Package
Through hole vs SMD vs Kelvin source SMD

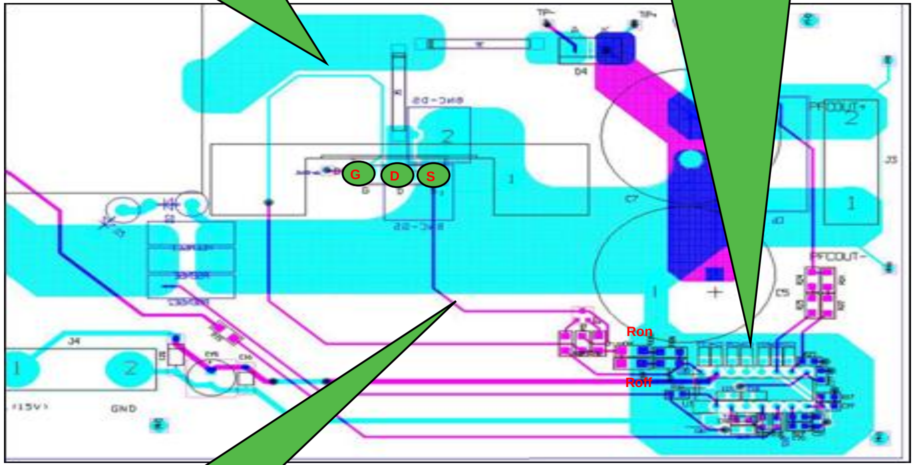
I_D=8A	600V/199mΩ, Power88	600V/199mΩ, D2PAK	600V/199mΩ, TO220
	Kelvin Source SMD	SMD	Through hole
Turn-off Transient			

Design Tips - Practical Layout Example – Boost PFC

Bad Layout:

Increased external G-D capacitance

Driver and gate resistor far away from gate pin of MOSFET

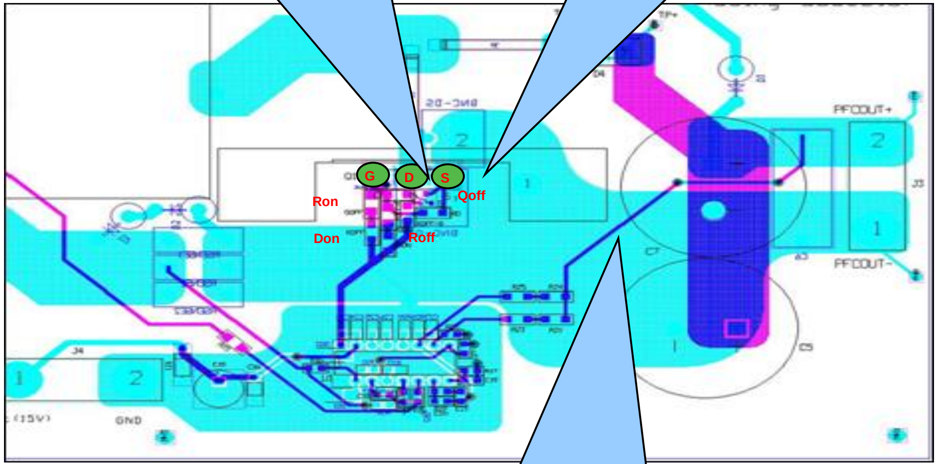


Long gate path

Good Layout:

Connect the driver-stage Gnd directly to the source pin to achieve best performance

Driver & Rg as close as possible to the gate pin of MOSFET

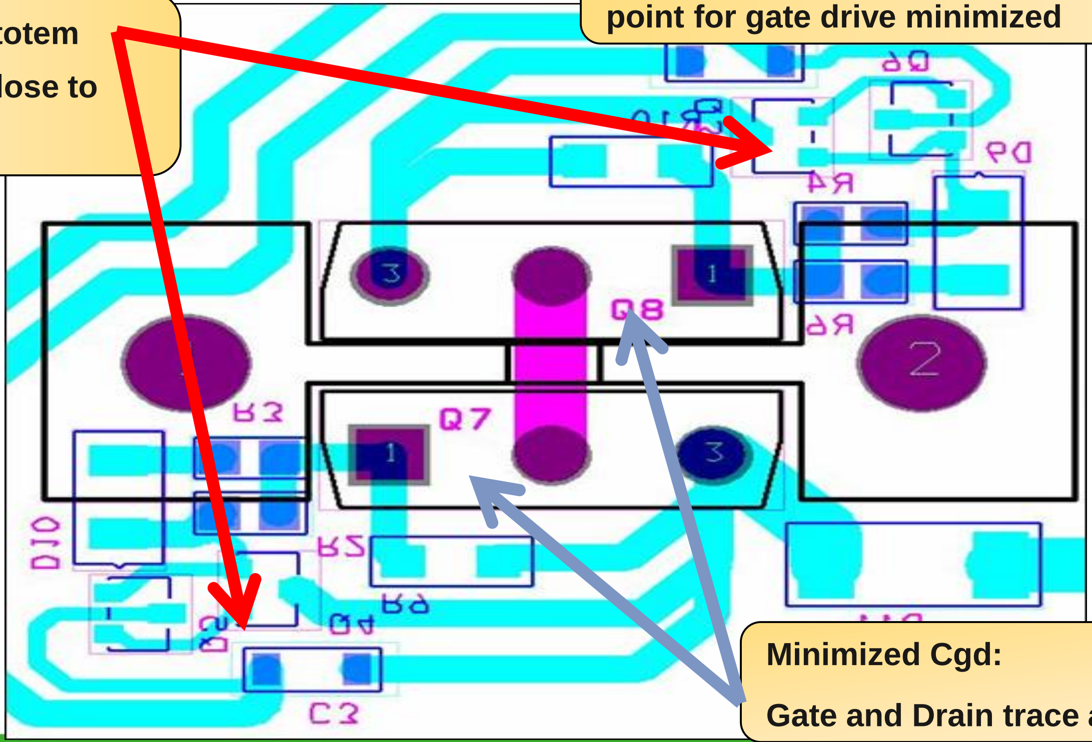


Separate Power GND and gate driver GND

Design Tips - Practical Layout Example - Paralleling MOSFETs

Minimized source inductance to reference point for gate drive minimized

Two independent totem pole drivers very close to MOSFET gate



Minimized Cgd:

Gate and Drain trace at 90° angle

Summary
How to Use Super-Junction MOSFET in Practical Layouts

- To achieve the best performance of Super-Junction MOSFETs, optimized layout is required
- Gate driver and Rg must be placed as close as possible to the MOSFET gate pin
- Separate POWER GND and GATE Driver GND
- Minimize parasitic C_{gd} capacitance and source inductance on PCB
- For paralleling Super-Junction MOSFETs, symmetrical layout is mandatory
- Slow down dv/dt, di/dt by increasing Rg or using ferrite bead

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