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# High–Density AC–DC Power Supplies using Active–Clamp Flyback Topology

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### High–Density AC–DC Power Supplies using Active–Clamp Flyback Topology

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#### Abstract:

This paper introduces the principle of operation of the active clamp flyback topology along with its merits and demerits. Also, a technique to improve its light load efficiency and standby power to pass various regulatory standards is presented. Further, a step-by-step methodology to design an ac-dc power supply using active clamp flyback topology is presented. Finally, performance data of a 65-W ultra-high density active-clamp flyback board is presented.

#### INTRODUCTION

The quest for high density power supplies is not new. It is a trend that is firmly established in low- and medium-voltage dc-dc power supplies. The ac-dc market has been largely immune to it. There are three main reasons: below 150 kHz EMI standards are less stringent. Therefore, switching frequency is typically limited so that the fundamental frequency of the EMI emissions is below 150 kHz. Passives-mainly transformer core materials did not keep up with the pace of innovation seen in the semiconductor industry and finally, high-voltage (> 650 V) switches had poor Figure of Merit (FoM) till very recently. The first limitation could be overcome with new Zero Voltage Switching (ZVS) which substantially limits EMI emissions. With advances made in high voltage FETs including new and exciting wide bandgap semiconductor devices, new topologies are in play. One such topology is Active-Clamp Flyback (ACF).

ACF has appeared in literature since the mid-1990s [1]. However, it has not been widely adopted and has seen success only in low-volume designs. The ACF topology utilizes the energy stored in the parasitic elements to achieve ZVS instead of dissipating it in the snubber circuit. The waveforms resulting from active clamp operation are free of spikes that occur due to parasitics resulting in better EMI than other conventional techniques. The classical flyback topology with RCD snubber has reached its limitation in terms of efficiency and power density. ACF solves the efficiency puzzle while lowering EMI emissions.

This paper has been organized into following sections:

- Introduction to active clamp flyback operation,
- Introduce the problem of light load efficiency & standby power in the ACF,
- Introduction to the NCP1568 and how it addresses the light load efficiency problem,
- Design equations for transformer selection of the ACF,
- Primary and secondary component selection considerations,
- Performance data of ultra-high density active clamp flyback board.



Figure 1. Simplified Active Clamp Flyback

#### THEORY OF OPERATION

In steady-state operation the ACF topology works in two different moded: energy storage mode and resonant power delivery mode.

#### A. Energy Storage Mode

The operation during the energy storage mode is similar to that of a standard flyback. When the main FET is turned on, the energy is stored in the transformer. The diode in the secondary side is reverse biased and hence no power transfer occurs. The magnetizing current in the ACF always works in Continuous Conduction Mode (CCM). The input voltage to output voltage relationship is given by:

$$V_{out} = V_{in} \cdot \frac{N_s}{N_P} \cdot \frac{D}{1 - D}$$
 (eq. 1)

Where, D is the duty cycle and  $N_S/N_P$  is the turns ratio.











(A) Energy Storage Mode.

(B) Transition from Energy Storage Mode to Resonant Power Delivery Mode.

(C) Resonant Power Delivery Mode.

(D) Transition from Resonant Power Delivery Mode to Energy Storage Mode.

#### Figure 2. Operating States of Active-Clamp Flyback

The flyback transformer shown in the Figure 2 is modeled to contain a leakage inductance,  $L_{leak}$ , a magnetizing inductance,  $L_{mag}$ , and an ideal transformer shown in the gray box. This model is used to demonstrate various currents flowing in an active clamp flyback: primary resonant current (Blue), magnetizing current (Brown) and secondary current (Green). Note that the current flowing in the main FET is upslope of the magnetizing current and the downslope is shown for visualization purpose.

# B. Transition from Energy Storage to Resonant Power Delivery Mode

At the end of the energy storage mode, the main FET is turned-off. The current that is flowing in the primary of the transformer continues to flow and charges the output capacitance of the main FET. Once the switch node voltage raises above the clamp capacitor voltage, it forward biases the body diode of the active clamp FET. Activating the active clamp FET at this instant results in ZVS turn-on. Since this transition is for a short duration the lump capacitor charging can be modeled linearly. It is given by:

$$T_{charge} = \frac{C_{lump} \cdot \left(V_{in} + V_{clamp}\right)}{I_{m(peak)}}$$
(eq. 2)

The active clamp capacitor voltage is given by:

$$V_{clamp} = \frac{V_{in} \cdot D}{1 - D}$$
 (eq. 3)

#### C. Resonant Power Delivery Mode

The activation of the active clamp FET at the end of  $T_{charge}$  starts the resonant power delivery mode. During the resonant power delivery mode, the secondary diode/FET is conducting and power is delivered to the load. During this mode, the leakage inductance starts resonating with the clamp capacitor.

The resonant frequency is given by:

$$F_{res} = \frac{1}{2\pi \sqrt{L_{leak} C_{clamp}}}$$
 (eq. 4)

The resonant current that flows is given by:

$$res = I_m \cos(\omega t)$$
 (eq. 5)

The difference between the primary resonant current and the magnetizing current flows in the secondary. Magnetizing current can be easily visualized by subtracting the primary current with the secondary current times the turns ratio.

The magnetizing current is given by:

$$I_{clamp} = V_{clamp} \cdot \frac{T_{off}}{L_{mag}}$$
 (eq. 6)

The magnetizing current in the ACF topology is always in CCM. Even if the secondary current reaches zero i.e. the secondary current becomes discontinuous and the synchronous rectifier is shutoff, the magnetizing current will always find a path in the primary side. This is due to the addition of the clamp FET. The magnetizing current in ACF works similar to the inductor current in a buck-boost topology. In fact, the primary side of an active clamp flyback resembles a synchronous buck-boost with the clamp capacitor acting as an output capacitor.

#### D. Transition from Resonant Power Delivery Mode to Energy Storage Mode

At the end of the switching period, the active clamp is turned-off. This starts the process of terminating power delivery to the secondary. While the magnetizing inductance is still clamped to the output, the leakage inductance forms a resonant tank with the lump capacitance on the switch node and it starts to ring down. For the capacitance on the switch node to completely discharge the energy stored in the leakage inductor should be greater than the energy stored in the switch node lump capacitor.

$$L_{leak} I_{pri}^2 > C_{lump} V_{SW}^2$$
 (eq. 7)

The voltage on the switch node increases with the input voltage and hence the energy stored in the lump capacitance increases in a parabolic fashion. Therefore, the leakage inductance needed to achieve ZVS can be quite high. To design a transformer with high leakage and tightly controlling its spread in high volume manufacturing adds cost and complexity. One alternative is to add additional resonant inductor. However, it adds volume and designing an efficient resonant inductor is often prohibitive in cost-sensitive applications.



Figure 3. Leakage Inductance Needed to Achieve ZVS for a Universal Input

As shown in Figure 4 the time it takes for the resonance between leakage inductance and lump capacitance to reach its valley point is  $1/4^{\text{th}}$  of a resonant period. Therefore:

$$T_{dis1} = \frac{\pi}{2} \sqrt{L_{leak} C_{lump}}$$
 (eq. 8)

$$V_{valley} = I_{mag(peak)} \sqrt{\frac{L_{leak}}{C_{lump}}}$$
 (eq. 9)

Turning off the clamp FET also initiates the process of the secondary current decaying to zero at a rate dictated by the leakage inductance. Once the secondary current reaches zero, the magnetizing inductance gets unclamped from the output. If the magnetizing inductance is chosen such that the valley of the magnetizing current is negative, after  $T_{dis1}$  magnetizing current starts flowing in the primary and discharges the lump capacitance on the switch node to ground in  $T_{dis2}$ 

$$T_{dis2} = C_{lump} \frac{V_{SW} - V_{valley}}{I_{valley}}$$
 (eq. 10)

At this instant, if the main switch in the primary is turned-on, it results in ZVS of the main switch. This methodology of using a combination of leakage inductance and the negative magnetizing current is shown in the Figure 4 in detail.



Figure 4. Zoomed Waveforms Illustrating ZVS of Main FET



Figure 5. ACF Magnetizing Current Fixed Frequency vs. Frequency Modulation

#### E. Frequency Modulation

As explained earlier, the magnetizing current in an ACF operates always in CCM, therefore, even at light load and standby conditions, the magnetizing current is continuously ramping up and down resulting in additional power loss. Further, for an optimal system performance, the negative valley magnetizing current that is needed to discharge the switch node lump capacitor should be kept at a minimum to lower the conduction losses. Therefore, as load is decreased and as input voltage is increased, the frequency of the operation needs to be increased such that the negative magnetizing current is kept to a minimum. The negative current needed for ZVS is typically in the order of -0.3 A for 600-V super junction FETs. This current could be lower for wide band gap devices such as GaN as their C<sub>oss</sub> is typically lower. In NCP1568, a proprietary frequency modulation technique is implemented to optimize the negative valley current while achieving ZVS.

#### LIGHT LOAD EFFICIENCY AND STANDBY POWER CHALLENGE

The CoC Tier II and DoE energy efficiency standards are stringent and demand excellent efficiency at 10% and standby conditions. For instance, for a 65-W USB PD adapter to meet the stringent CoC Tier II standard, it needs to consume less than 75 mW in standby condition. Frequency modulation while delivering excellent efficiency at medium load condition falls short at light load and standby condition.

At standby i.e. no load condition the magnetizing current cycles up and down with zero average current. Despite ZVS, this phenomenon results in higher conduction and core losses compared to a standard flyback operating in DCM. Furthermore, even with ZVS turn-on the switching losses will be higher than a hard-switching DCM operation because the frequency foldback cannot be implemented if the magnetizing current is in CCM.

Therefore, an optional transition from active clamp flyback mode to DCM flyback is implemented in **onsemi**'s latest PWM IC, NCP1568 – Highly integrated ac-dc Active-Clamp Flyback controller.

#### A. DCM Operation

The ACF topology can be turned into a standard flyback topology by turning-off the active clamp FET. The body diode of the active clamp FET acts as "D" in the RCD clamp. It should be noted that the clamp capacitor is typically much larger than a standard flyback and the characteristics of the body diode of clamp FET is different than that of an ultra-fast rectifier typically used in a standard flyback. At that point typically pure ZVS operation is lost and at light load magnetizing current enters DCM operation. As the load falls further frequency foldback can be implemented and the converter gradually enters into burst mode during no load or standby operation.

Figure 6 shows DCM flyback waveforms. It can be seen that the magnetizing current returns to zero each cycle Further, the SW node starts ringing once the transformer is demagnetized.



Figure 6. DCM Operation Waveforms

In DCM operation, a foldback technique can be implemented in order to achieve excellent light-load efficiency. This can be a linear foldback of frequency or nonlinear foldback or a combination of both. The peak current is typically limited to a minimum value to lower the frequency of operation. Low-frequency operation keeps the switching losses low and turns the main FET on when power delivery is needed. However, a 25-kHz frequency clamp needs to be implemented to prevent operation in the audible range.



Figure 7. Turning ACF Topology into DCM Flyback

*B. Introduction to NCP1568 – Highly Integrated Active Clamp Flyback Controller* 



Figure 8. NCP1568 Pinout

The NCP1568 [2] is a highly-integrated ac-dc PWM controller designed to implement an active clamp flyback topology. The NCP1568 features a 700-V startup circuit, a 2-A low-side driver, and a 5-V logic-level driver for active-clamp FET. It also features a suite of protection features along with direct sensing of ZVS via a 700-V JFET. The NCP1568 is suitable for a variety of applications including ac-dc adapters, industrial, telecom, lighting and other applications where power density is an important requirement.

The NCP1568 implements peak-current-mode control architecture for pulse width modulation. Peak-current-mode control simplifies the loop compensation and typically will result in a simple Type II compensator. With relatively simple compensation schemes, aggressive bandwidths can be achieved compared to a standard voltage-mode control. Further, it inherently provides current limiting while also providing a line feed-forward resulting in excellent line transient response. However, peak-current-mode control is susceptible to subharmonic oscillation for duty ratio greater than 50%. Subharmonic oscillation is characterized by alternating narrow and wide pulse-widths. To prevent subharmonic oscillation, NCP1568 also features additional slope compensation.

The NCP1568 features multi-mode operation to optimize efficiency across line and load conditions. Below are the modes of operation:

- Active Clamp operation with variable frequency,
- Transition from ACF Mode to DCM Mode and vice-versa,
- Discontinuous conduction mode with frequency foldback,
- Skip mode.

In pure ACF mode, NCP1568 implements variable frequency operation as explained in the Frequency Modulation section to optimize negative valley current while achieving ZVS. The multi-mode operation is achieved by comparing the feedback to the voltages programmed on ATH (ACF Threshold) and DTH (DCM Threshold). If the FB voltage is lower than the voltage on DTH, then the part enters DCM operation in a nonlinear fashion as shown in Figure 9. Further, as the load is decreased a linear foldback technique is employed while freezing the peak current. Similarly as the load is increased and the FB crosses ATH voltage the part transitions into ACF mode.

The combination of mandated agency stand-by power and light-load efficiency targets at various load points necessitates the need to change the frequency of operation when the IC is in DCM mode. In DCM operation the frequency is the highest once the FB reaches a programmable  $V_{DTH}$  threshold. As the load decreases, the frequency will keep decreasing until it stops at the minimum frequency clamp of 25 kHz. Figure 9 depicts frequency movement across the load conditions for NCP1568.



Figure 9. Frequency Movement across Load in NCP1568

Since the energy in the leakage inductance is not recycled in DCM operation, the clamp capacitor voltage in DCM operation is greater than the clamp capacitor in ACF operation which is shown in Equation 3. Further, transition from DCM mode to ACF operation or vice-versa should be gradual while allowing the time for the loop to stabilize. Therefore, in NCP1568 while transitioning to active-clamp mode, the energy in the clamp capacitor is slowly discharged by soft-starting the active clamp FET. Leading Edge Modulation (LEM) is employed as shown in Figure 10. LEM allows the main FET to ZVS during transition because turning on the active clamp FET for a brief period discharges the clamp capacitor current and when active clamp FET is shut-off, this current will discharge the lump capacitance. During the active clamp FET soft-start time, its pulse width will increase gradually from a minimum of approximately 250 ns to (1-D) T<sub>sw</sub> in a linear fashion.



Figure 10. Leading Edge Modulation of ADRV during DCM to ACF

Figure 10 shows that the secondary current shape starts to resemble that of resonant current during the LEM period and eventually resonant current can be seen throughout the 1–D cycle as the soft-start is finished.

#### C. DCM Operation Determination

The efficiency sweet spot for active clamp operation versus DCM operation can vary from system to system. The sweet spot depends on conduction losses in the primary vs. the switching losses. The NCP1568 can be configured to operate in pure ACF operation and/or pure DCM operation. The best method to determine transition point is to configure them in pure DCM and ACF mode respectively and gather efficiency at light and medium loads. In the following example, efficiency was gathered at loads less than 50% for a 3-A, 20-V output.



Figure 11. ACF vs DCM Efficiency at Light Load

Once the efficiency is gathered then the transition point can be determined. In NCP1568, FB (compensated output

voltage error signal) is used to determine transitioning from ACF to DCM or vice-versa via the ATH and DTH pins. In the above example, the idea transition point is 0.7 A of load current which is roughly 25 % of load current.

#### TRANSFORMER DESIGN

To illustrate transformer design for an ac-ac power supply utilizing active clamp flyback, following specifications compliant with USB PD 2.0 and passing stringent DoE and CoC Tier II efficiency standards are assumed.

Since ACF can increase the power density of the power supply for aforementioned reasons, a maximum frequency of 400 kHz is assumed for this design. This is approximately 3.25 to 4 times the maximum frequency of operation of standard 65-W ac-dc adapters. 400 kHz is a good compromise between high power density and what can be achieved using the industry standard 600-V super-junction MOSFETs.

Description	Min	Тур	Мах	Unit
Input Voltage	85		265	Vrms
Line Frequency	47		63	Hz
Min Output Voltage	4.75	5	5.25	V
Max Output Voltage	19	20	21	V
Output Current	0		3.0	А
Target Efficiency		93		%
Frequency ACF	100		400	kHz
Max Power			60	W

#### Table 1. SPECIFICATIONS OF THE DESIGN INPUTS

#### A. Turns Ratio

The turns ratio of the transformer can be calculated by assuming a maximum duty cycle of 50% at lowest input voltage while delivering maximum power. The duty ratio of NCP1568 is internally limited to 80%. This allows additional room to account for transients and other non-ideal conditions while delivering full power.

$$N_{PS} = \frac{D_{max} \cdot V_{in(min)}}{(1 - D_{max}) \cdot V_{out(max)}}$$
(eq. 11)

For the conditions mentioned in Table 1, Equation 11 results in a turns ratio of 6. With the primary to secondary turns ratio calculated, the designer must check the minimum on-time to ensure that it is not less than the minimum on-time of the IC. The minimum on-time must be checked at maximum frequency at the highest input voltage and must also be checked at the minimum operating frequency at the highest input voltage in case of variable output design.

$$T_{min1} = \frac{N_{ps} \cdot V_{out(max)}}{(N_{PS} \cdot V_{out(min)} + V_{in(max)}) \cdot F_{max}} \quad (eq. 12)$$

$$T_{min2} = \frac{N_{ps} \cdot V_{out(min)}}{(N_{PS} \cdot V_{out(min)} + V_{in(max)}) \cdot F_{min}} \quad (eq. 13)$$

The minimum on-time of NCP1568 is about 200 ns. The calculated minimum on-time from Equations 12 and 13 is 600 ns and 700 ns respectively, well above the capability of the IC. If the calculated minimum on-time is lower than the minimum on-time of the IC, then the turns ratio or frequency has to be iterated.

To calculate magnetizing inductance we need to know the desired swing of the magnetizing current ( $\Delta I$ ). However, since we are employing negative magnetizing current to achieve ZVS. Therefore, the negative current needed to discharge a 600 V super junction FET needs to be calculated.

#### B. Valley Current needed to achieve ZVS

The energy needed to achieveZVS can be calculated by approximating the capacitance on the switch node during the discharge of the node. The capacitance can be simplified as a term referred to as Clump. Clump is a summation of all capacitances that connect to the switch node directly via the primary side or indirectly through windings on the transformer. For the design of the transformer, a simplifying assumption can be made that the major contributing capacitances are the low side MOSFET, the high side MOSFET, and the secondary side MOSFET. Only the worst case capacitance of these devices will be used which is at maximum input voltage. The capacitance can be found on most high voltage MOSFET datasheets and is referred to energy related output capacitance or Co(er). For ease of calculation, these numbers will be assumed as the following: the high side and low side MOSFET have a Co(er) of 98 pF and the secondary side 150 pF Co(er) is estimated at 800 pF.

The three capacitances are combined and the valley current is estimated in the following equations.

$$C_{lump} = C_{o(er)Q1} + C_{o(er)Q2} + \frac{C_{o(er)Q3}}{N_{PS}^2}$$
 (eq. 14)

The above formula results in lump capacitance on SW node,  $C_{lump}$ , of 220 pF.

$$I_{valley} = C_{lump} \cdot \frac{N_{PS} \cdot V_{Out} + V_{in}}{T_{reg}}$$
 (eq. 15)

The above calculations are the worst-case negative currents and the designer should note that the amount of negative current required to discharge the capacitance varies with changes in line and output voltage. The valley current can be used to calculate the primary inductance. If the capacitance is not known, a good rule of thumb is to use a negative current of 300 mA for SJ MOSFETs and about 150 mA for eGaN HEMTs.

#### C. Inductance Calculation

The inductance should be calculated at the minimum input voltage and the minimum output voltage. The NCP1568 features ZVS-based frequency modulation where the frequency of operation is lowest at the minimum input voltage and minimum output voltage and maximum load current. For this specification 100 kHz is assumed. If the designer would like some margin in the design, the maximum output current in Equation 16 can be increased.

$$L_{mag} = \frac{V_{in(min)} \cdot D_{min}}{2 \cdot F_{SW(min)} \left( \frac{I_{out(max)}}{(1 - D_{min}) N_{PS}} - I_{valley} \right)}$$
(eq. 16)

Where, minimum duty cycle, D<sub>min</sub>, is given by:

$$D_{min} = \frac{V_{out(min)} \cdot N_{PS}}{V_{out(min)} \cdot N_{PS} + V_{in(min)}}$$
(eq. 17)

Equation 16 results in a magnetizing inductance of 129  $\mu$ H. For this design an inductance of 120  $\mu$ H will be selected. Figure 12 shows the how inductance varies with negative valley current requirement. Higher the current lower the inductance and hence higher the flux swing.



Figure 12. Negative Valley Current Requirement

#### D. Primary and Secondary Turns

While selecting the number of turns on the primary side of the transformer, the cross sectional area and material must be taken into account to optimize the efficiency and power density. This process is typically iterative. The goal of this design is to demonstrate highest possible power density. Therefore, a relatively small RM8LP style core was chosen. The cross sectional area  $A_e$  for the transformer is 64.9 mm<sup>2</sup>.  $I_{PK}$  is the peak drain current specified in Equation 22 and  $\Delta B$ is the flux density swing. A flux density of 0.2 T will be selected for the Active Clamp Flyback that is operating between 100 kHz and 400 kHz.

$$N_{P} = \frac{L_{mag} \cdot \left(\frac{I_{out(max)}}{(1 - D_{min}) \cdot N_{PS}} - I_{valley}\right)}{\Delta BA_{e}} \qquad (eq. 18)$$

Above equation results in primary turns of 23.1. For the sake of simplicity, an even number of 24 turns has been selected for this design. Hitachi ML29D core material was selected for this design since it exhibited low core loss at high frequency. The core losses can be estimated from the core material datasheet where the power loss per unit volume is specified at 200 kHz. ML29D shows a flat loss curve over the temperate range. But, for other materials core loss vs. temperature needs to be accounted.

$$RM8LP_{Loss} = P_{LossV} \times Volume_{RM8LP}$$
 (eq. 19)

Equation 19 results in 1.8 W of loss which is 3.0% of hit in efficiency.

The turns ratio was established earlier and thus the number of secondary windings can be calculated as shown below:

$$N_{S} = \frac{N_{P}}{N_{PS}}$$
 (eq. 20)

Plugging in the values, the number of turns in the secondary is 4 turns.

## KEY PRIMARY AND SECONDARY COMPONENT SELECTION

#### A. Clamp Capacitor

The clamp capacitance should be calculated such that at the lowest frequency of operation and lowest duty cycle, the resonance period of the  $L_{leak}$  and  $C_{clamp}$  is 1/2 the resonant period.

$$C_{Clamp} = \left[\frac{D_{min}}{F_{min}}\right]^2 \times \frac{1}{0.5 L_{leak} \pi^2}$$
 (eq. 21)

This results in  $C_{clamp}$  of 300 nF. Three 220 nF ceramic capacitors were chosen for this design since ceramic capacitors can lose up to 50% of its value with dc bias. It should be noted that the clamp capacitor can be smaller if so desired but it can result in higher conduction losses in the secondary and thus slightly lower efficiency.

#### B. Primary Side Current Sense Resistor

To limit power to the output and provide current mode control, a current sense resistor can be placed in series with the low side MOSFET. A maximum output current can be set at 120% of the rated output current. Equation 22 below calculates the peak current at the current limit point at maximum output voltage and rated current.

$$I_{PK} = \frac{I_{LIM}}{(1 - D_{max}) \times N_{PS}} \times 2 - I_{valley} \qquad (eq. 22)$$

The current limit threshold for NCP1568 is set at 800 mV. To meet the goal of having a current limit of 120%, the resistor shown in Equation 23 should be used.

$$R_{S} = \frac{V_{LIM}}{I_{PK}}$$
 (eq. 23)

The power dissipation of the device must be calculated at low line with the highest output voltage at full load to determine its loss.

$$I_{RMS} = I_{PK} \cdot \frac{D}{\sqrt{3}}$$
 (eq. 24)

$$\mathsf{P}_{\mathsf{RS}} = \mathsf{R}_{\mathsf{S}} \cdot \mathsf{I}_{\mathsf{RMS}}^2 \qquad (\mathsf{eq.}\ \mathsf{25})$$

#### C. Main FET & Active Clamp FET Selection

The rms current of the main FET in the primary side is same as Equation 24 noted above. The rms current of the clamp FET [3] is given by:

$$I_{AC(RMS)} = I_{PK} \cdot \sqrt{\frac{1 - D_{min}}{6}} \qquad (eq. 26)$$

#### D. Synchronous Rectifier

The voltage stress on the secondary side can be calculated as follows:

$$V_{SR} = \frac{V_{in(max)}}{N_{PS}} + V_{spike}$$
 (eq. 27)

Assuming a leakage spike of 30 V, the synchronous rectifier should be rated for at least 92.5 V.

All of the switch voltage stresses must be derated to ensure a long operating lifetime for the power supply.

$$V_{SR(max)} = \frac{V_{SR}}{Derate}$$
 (eq. 28)

Assuming a derating factor of 20%, a 120 V FET has been selected for synchronous rectification.

The rms currents in the secondary side can be calculated as follows:

$$I_{sec(RMS)} = \frac{2P_{out}}{V_{out} \cdot \sqrt{2 (1 - D_{min})}}$$
(eq. 29)

This results in secondary rms currents of 3.8 A.

#### E. Output LC Filter

A standard output LC filter similar to other flyback topologies can be used with ACF. However, there is a scope to create a multiple resonant ACF by tuning the output filter [6]. One way is to significantly reduce the capacitor immediately followed by the synchronous rectifier stage and increase the capacitance of the capacitor bank connected directly to the load. This method can create a resonant network while active clamp FET is conducting and help reduce rms currents in the primary while possibly enabling zero current switching in the secondary

#### 60-W ULTRA-HIGH DENSITY ACF BOARD PERFORMANCE

A 60-W ultra-high density ac-dc adapter fully compliant with USB PD 2.0 and efficiency standards set by EU CoC Tier II and US DoE was designed using NCP1568 and the design criteria explained above. The dimensions of the board are  $1.66'' \times 1.78'' \times 0.70''$  (4.2 cm × 4.5 cm × 1.7 cm) resulting in a power density of 31 W/in<sup>3</sup> or 1.7 W/cm<sup>3</sup> The frequency of operation varies from 100 kHz at 90 V rms, 5-Vout output and 3-A load current to 420 kHz operation at 265 V rms, 20-Vout and 1.5-A load current. NCP51530, a 3-A half-bridge driver is used as high side gate drive while the low side is directly driven by the NCP1568. NCP4305, an intelligent SR controller is used to drive the synchronous rectification FET. There is no direct communication between primary and secondary and the SR FET is turned on by NCP4305 by looking at the body diode conduction and is turned off when secondary current reaches zero.

A simplified schematic is shown Figure 14. As any standard flyback, TL431/NCP431 can be used as an error amplifier in the feedback network. Looking at the schematic one can notice that when compared to a standard DCM/QR flyback the additional components are:

• Active-clamp FET,

- Half-bridge driver,
- Additional clamp capacitors.

Thus, the cost adder is minimal while delivering 2 to 3 times the power density of existing solutions.

The efficiency graph at full load output is as shown below.



#### Figure 13. Efficiency vs. Load Current for 20-V Output

At full load the board is at 93.3% efficiency at both low line and high line. The NCP1568 is configured to transition to DCM around 27.5% of load. Therefore, both the 25% and 10% efficiency numbers are captured in DCM operation. This board also delivers excellent standby of < 35 mW at 115 V rms and 230 V rms.

Figure 14 shows a high level schematic of active clamp flyback using NCP1568. A detailed schematic along with layout files and bill of materials can be found on ONSEMI web site. Further, pictures of the high-density board is shown for reference. Figure 16 (A) shows the 2 primary FETs along with NCP1568 controller and NCP51530 driver. Figure 16 (B) shows the RM8LP transformer, EMI choke, and output capacitor.



Figure 14. Typical Schematic of Active-Clamp Flyback with NCP1568

Typical switching waveforms for various output voltages in both ACF and DCM is shown in Figure 16. It can be observed that in ACF mode, the switching frequency increases with both input voltage and output voltage to minimize the negative current to achieve.

Further, it can also be seen that in DCM operation the frequency is relatively flat across the input and output voltage. This is due to the nonlinear foldback shown in Figure 9. The NCP1568 when it enters DCM starts around  $F_{min}/2$ . In this design example, it is 50 kHz.



Figure 15. Thermal Scan of ACF UHD Board at 115 V rms, 60 W



(A)



(B)

Figure 16. Pictures of Active-Clamp Flyback Board



(A) & (B) show ACF operation at 90 V rms and 265 V rms.

(C) & (D) show DCM operation at 90 V rms and 265 V rms.

The waveforms are arranged in descending order of output voltage for all the 4 waveforms.

Top to Bottom: 20 V, 15 V, 12 V, 9 V and 5 V.



#### CONCLUSION

In this paper, an Active-Clamp Flyback (ACF) converter has been described and key design equations introduced.

The advantage of a DCM-operated circuit has been also documented, highlighting the benefits of smoothly transitioning between CCM and DCM. The new Active-Clamp Flyback controller NCP1568 seamlessly toggles between modes and packs all necessary features to build rugged and cost-sensitive converters.

A 60-W demonstrator has been assembled to verify and extract measurement data, confirming the maturity of a high-voltage flyback converter operated in an active-clamp mode.

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