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AN-4154
MOSFETs for 60 W High-Power PoE Applications

Summary

Power over Ethernet (PoE) introduces a new facet to Ethernet networking, delivering DC power through a Category 5E (CAT5E) network cable. It is convenient to install Power Devices (PD); such as IP telephones, wireless LAN access points, and security cameras; without any wall power lines because the CAT5E cable delivers data as well as the power required by those PDs. In addition, the Power Source Equipment (PSE) communicates to the PD first and provides the limited power to PD according to the power class of PD specified by IEEE802.3af and IEEE802.3at standards *(see Table 1)*. The maximum PSE power in IEEE802.3af and IEEE802.3at is 15.4 W and 30 W, respectively. As devices become more complex and functional, they require more power than specified by IEEE 802.3af and IEEE 802.3at. By using four-pair architecture, up-to 60 W can be delivered to a power device. In this application note, four-pair architecture for 60 W high-power PoE is explained and Fairchild's power solutions are presented for an efficient PoE system.

Table 1. IEEE802.3af/at PoE Classifications

Class	IEEE 802.3af Max. PSE Power	IEEE 802.3at Max. PSE Power
0	15.4 W	30 W
1	4 W	4 W
2	7 W	7 W
3	15.4 W	15.4 W
4	15.4 W	30 W

Four-Pair Architecture for High-Power PoE

Figure 1 and Figure 1 show two-pair architecture and four-pair architecture, respectively, to deliver the power and data throughout CAT5E cable from PSE to PD. The two-pair architecture delivers power in a single loop over two pairs of the CAT5E cable. Because CAT5E has a current limitation of 720 mA, two-pair architecture has an available power limitation of 30 W delivered power. In four-pair architecture, up to 60 W available power is possible; delivered to the PD with two current loops over all four pairs at the same time. There are two power devices on the current loop, bridge circuit and hot swap switch, which are the critical to the system reliability.

GreenBridge™

One of main design considerations of the four-pair architecture is to balance the current of two current loops. When a diode bridge is used for polarity protection in the PD, the designer should consider the thermal rush in diode bridge due to the negative temperature coefficient in the worst imbalance current loop. As the junction temperature of diode increases, the forward voltage decreases, resulting in even more current flowing in the hotter diode bridge. Some semiconductor makers propose balance circuits to use extra BJTs, but it adds costs and makes circuit complex.

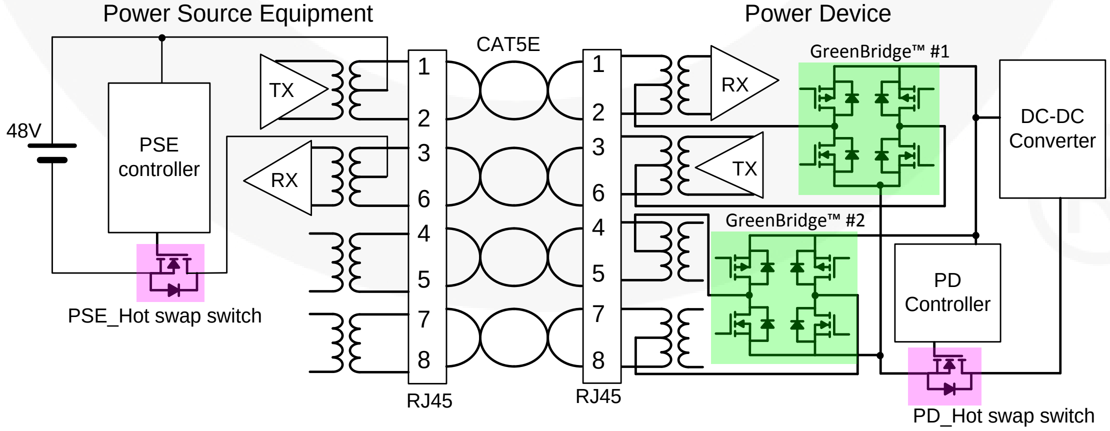


Figure 1. Two-Pair Architecture PoE System

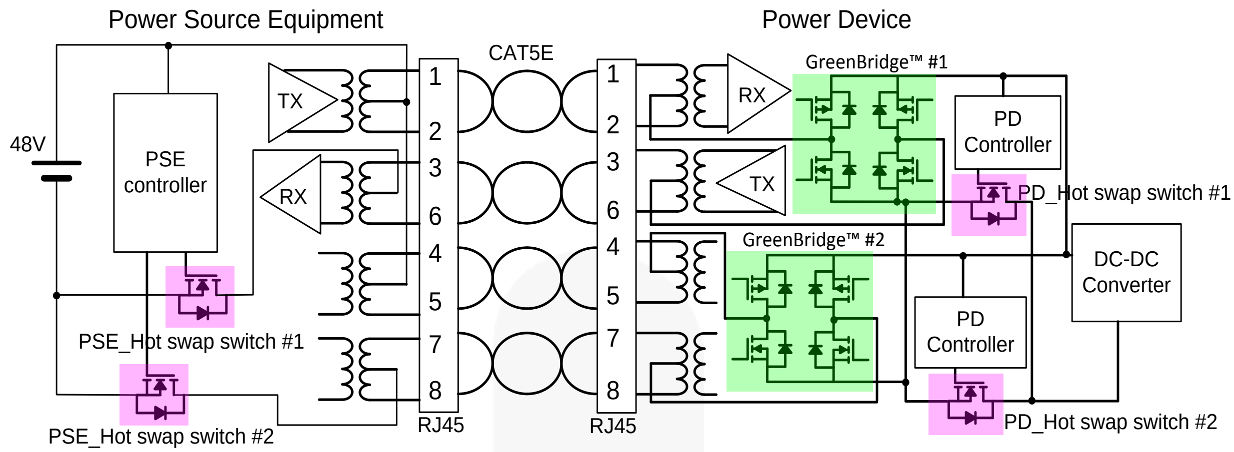


Figure 2. Four-Pair Architecture PoE System

Fairchild's GreenBridge™ solution resolves the imbalance problem of two current loops because a MOSFET has a positive temperature coefficient. If GreenBridge #1 on the current loop of 1 and 2 and 3 and 6 pins pair of RJ45 is hotter due to the imbalance current, GreenBridge #1's $R_{DS(ON)}$ increases more than GreenBridge #2 on the current loop of 4 and 5 and 7 and 8 pins pair of RJ45. It reduces the current in the GreenBridge #1 and forces more current to flow in GreenBridge #2. The other advantage of GreenBridge is reduced power loss in bridge circuits. The power dissipation of diode bridge due to the conduction loss is calculated by:

$$=2 \times V_F \times I \tag{1}$$

GreenBridge power loss is calculated by:

$$=I^2 \times R_{DS(ON)}\_Pch + I^2 \times R_{DS(ON)}\_Nch \tag{2}$$

In case of a 60 W PoE system, GreenBridge FDMQ8203 is used, which integrates dual P-channel and dual N-channel MOSFETs in a compact and thermally enhanced package. Table 2 shows the GreenBridge FDMQ8203 electrical and thermal parameters. Each power loss of FDMQ8203 and general diode bridge is calculated and compared. Minimum input voltage of the PD is 42.5 V, specified by IEEE802.3at, so the minimum input current is 1.43 A at 60 W output power and each current per bridge is 0.715 A in four pairs.

- Two GreenBridge power losses are calculated by:
  $= (0.715^2\text{A} \times 110\text{m}\Omega + 0.715^2\text{A} \times 190\text{m}\Omega) \times 2 = 0.307\text{W}$
- Two diode bridge power losses are calculated by:
  $= (0.7\text{V} \times 0.715\text{A} \times 2) \times 2 = 2.002\text{W}$

The GreenBridge FDMQ8203 saves the power loss by 1.695 W compared to a diode bridge at 60 W output power.

Table 2. GreenBridge™ FDMQ8203 Parameters

Part No.	MOSFET	B_{VDSS} (V)	$R_{DS(ON)}$ @10 V_{gs} [mΩ]	Q_g @10 V_{gs} [nC]	Θ_{JA} [°C/W]
			Max.	Typ.	
FDMQ8203	Q1, Q4	100	110	2.9	50
	Q2, Q3	-80	190	13	

The self-driven gate circuit for GreenBridge FDMQ8203 is explained in application note *AN-9759 — GreenBridge™ to Replace Conventional Diode Bridge in Power Over Ethernet Applications* on Fairchild's website.

Hot Swap Switching MOSFET

The other design point for system reliability is to select a "hot" swap switch that turns on slowly to avoid a high inrush current and voltage drop when the PSE starts to deliver power to the PD. Figure 3 explains the three modes in MOSFET operation: Ohmic, Linear, and Off. When MOSFET is Off, the drain-to-source voltage (V_{DS}) is the same as the input voltage and there is no drain–to-source current (I_{DS}). As the gate-to-source voltage (V_{GS}) increases, the MOSFET starts to flow I_{DS} and even V_{DS} maintains at the input voltage, which is called Linear Mode. During Linear Mode, the MOSFET dissipates huge power loss so the Safe Operation Area (SOA) must be checked to verify the MOSFET can withstand the thermal stress.

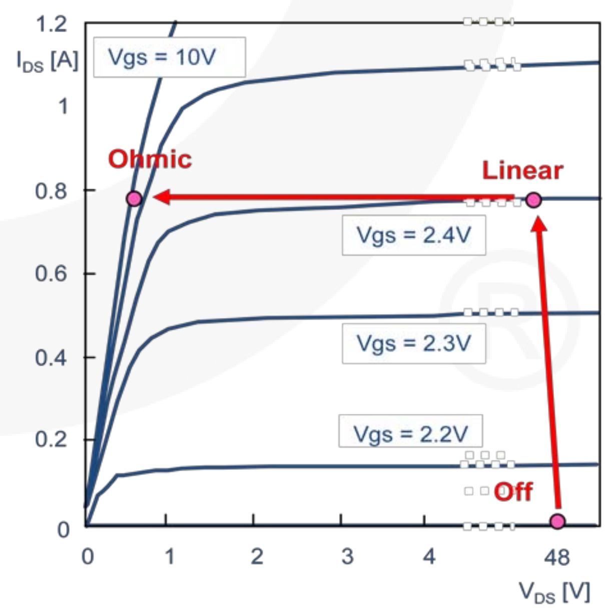


Figure 3. On Region Characteristics

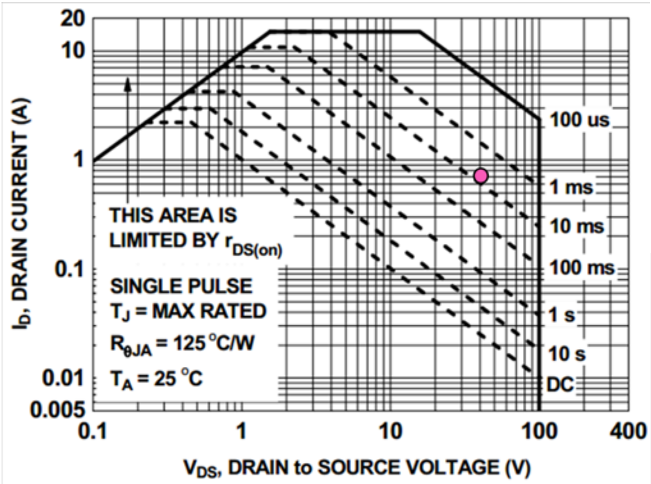


Figure 4. Forward Bias Safe Operating Area

Figure 4 is the Forward Bias Safe Operating Area (FBSOA) of the FDMC86116LZ for an example as the hot swap switch. If FDMC86116LZ with thermal impedance (θ_{JA} = 125°C/W) is switched in 730 mA of I_{DS} and 48 V of V_{DS}, as shown in Figure 3, the turn on time of FDMC86116LZ must be under 1ms.

60 W Four-Pair Architecture PoE System

Like the 60 W high-power PoE system design diagram shown in Figure 5, the PSE board delivers a maximum of 70 W power to the PD through both the spare pair and data pair of the CAT5E cable. Then the PD, using active clamp forward DC-DC topology, converts the nominal 48 V_{IN} (42 V ~ 57 V) to 12 V of the output voltage at 250 kHz of the operating frequency. Table 3 and Table 4 show the power design specification of the PSE and PD boards. Both boards are compliant with the IEEE 802.3at specification.

Table 3. PSE Power Design Specification

IEEE Standard	IEEE802.3at
PSE Output Voltage	44 ~ 57 V
Max. Source Power	70 W
Hot Swap Switch	FDMC86116LZ

Table 4. PD Power Design Specification

IEEE Standard		IEEE802.3at
PoE Class		Class 4
Bridge		GreenBridgeFDMQ8203
Input Voltage from PSE		42 ~ 57 V
DC-DC Converter	**Topology**	Active Clamp Forward DC-DC
	V_{OUT}	12 V
	Max. I_{OUT}	5 A
	Max. Power	60 W
	f_{SW}	250 kHz

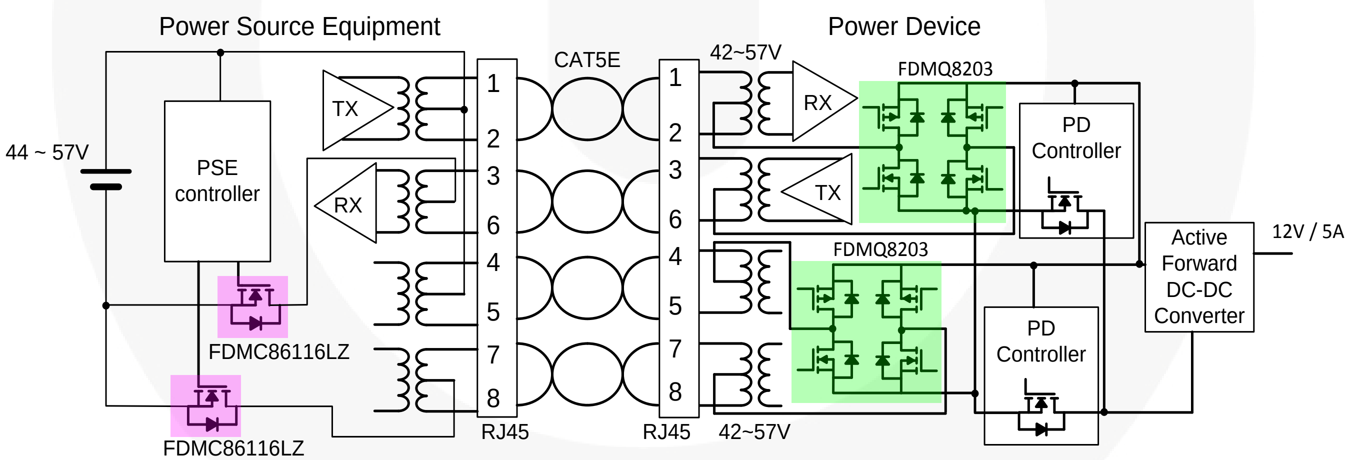


Figure 5. 60 W High-Power PoE System Design Diagram

Figure 6 shows the efficiency and power loss of the PD board. At the maximum power of 60 W, the total efficiency the PD achieves is around 91% in the PD input voltage range from 42 V to 75 V.

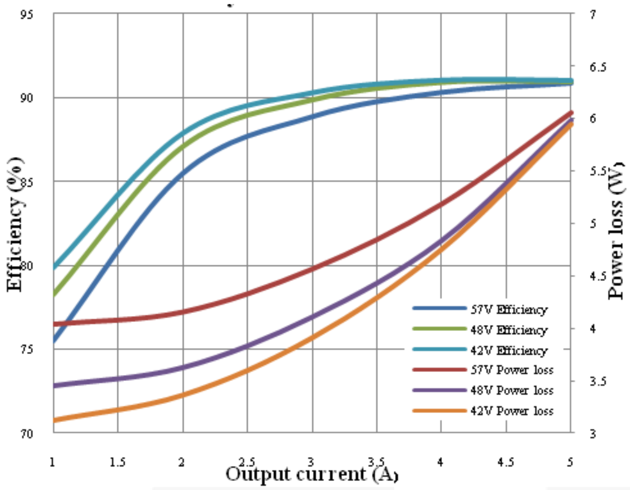
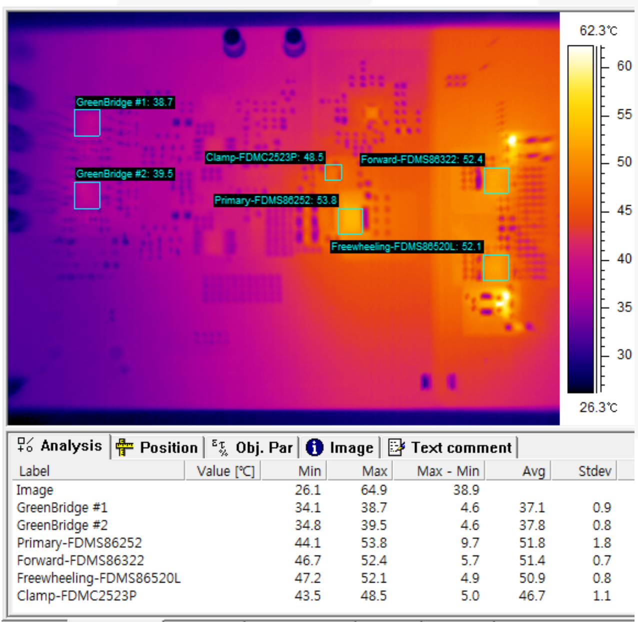


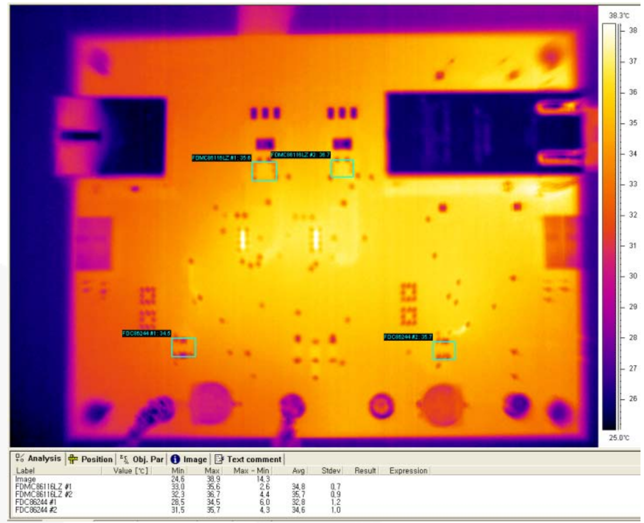
Figure 6. Efficiency & Power Loss of PD Board, T_A=25°C



Label	Value [°C]	Min	Max	Max - Min	Avg	Stdev
Image		26.1	64.9	38.9		
GreenBridge #1		34.1	38.7	4.6	37.1	0.9
GreenBridge #2		34.8	39.5	4.6	37.8	0.8
Primary-FDMS86252		44.1	53.8	9.7	51.8	1.8
Forward-FDMS86322		46.7	52.4	5.7	51.4	0.7
Freewheeling-FDMS86520L		47.2	52.1	4.9	50.9	0.8
Clamp-FDMC2523P		43.5	48.5	5.0	46.7	1.1

GreenBridge #1: 38.7°C, GreenBridge #2: 39.5°C

Figure 7. . Thermal Image of PD Board @ V_{IN}=48 V, V_{OUT}=12 V, I_{OUT}= 5 A ,T_A=25°C



Label	Value [°C]	Min	Max	Max - Min	Avg	Stdev	Result	Expression
Image		24.6	38.9	14.3				
FDMC86116LZ #1		33.0	35.6	2.6	34.8	0.7		
FDMC86116LZ #2		32.3	36.7	4.4	35.7	0.9		
FDC86244 #1		28.5	34.5	6.0	32.8	1.2		
FDC86244 #2		31.5	35.7	4.3	34.6	1.0		

FDMC86116LZ #1: 35.6°C, FDMC86116LZ #2: 36.7°C

Figure 8. Thermal Image of PSE Board @ V_{IN}=48V, P_{OUT}= 70 W, T_A=25°C

Figure 7 and Figure 8 show the thermal images of the PD and PSE board at the 60 W maximum power. The temperature difference between two GreenBridge™ and two FDMC86116LZ hot swap switches is 0.8°C and 1.1°C, respectively, which shows the well-balanced current loops at the maximum input current. Together, the GreenBridge and FDMC86116LZ hot swap switch show outstanding thermal performance.

Conclusion

The four-pair architecture design is explained for 60 W high-power PoE applications. To balance currents of two current loops and improve the power dissipation of the bridge, the GreenBridge solution is proposed. For selecting hot swap switching MOSFETs for high-power PoE applications, design considerations are discussed. With Fairchild's GreenBridge and hot swap switching MOSFET FDMC86116LZ, the 60 W PoE system achieves over 90% total efficiency.

Authors

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Edgar Kim – LV Applications Engineer

References

[1] AN-9759 GreenBridge™ to Replace Conventional Diode Bridge in Power Over Ethernet Applications

Related Resources

FDMQ8203 — GreenBridge™ Series of High-Efficiency Bridge Rectifiers Dual N-Channel and Dual P-Channel PowerTrench® MOSFET N-Channel: 100 V, 6 A, 110mΩ P-Channel: -80V, -6 A, 190mΩ

FDMC86116LZ — N-Channel PowerTrench® MOSFET N-Channel: 100 V, 7.5 A, 103mΩ

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