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## Semiconductor Consideration for DC Power Supply Voltage Protector Circuits



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### ABSTRACT

This paper addresses the requirements for the semiconductor sensing circuitry and SCR crowbar devices used in DC power supply over/under voltage protection schemes.

### INTRODUCTION

It is uncommon now to find several hundred dollars worth of microprocessors and memory chips powered from a single low DC supply.

If this supply on the board doesn't have overvoltage or undervoltage protection, potentially large sums of money can literally go up in smoke due to component failure, or, for instance, a tool may be accidentally dropped across the supply buses of different voltages during testing or repair of the system.

Since a couple of years, computer and industrial manufacturers agree to put additional small investment in Over Voltage Protection (OVP) and Over/Under Voltage Protection (OUVP) circuitry to prevent disasters.

ON Semiconductor chose the "crowbar" sensing circuit technology. This system senses the overvoltage condition, and quickly "crowbars" or short circuits the supply, forcing the supply into current limiting or opening the fuse or circuit breaker. Before detailing this technology, three questions should be considered:

1. Why OVP? To save money and increase the reliability of the system.
2. Where OVP?
  - Everywhere over/under voltage is a problem.
  - Everywhere a power supply system is used.
  - Everywhere a switchmode system is designed.
3. How OVP? There are several types of sense circuits presently being used in OVP applications. They can be classified into three types:
  - a) Zener
  - b) Discrete
  - c) MC1723 (voltage regulator in OVP configuration)

This document may contain references to devices which are no longer offered. Please contact your ON Semiconductor representative for information on possible replacement devices.

### APPLICATION NOTE

#### The Zener Sense Circuit

The simplest way to protect against overvoltage is to use a Zener diode to sense the output voltage (Figure 1). When the Zener goes into avalanche, it triggers the SCR.

There are problems with this kind of protection:

1. No threshold adjustment, except by selecting different Zener diodes.
2. Inability to ignore momentary transients.
3. Poor SCR reliability caused by inadequate trigger-current rise time when slowly varying voltage is sensed.

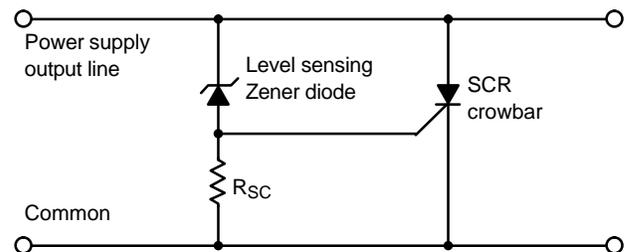


Figure 1.

#### The Discrete Sense Circuit

A technique which can provide adequate gate drive and an adjustable, low temperature coefficient trip point is shown in Figure 2.

This circuit includes the Zener reference voltage (Z1), the comparator section (Q1, Q2), band gap circuit (Q3, Q4), potentiometer (R1), trip point, and output section (Q5, R2, R3, D1).

While overcoming the problems of the Zener sense circuit, this technique also brings many disadvantages:

1. This technique requires many components (12 here).
2. Cost is very high.
3. This method is not particularly noise immune and often suffers from nuisance tripping.

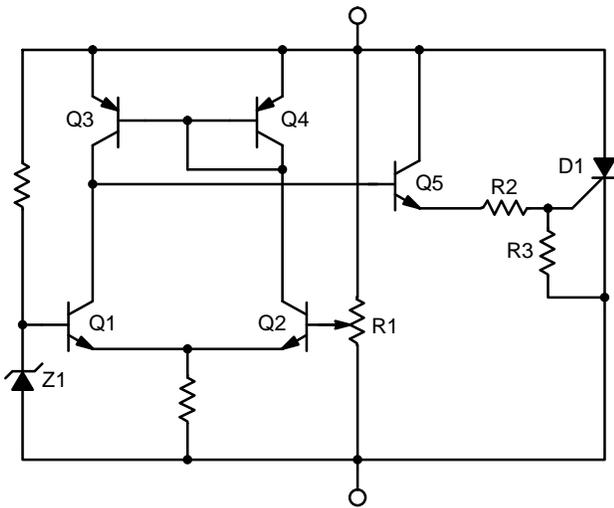


Figure 2.

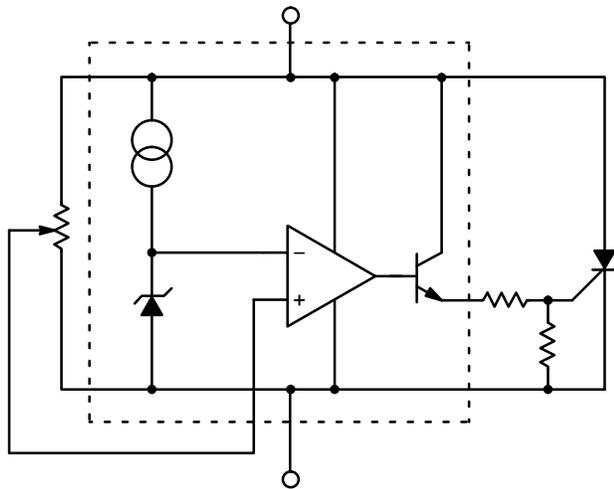


Figure 3.

**The MC1723 Sense Circuit**

A simpler approach is to fire the SCR crowbar with an MC1723 voltage regulator.

A considerable reduction in component count is done (see Figure 3). The main disadvantages are:

1. No noise immunity.
2. The minimum input voltage range is 9.5 V, so you are restricted to use it for higher voltages or to supplement it by feeding in an auxiliary supply voltage.

**THE SCR CHOICE**

The use of the SCR crowbar overvoltage protection circuits in DC power supplies has been, for many years, a popular method of providing protection to the load from accidental overvoltage stresses. This technique and its proper implementation have become increasingly important in light of the recent advances in LSI made by the semiconductor industry.

Referring to Figures 4 and 5, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance,  $C_{OUT}$ . This surge current is illustrated in Figure 6 and can cause SCR failure or degradation by any one of three mechanisms:  $di/dt$ , absolute peak surge, or  $I^2t$ . The interrelationship of these failure methods and the breadth of the application make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's  $di/dt$  and surge capabilities simplifies this task.

**$di/dt$**

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned-on gate region, very high current densities can occur in the gate region if high anode currents appear quickly ( $di/dt$ ). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities – depending on the severity of the occasion.

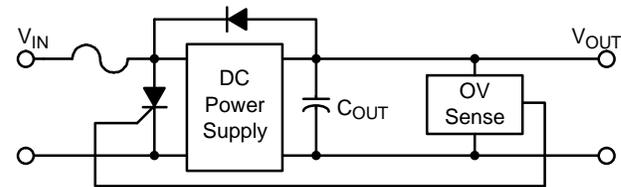


Figure 4.

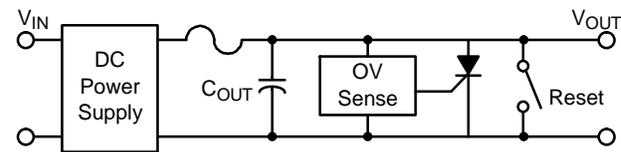


Figure 5.

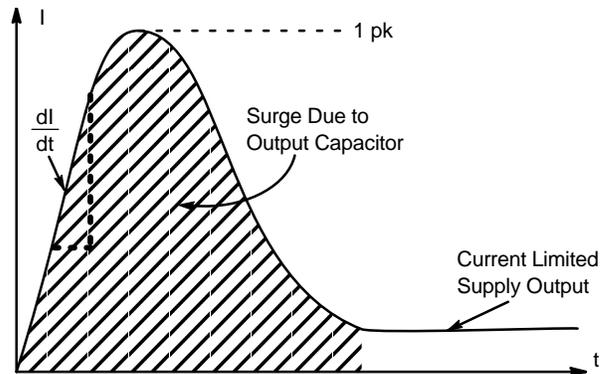


Figure 6.

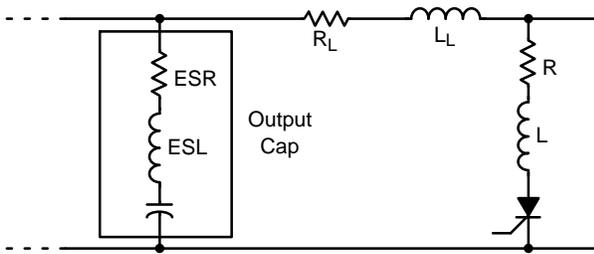


Figure 7.

C<sub>OUT</sub> consists of the power supply output caps, the load's decoupling caps, and in the case of Figure 4, the supply's input filter caps.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center-gate-fire SCR has more di/dt capability than a corner-gate-fire type and heavily overdriving (3 to 5 times I<sub>GT</sub>) the SCR gate with a fast (< 1 μs) rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 Arms rating might be 200 A/μs, assuming a gate current of five times I<sub>GT</sub> and < 1 μs rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 7. Of course, this reduces the circuit's ability to rapidly reduce the DC bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

**Surge Current**

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance – see Figure 7) to a safe

level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the DC power supply.

**OVERVOLTAGE PROTECTOR: THE MC3423**

To fill the need for a low cost, low complexity method or implementing crowbar overvoltage protection which does not suffer the disadvantages of previous techniques, ON Semiconductor has developed the MC3423 and its military range version, the MC3523.

This circuit was designed to provide output currents of up to 300 mA with a 400 mA/μs rise time in order to maximize the di/dt capabilities of the crowbar SCR. In addition, its main features include:

- Operation off 4.5 V to 36 V supply voltages
- Adjustable, low temperature coefficient trip point
- Adjustable minimum overvoltage duration before actuation (0.5 μs to 1.0 ms) to reduce nuisance tripping in noisy environments
- Remote activation input
- Activation indication output
- Output short circuit protected for V<sub>CC</sub> ≤ 10 V

**The Block Diagram**

The block diagram of the MC3423 is shown in Figure 8. It consists of a stable 2.6 V reference, two comparators and a high current output.

This output, together with the indication output transistor, is activated either by a voltage greater than 2.6 V on pin 3 or by a TTL/5 V CMOS high logic level on the remote activation input, pin 5.

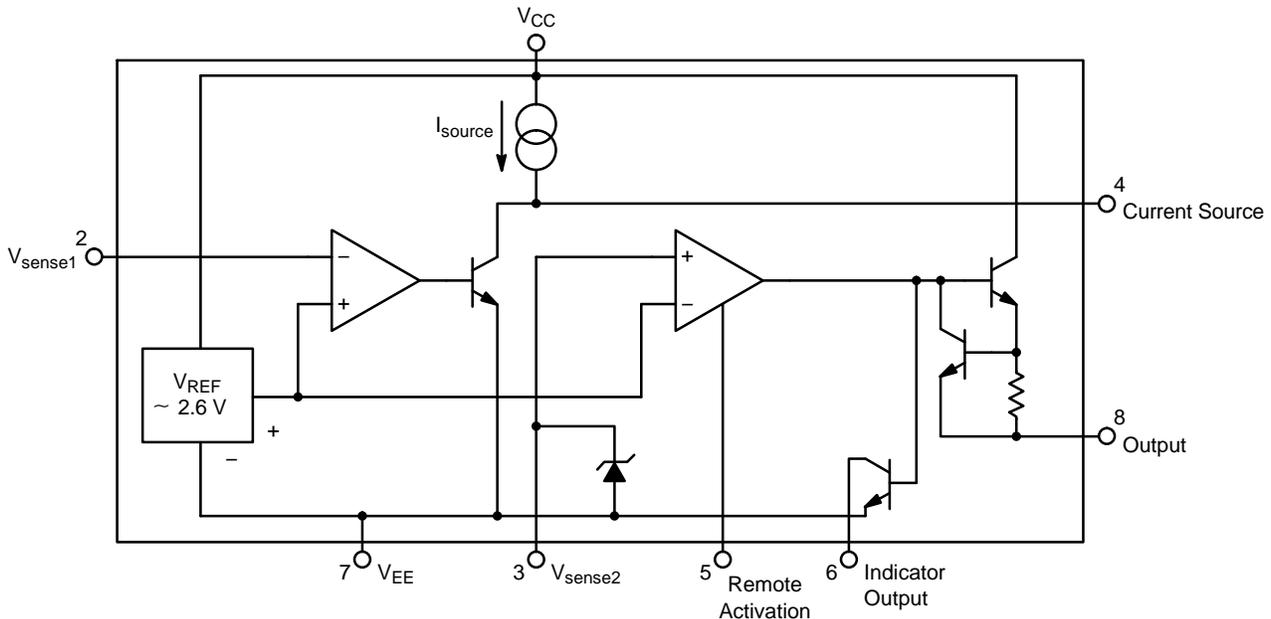


Figure 8.

The first comparator is designed to initiate a stable time delay and the second one activates both a crowbar firing current and a low level indication signal.

**The Basic Circuit**

The basic circuit configuration of the OVP is shown in Figure 9. In this circuit, the voltage sensing inputs of both the internal amplifiers are tied together for sensing the overvoltage condition. The shortest possible propagation delay is thus obtained.

The threshold on trip voltage at which the MC3423 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R1 and R2. Their values can be determined by the Equation 1:

$$V_{trip} = V_{REF} \left( 1 + \frac{R1}{R2} \right) = 2.6 V \left( 1 + \frac{R1}{R2} \right) \quad (eq. 1)$$

$R2 \leq k\Omega$  for minimum drift.

Figure 10 shows (with  $R2 = 2.7 k\Omega$ ) the value (min, typ, max) of R1 versus trip voltage.

The switch S1, shown in Figure 9, may be used to reset the SCR crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non-current-limited supply is used, a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

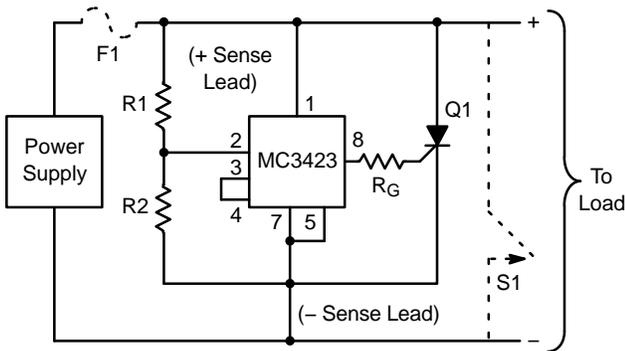


Figure 9.

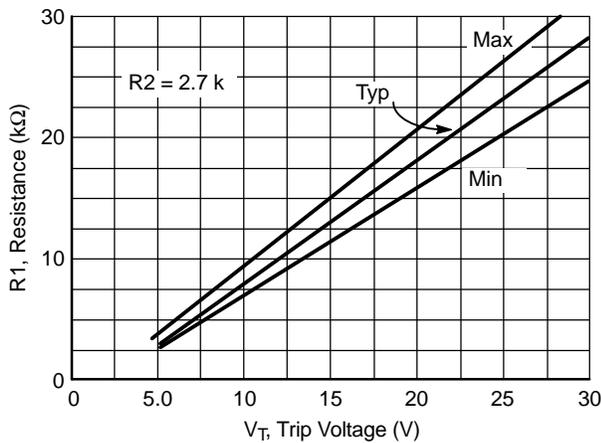


Figure 10.

The minimum value of the gate current limiting resistor,  $R_G$ , is given in Figure 11. Using this value of  $R_G$  the SCR Q1 will receive the greatest gate current possible without damaging the MC3423. If lower output currents are required,  $R_G$  can be increased in value.

**THE PROGRAMMATION**

**Low Voltage < 36 V**

In many instances, the MC3423 will be used in a noise environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load, the MC3423 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 12 is used. In this configuration, a capacitor is connected from pin 3 to  $V_{EE}$ . The value of this capacitor determines the minimum duration of the overvoltage condition which is necessary to trip the OVP. The value of C can be found from Figure 13. The circuit operates in the following manner: when  $V_{CC}$  rises above the trip point set by R1 and R2, an internal current source (pin 4) begins charging the capacitor, C, connected to pin 3. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate  $\approx 10$  times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

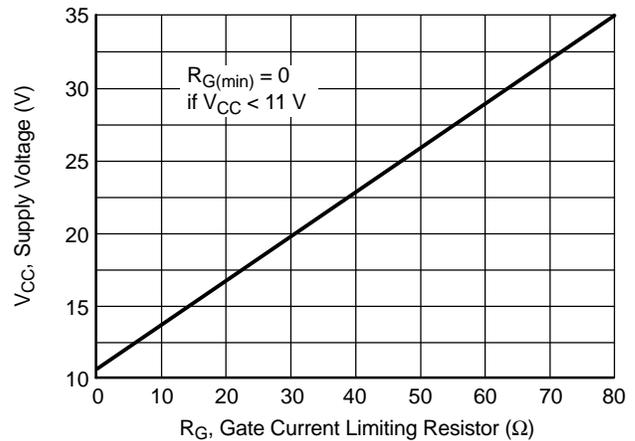


Figure 11.

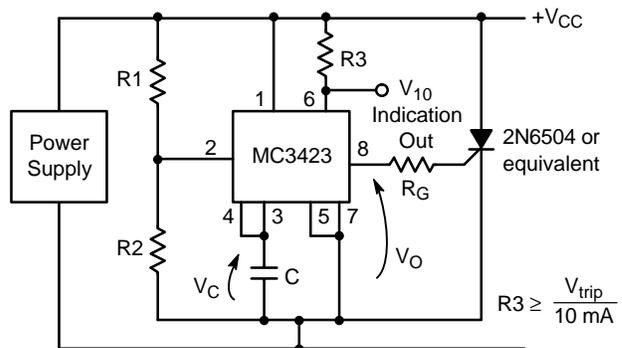


Figure 12.

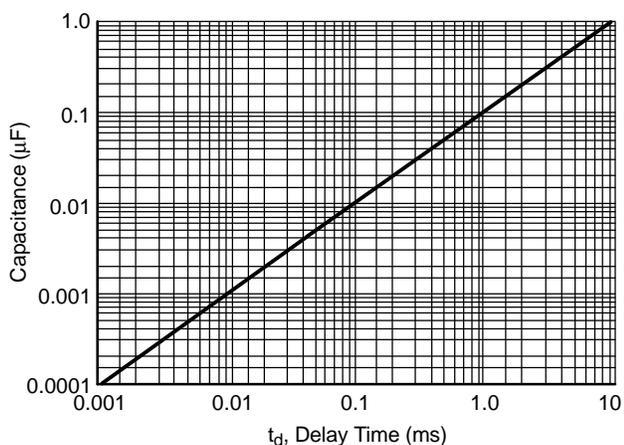


Figure 13.

Occasionally, it is desired that immediate crowbarbing of the supply occurs when a high overvoltage condition occurs, while retaining the false tripping immunity of Figure 12.

#### High Voltage $36\text{ V} < V < 800\text{ V}$

Figure 14 is a typical application for voltage protection over 36 V, using a Zener diode 1N4740 (10 V) and a 10 µF (15 V) capacitor at the positive sense lead.

The value of  $R_S$  can be calculated with the following formula:

$$R_S = \frac{(V_S - 10)}{25} \text{ k}\Omega \quad (\text{eq. 2})$$

The  $V$  trip is given by the Equation 1.

Following the choice of the SCR (Q1), the protection can be done up to 800 V:

- $V_S \leq 50\text{ V}$ : 2N6504 or equivalent
- $V_S \leq 100\text{ V}$ : 2N6505 or equivalent
- $V_S \leq 200\text{ V}$ : 2N6506 or equivalent
- $V_S \leq 400\text{ V}$ : 2N6507 or equivalent
- $V_S \leq 600\text{ V}$ : 2N6508 or equivalent
- $V_S \leq 800\text{ V}$ : 2N6509 or equivalent

On this configuration (Figure 14) the typical propagation delay is 1.0 µs. If faster operation is desired, pin 3 may be connected to pin 2 with pin 4 left floating. This will result in decreasing the propagation delay to approximately 0.5 µs at the expense of a slightly increased  $T_C$  for the trip voltage value.

## THE ADDITIONAL FEATURES

### Activation Indication Output

An additional output for use as an indication of OVP activation is provided by the MC3423. This output is an open collector transistor which saturates when the OVP is activated. It will remain in a saturated state until the SCR crowbar pulls the supply voltage,  $V_{CC}$ , below 4.5 V as in Figures 12 and 15. This output can be used to clock an edge triggered flip-flop whose output inhibits or shuts down the

power supply when the OVP trips. This reduces or eliminates the heat-sinking requirements for the crowbar SCR.

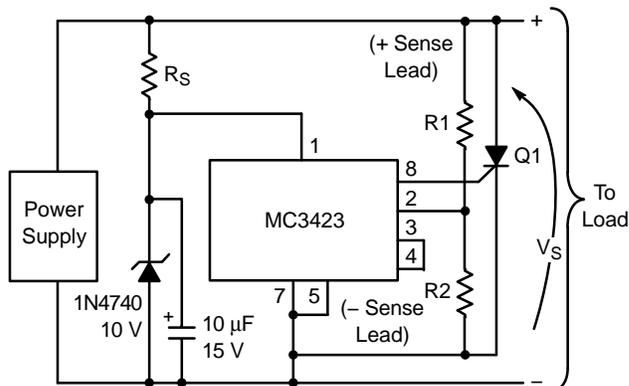


Figure 14.

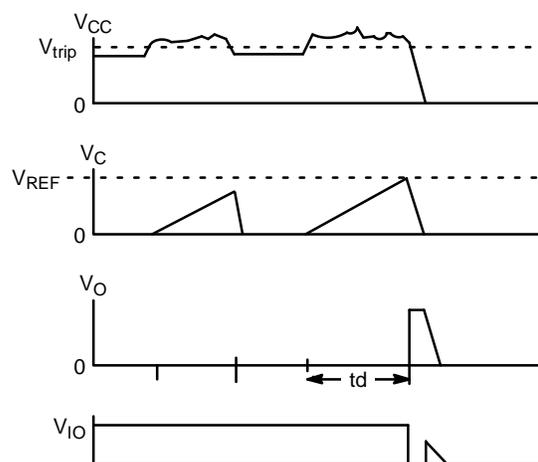


Figure 15.

Using Figure 13 (C value) and Figure 15,  $t_d$  is equal to:

$$t_d = \frac{V_{REF}}{I_{source}} \times C = (12.10^3) \cdot C \quad (\text{eq. 3})$$

### Remote Activation Input

Another feature of the MC3423 is its remote activation input, pin 5. If the voltage on this CMOS/TTL compatible input is held below 0.8 V, the MC3423 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present. It should be noted that pin 5 has an internal pull-up current source. This feature can be used to accomplish an orderly and sequenced shut-down of system power supplies during a system fault condition. In addition, the activation indication output of one MC3423 can be used to activate another MC3423 if a single transistor inverter is used to interface the former's indication output to the latter's remote activation input, as shown in Figure 16. In this circuit, the indication output (pin 6) of the MC3423 on power supply 1 is used to activate the MC3423 associated with power supply 2. Q1 is any small PNP with adequate voltage rating.

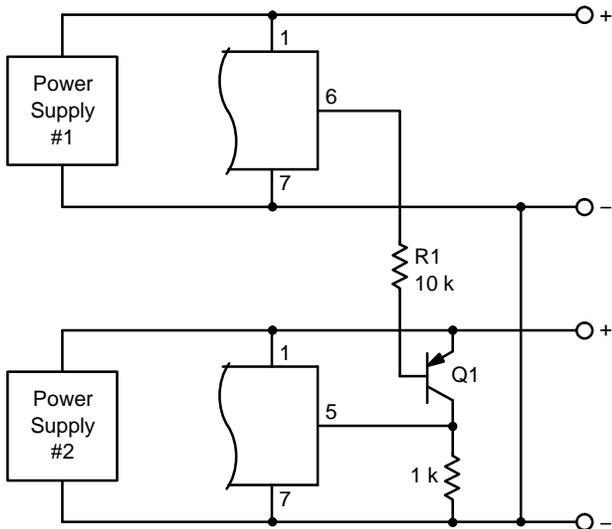


Figure 16.

Note that both supplies have their negative output leads tied together (i.e., both are positive supplies). If their positive leads are common (two negative supplies), the emitter of Q1 would be moved to the positive lead of supply 1 and R1 would therefore have to be resized to deliver the appropriate drive to Q1.

**A Word About Fuse Protector**

Referring back to Figures 4 and 5, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an  $I^2t$  rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents.

In addition, it must be capable of successfully cleaning the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

**WHAT ABOUT OVER AND UNDERVOLTAGE PROTECTION**

Two types of circuits have been developed: MC3424 and MC3425, and their military temperature range series MC3524 and MC3525. Like the MC3423, these circuits were primarily intended for use as voltage protection circuits. Basically the MC3424 and MC3425 also use the “crowbar sensing circuit technology” and the block diagrams (Figures 17 and 18) seems to the MC3423.

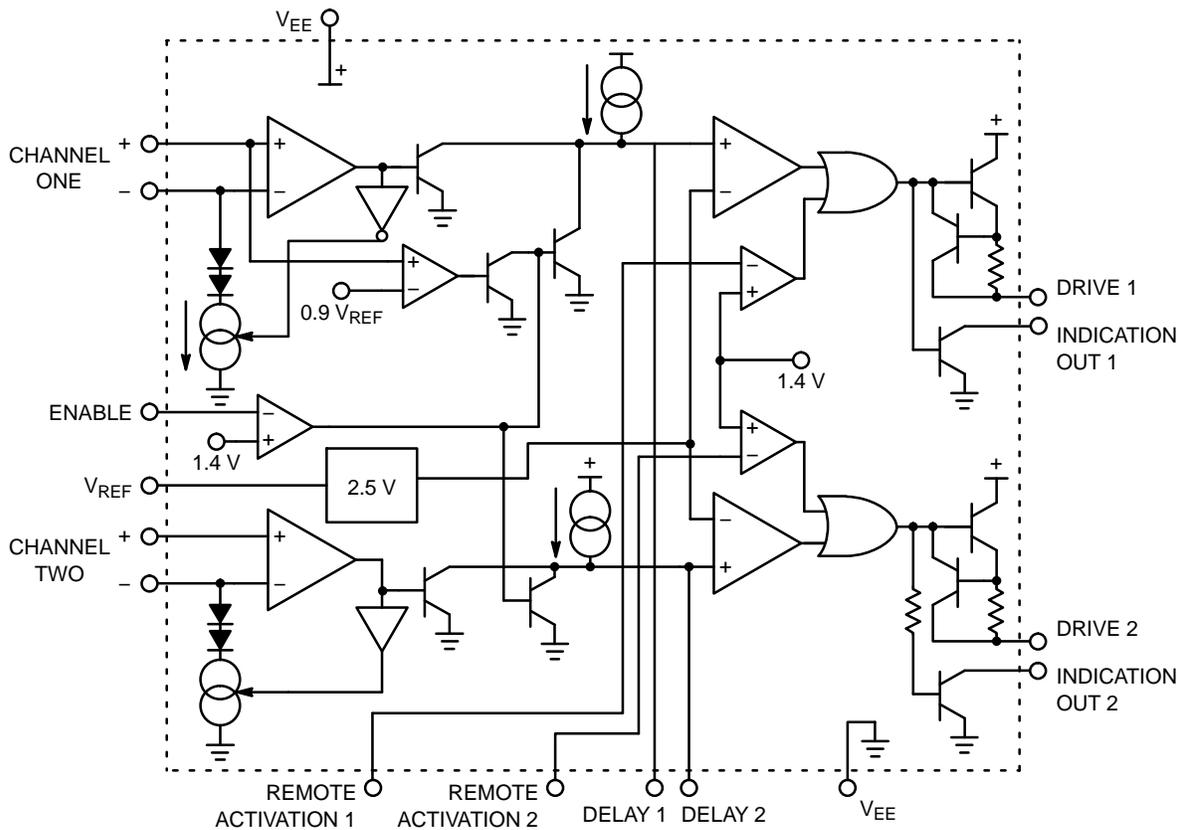


Figure 17. MC3424/MC3524 Equivalent Circuit

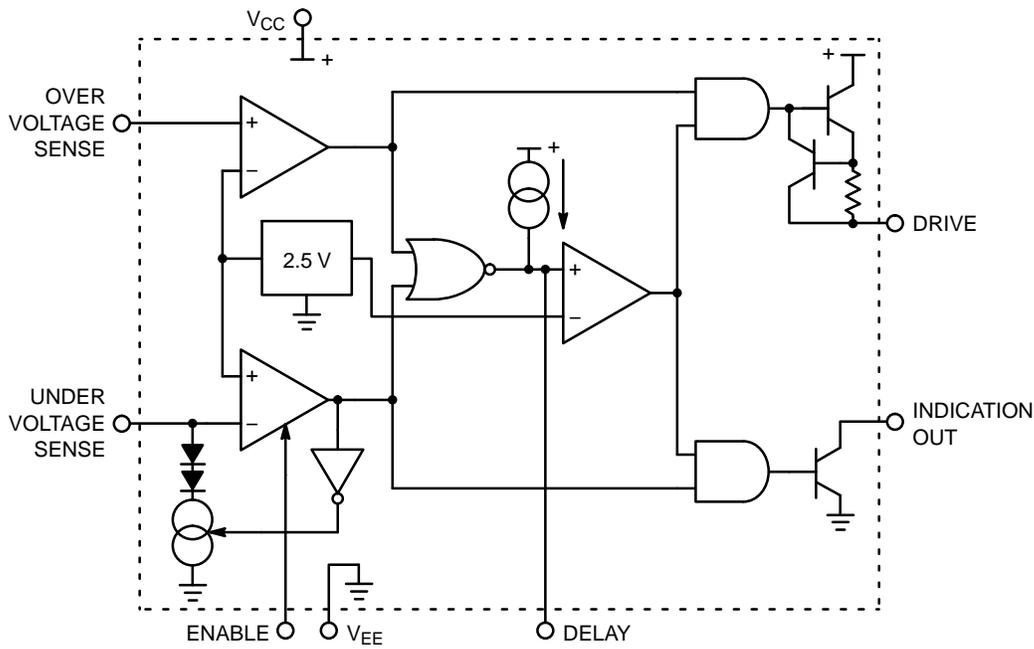


Figure 18. MC3425/MC3525 Equivalent Circuit

A look at Figure 17 (MC3424) shows two channels of uncommitted differential inputs with a common mode range from ground ( $V_{EE}$ ) to  $V_{CC+}$ , for maximum flexibility. This circuit has an externally programmable hysteresis. However, the output is very stable ( $T_C < 0.01\%/^{\circ}C$ ), due mainly to its band gap reference voltage circuit: 2.5 V at 10 mA.

The two independent drive outputs are capable of sourcing 300 mA at a slew rate of 200 to 400 mA/ $\mu$ s.

The two indicators are capable of sinking 300 mA.

The enable input (CMOS, TTL, DTL compatible) control of either channel 2 or both channels depending on channel 1 input conditions.

Each channel can be operated closed loop with gain or unity gain, stabilized at the delay pin.

Figure 18 (MC3425) shows a low cost OUVP version: 8 pins dual in line instead of 14 pins for the MC3424.

A typical application is shown in Figure 19. Following the trip voltage required, the value of resistors  $R_S$  and  $R_B$  will be selected following the formula (see Equation 1):

$$V_{trip} = V_{REF} \left( 1 + \frac{R_S}{R_B} \right) = 2.6 V \left( 1 + \frac{R_S}{R_B} \right) \quad (eq. 4)$$

To prevent a minimum drift of the circuit,  $R_B$  value should be around 10 k $\Omega$  and  $R_E$  and  $C_D$  are calculated by the following equations:

$$R_E = \frac{T}{C_{E} L_n \left( \frac{V_S}{V_S - V_E} \right)} \quad (eq. 5)$$

$$C_D = \frac{I_s T_d}{V_{REF}} = \frac{200 \mu A T_d}{2.5 V} \quad (eq. 6)$$

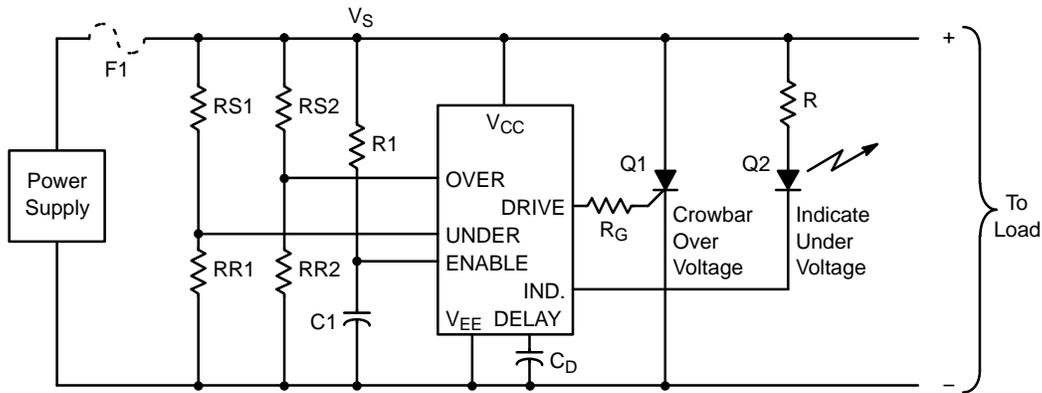


Figure 19.

## CONCLUSION

The use of a crowbar to protect sensitive loads from power supply overvoltage is quite common and, at the first glance, the design of these crowbars seems like a straight forward relatively simple task:

- How much overvoltage and for how long (energy) can the load take this overvoltage?
- Will the crowbar respond too slowly and thus not protect the load, or too fast resulting in false, nuisance triggering?
- How much energy can the crowbar thyristor (SCR) take and will it survive until the fuse opens the circuit breaker opens?
- Can the fuse adequately differentiate between normal current levels, including surge currents, and crowbar short circuit conditions?

All the users are involved with these problems; it is the attempt of this article to answer these questions.

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