Understanding eFuse Input Voltage Transients from Hot Plug Events

How to Determine if an eFuse System Can be Safely Hot−Plugged

AND90059/D

INTRODUCTION

System designers must account for voltage surges that occur when supplies or loads are connected. eFuses are integrated circuits with many features to protect loads from these surges. However, it is important to ensure that the eFuse itself will not receive excessive voltage on its input. This application note uses mathematical calculations, simulations, and actual lab data to illustrate the voltage surge as an eFuse is suddenly connected on the input side. System designers can use this information to make certain that the eFuse will be within its limits.

Basic System Layout

The maximum input voltage of an eFuse is always specified on the datasheet. An eFuse may not be damaged by a voltage above the maximum specified on the datasheet, but it could be dangerous depending on the circumstances. Figure 1 helps visualize the issue. During a hot plug on the input, the voltage may enter either the blue or red zone depending on variables. These variables include:

- DC supply voltage level
- Maximum eFuse input voltage
- Resistance, inductance, and capacitance (RLC) values
- Presence of a protection device like a Zener diode

A diagram of a system where these voltage levels can appear is shown in Figure 2. There is a detachable cable between the DC voltage supply and the eFuse that allows a user to quickly switch supplies or circuit boards. Any circuitry downstream of the eFuse (i.e. on the output side) will be protected by the eFuse and its protection features during the input hot plug. The system diagram can be broken down into an electrical schematic with R, L, and C components for analysis.

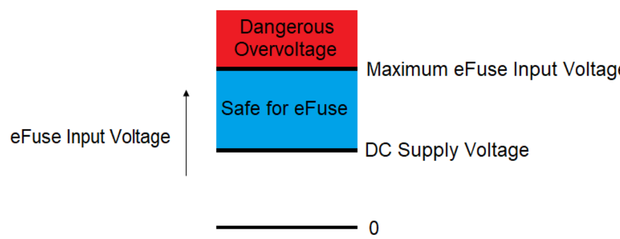

Figure 1. Important Voltage Levels in a System with an eFuse

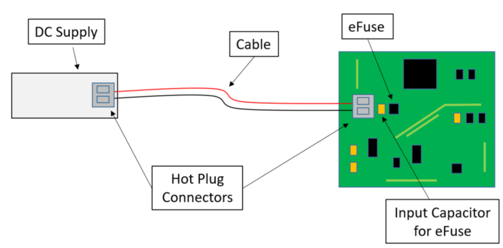

Figure 2. System Diagram

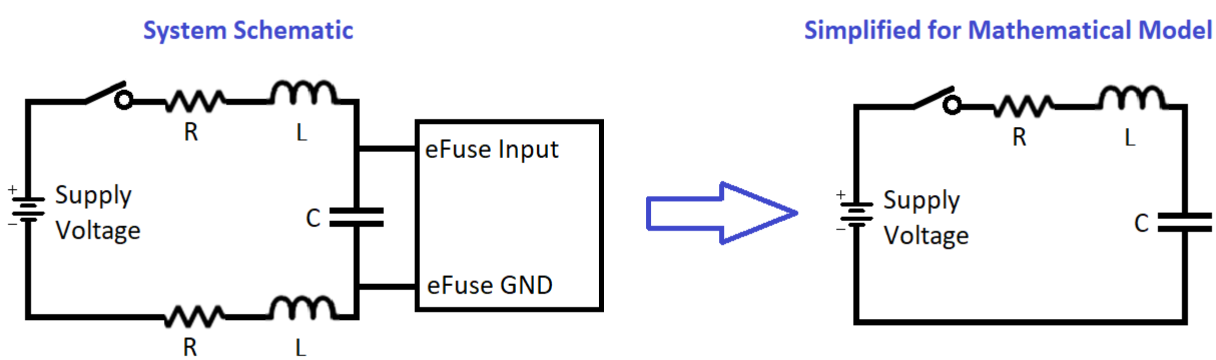

Figure 3. The System Schematic is Converted to a Simplified Series RLC Circuit since the eFuse can be Considered High Impedance. Also since the Positive and GND Return Cables are in Series they can be Lumped Together

August, 2021 − Rev. 1
Publication Order Number:
AND90059/D

Calculations and Spreadsheet Tool

The electrical schematic with R, L, and C components and a DC supply is shown on the left side of Figure 3. The voltage across the capacitor is the voltage that will appear at the input of the eFuse. A simplified model is shown on the right side of Figure 3. To generate the simplified model, the series components are lumped together, the eFuse output voltage is ignored (the eFuse has a delay circuit to keep the output disconnected during the hot plug), and the very small (< 1 mA) eFuse input to GND bias current that powers the eFuse's controller is ignored.

The equation that describes the voltage across the capacitor in this circuit is:

$$\upsilon_c(t) = V_{supply} - (V_{supply})\left[\exp(\sigma t)\left(\cos(\omega_d t) - \frac{\sigma}{\omega_d}\sin(\omega_d t)\right)\right]$$

$$\sigma = \frac{-R}{2L}, \; \omega_d = \sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}$$

A mathematical model was created. This can be done with software such as Microsoft Excel or MATLAB. The following case was tested:

DC Supply (V)	R (Ω)	L (H)	C (F)
30	0.1	5E−07	1E−06

Figure 4 shows the capacitor voltage vs. time. Although the DC supply voltage was only 30 V, the peak capacitor voltage was 54 V.

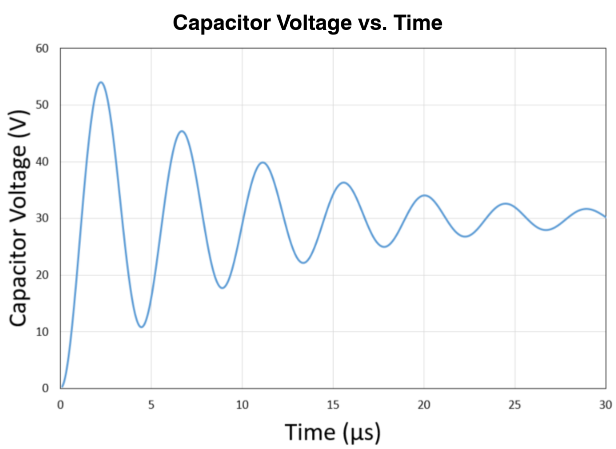

Figure 4. Result from Mathematical Model

Simulations

Simulation software can be used to model the waveform. The schematic is shown below in Figure 5.

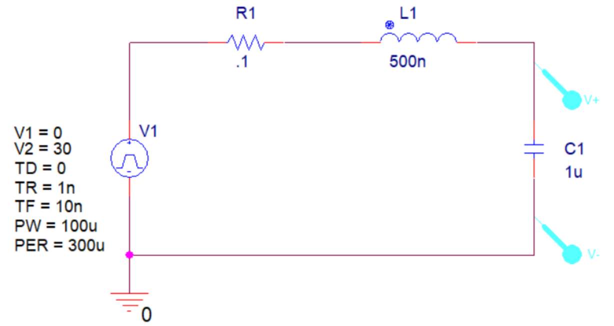

Figure 5. Simulation Schematic

The result in Figure 6 can be compared to that from the mathematical model in Figure 4. Note that the $V_C(t)$ response is almost identical between the mathematical model and the simulation.

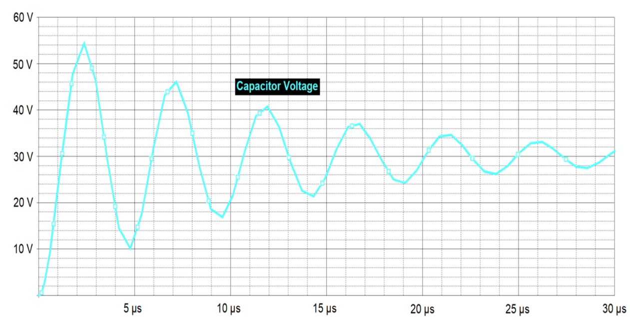

Figure 6. Simulation Result

Lab Measurements

A lab measurement was taken to corroborate the mathematical model and simulation results. A 12", 18 gauge banana cable was used. The inductance and resistance of the combination of the power supply and cable were 500 nH and 120 mΩ. There were some additional parasitics in the capacitor that were not measured, but the values were considered close enough for corroboration to the results presented from the mathematical model and simulations in Figures 4 and 6. The capacitor was a 1 µF, 50 V ceramic type (part number: FK20X7R1H105K by TDK Corporation). The power supply was an Extech 382275. The power supply's internal output capacitance near the terminals is very large (more than 800 µF), which is a nearly ideal DC supply.

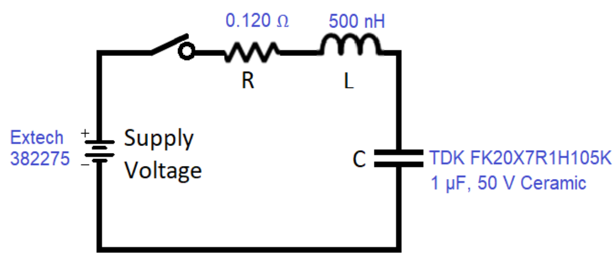

Figure 7. Lab Measurement Circuit

The peak voltage and oscillation frequency showed a close match to the mathematical result in Figure 4 and the simulation result in Figure 6.

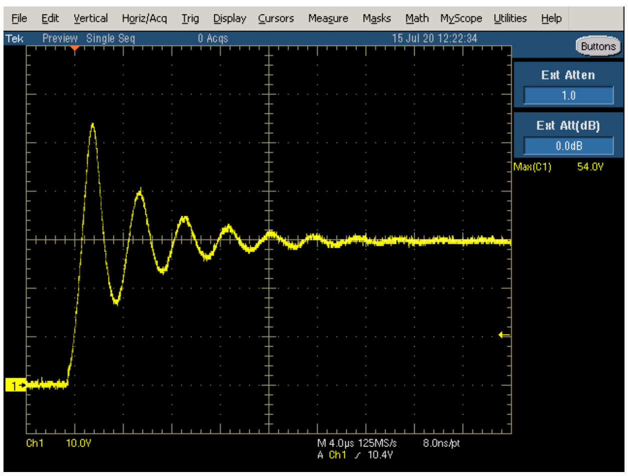

Figure 8. Lab Measurement Hot Plugging into a 1 μF Capacitor Only (no eFuse)

Next, an eFuse was connected to check if the presence of the eFuse would change the $V_C(t)$ waveform. An NIS5420 eFuse was connected in parallel with the capacitor. Comparing Figures 8 and 9, the results are indistinguishable and it is clear that the eFuse does not change the $V_C(t)$ result.

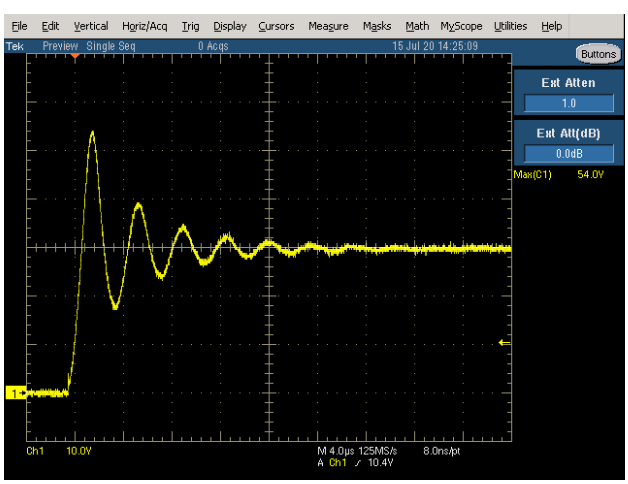

Figure 9. Lab Measurement with 1 μF Capacitor and an NIS5420 eFuse Connected in Parallel

Additional Test Cases

Several other RLC combinations were tested using the mathematical model and simulations and the results are shown in the Table 1 below. % Surge is the additional voltage above the supply voltage that appears across the capacitor. Note that the max capacitor voltage (Max Vc) is never more than twice the supply voltage.

Table 1. ADDITIONAL TEST CASES

Case	DC Voltage (V)	R (Ω)	L (H)	C (F)	Max Vc (V)	% Surge	Peak Current (A)
1	30	0.1	5.00E-07	1.00E-06	54	80	38
2	30	0.1	5.00E-07	1.00E-05	45	50	99
3	30	0.1	5.00E-07	1.00E-04	31	3	193
4	30	0.1	2.00E-06	1.00E-06	57	90	20
5	30	0.1	2.00E-06	1.00E-05	51	70	57
6	30	0.1	2.00E-06	1.00E-04	39	30	134
7	30	0.1	5.00E-06	1.00E-06	58	93	13
8	30	0.1	5.00E-06	1.00E-05	54	80	38
9	30	0.1	5.00E-06	1.00E-04	43	43	98
10	30	0.3	5.00E-07	1.00E-06	45	50	32
11	30	0.3	5.00E-07	1.00E-05	32	7	63
12	30	0.3	5.00E-07	1.00E-04	30	0	88
13	30	0.3	2.00E-06	1.00E-06	51	70	18
14	30	0.3	2.00E-06	1.00E-05	40	33	43
15	30	0.3	2.00E-06	1.00E-04	30	0	75
16	30	0.3	5.00E-06	1.00E-06	54	80	12
17	30	0.3	5.00E-06	1.00E-05	45	50	32
18	30	0.3	5.00E-06	1.00E-04	30	0	63
19	30	0.5	5.00E-07	1.00E-06	39	30	27
20	30	0.5	5.00E-07	1.00E-05	30	0	46
21	30	0.5	5.00E-07	1.00E-04	30	0	56
22	30	0.5	2.00E-06	1.00E-06	47	57	17
23	30	0.5	2.00E-06	1.00E-05	34	13	35
24	30	0.5	2.00E-06	1.00E-04	30	0	52
25	30	0.5	5.00E-06	1.00E-06	51	70	11
26	30	0.5	5.00E-06	1.00E-05	39	30	27
27	30	0.5	5.00E-06	1.00E-04	30	0	46

Max capacitor voltage (Vc) was plotted individually against R, L, and C. Figures 10–12 correspond to parameters of Table 1. These figures show that larger voltage surges correspond to lower resistance, lower capacitance, and higher inductance.

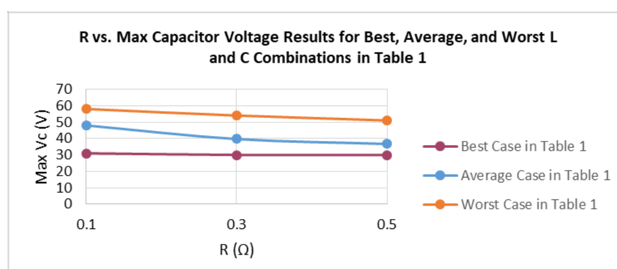

Figure 10. R vs. Average Max Capacitor Voltage

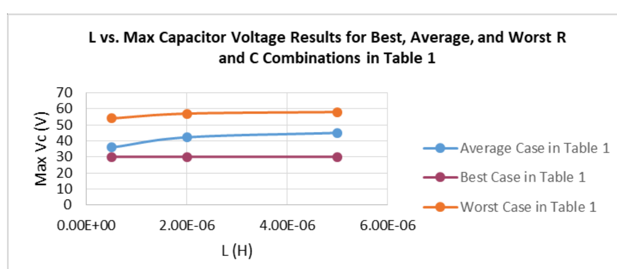

Figure 11. L vs. Average Max Capacitor Voltage

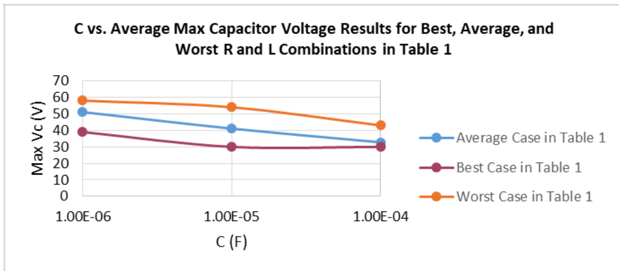

Figure 12. C vs. Average Max Capacitor Voltage

Inrush current can also be a consideration. The peak inrush current can be obtained simply by using the i = C*dv/dt equation. Although higher capacitance helps suppress the voltage, it will draw additional inrush current. For example, in Table 1, with the large 100 μF capacitor the inrush current ranged from 46 to 193 A depending on the R and L values.

One way to lower the voltage spike without increasing the inrush current is to use an external Zener diode. A test was done with a 33 volt zener (part number: MMBZ5257B by **onsemi**) using the same bench test setup.

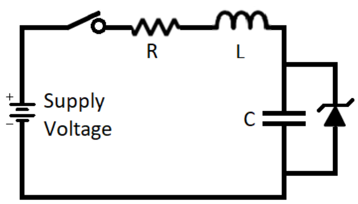

Figure 13. Addition of Zener Diode

Although the nominal value of the Zener was 33 V, the peak voltage reached 48 V because of the resistive nature of the Zener when there is high current.

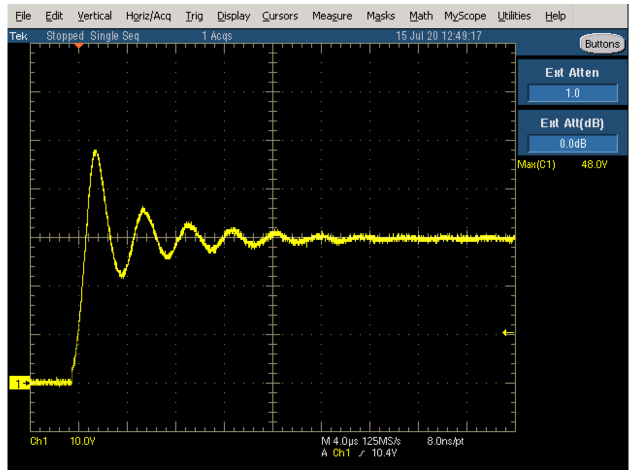

Figure 14. Voltage Spike was Reduced from 54 to 48 V with the Addition of the 33 V Zener Diode

Summary

During a hot plug event on the input, the eFuse input voltage may reach a level that is twice the DC supply voltage. A larger capacitor or Zener diode at the input can help keep the eFuse input voltage at a safe level.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800-282-9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative