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Long Integration Timing for Interline CCD Image Sensors

Introduction

This note describes the voltage and timing recommendations for the best performance of Interline CCDs in long-integration applications. It will result in the lowest level of dark current, point defects, amplifier glow, and power consumption. The following recommendations apply to the KAI-0340, KAI-2001, KAI-2020, KAI-2093, KAI-4011, KAI-4021, KAI-04022, and KAI-11002 Image Sensors.

Recommendations

During a long integration, the vertical CCD (VCCD) clocks should be stopped in the low state (-9 V). Clocking the VCCD during integration will increase the amount of dark current collected in the photodiodes. In addition, clocking the VCCD will cause some photodiodes to collect significantly more dark current than others, which will create bright point defects.

It is a common belief that the VCCD must be clocked to prevent the VCCD from over-filling with dark current during the integration. This is not true. When both phases (V1 and V2) of the VCCD are held at -9 V, the dark current generation rate in the VCCD will be less than the dark current generation rate of the photodiodes. Hence, the VCCD will not fill up with dark current before the photodiodes.

At the beginning of integration, set V1 and V2 to -9 V and then pulse the electronic shutter once to clear the photodiodes. The falling edge of the electronic shutter pulse will mark the beginning of the integration time. The output

APPLICATION NOTE

amplifier supply, VDD, should be set to zero volts to eliminate glowing of the output amplifier. The horizontal CCD (H1S, H2S, H1B and H2B) and reset clocks may also be stopped in the high level state. In some cameras the electronics design will not allow the HCCD clocks or reset clock to be stopped high. In this case they may also be stopped in the low level state, but the high level will give the best results. RD, OG, VSUB, and ESD should remain unchanged. With these settings the image sensor will consume no power.

Before transferring charge from the photodiodes to the VCCD, what little dark current that has collected in the VCCD should be swept out. This is best done with the same timing used to read out the image, in both speed and number of transfers (at least 1214 lines for the KAI-2001). If the VCCD is emptied using the fast dump gate and clocking the VCCD faster than the normal line rate, the VCCD will contain an uneven level of dark current. The uneven dark current will confuse many dark level subtraction circuits. After emptying the VCCD, turn VDD back on. In the case of the KAI-0340, VDD must be turned on for the emptying of the VCCD since the reset drain voltage is generated from VDD on this particular device. Once the VCCD has been cleared, begin normal image readout with the frame timing. This sequence is shown in the timing diagram below.

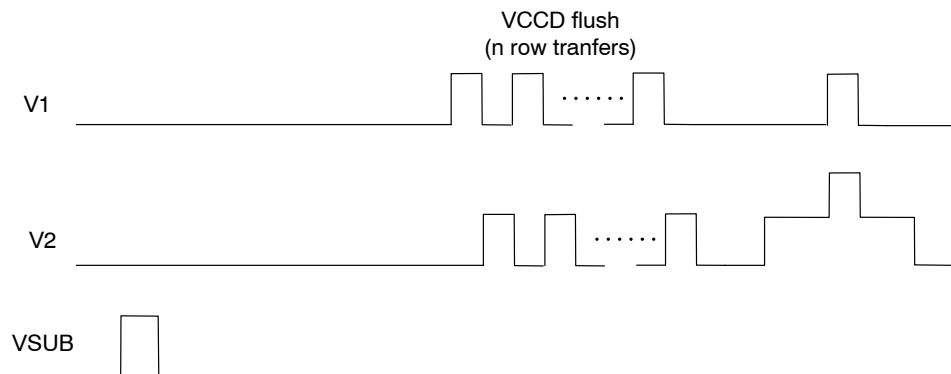



Figure 1. Sample Timing Diagram

AND9186/D

If the camera is sitting idle for a long period of time without taking pictures, the VCCD should be clocked at the normal line rate. This will ensure the image sensor is ready

to take a new picture with no startup time delay. VDD may also be set to zero to lighten the load on the cooling system.

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