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Readout Artifacts in LUPA 1300-2 and Solutions

Scope

This application is intended to explain some aspects regarding image artifacts in LUPA 1300-2.

AFFECTED OPNs

LUPA 1300-2 mono windowless	NOIL2SM1300A-GWC
LUPA 1300-2 mono	NOIL2SM1300A-GDC
LUPA 1300-2 color	NOIL2SC1300A-GDC

The LUPA 1300-2 Readout

The LUPA family of image sensors features high frame rates for small ROIs. This feature is enabled by a high speed analog multiplexer feeding the data to 24 ADCs operating in parallel.

Inside the multiplexer, several delay stages with controllable values are built in. It has been found that it may be required to tune the settings of these in a few cases when readout artifacts appear at higher temperatures.

ADC Sampling Phase Problems

Symptom

Figure 1 shows an example of an artifact type that may appear at high temperatures and is caused by the sampling (or rather digitization) moment of the ADC appearing too early. Horizontal stripes of length 24 (= the number of ADCs) appear at random positions in the image and grow into vertical bands as the temperature increases. The stripes may be either brighter or darker than the actual image.

Cause

The root cause is a timing mismatch inside the sensor, where the ADC is not sampling the data at the time it appears on its inputs. Some dependence on supply levels and decoupling has also been noticed.

Setting to Tune

The actual time that the ADC is sampling is determined by several settings, but the first action to take in these situations is to try to increase the ADC delay with the `adclck` setting in `5[7:4]` (see Table 1).



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APPLICATION NOTE

The second action is, if the above doesn't help, to use the settings in `14[5]`, `104[1]` and `[2]` to further shift the sampling moment.

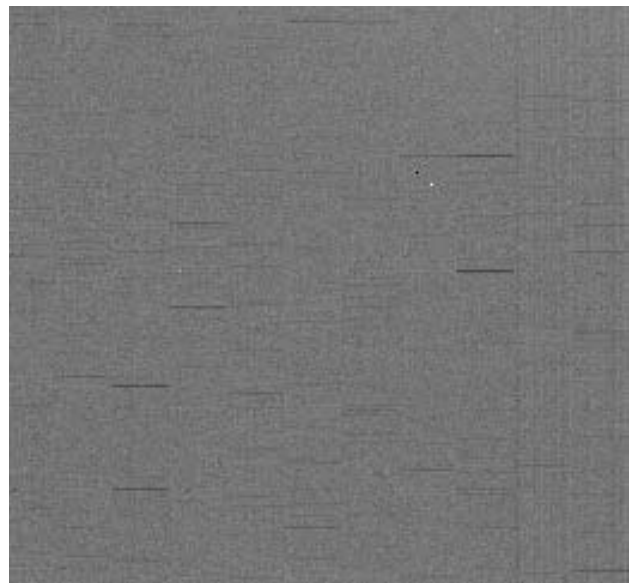



Figure 1. Example of ADC Sampling Phase Artifacts

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Table 1. RELEVANT SETTINGS FOR READOUT DELAY CONTROL

Location	Name	Default	Comment
5[7:4]	clkadc phase	0x0	ADC sampling phase delay
14[5]	clkmaininvert	0x0	When = 1, inverts the IMC main CLK, which causes a small phase shift
57[4:0]	Datadelay	Set to 17 in initialization	Digital delay post ADC
58[7]	Sync_timer	0x0	Gates changes to some settings in between ROTs, so that the sensor is stable during the read-out phase
104[0]	AFE sync bypass	0x0	When = 0, the chip uses an automatic phase alignment circuit for the AFE. This normally works well, but the function can be bypassed by setting this bit = 1. The settings in 104[1] and [2] are used by this tuning circuit.
104[1]	AFE sample egde	0x0	
104[2]	AFE sync egde	0x0	

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