NCV91300 Evaluation Kit User Manual

EVBUM2789

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

DOCUMENT DESCRIPTION

Goal of Document

This document describes the operation and use of the NCV91300 evaluation kit. This kit is provided by ON Semiconductor to help user to evaluate and set up the NCV91300 numerous operation modes as well as the typical operating characteristics.

In this document, user will find information about hardware and Graphical User Interface software, as well as typical Bill of Material, board schematic and layout.

Applicable and Reference Documents

APPLICATION INFORMATION

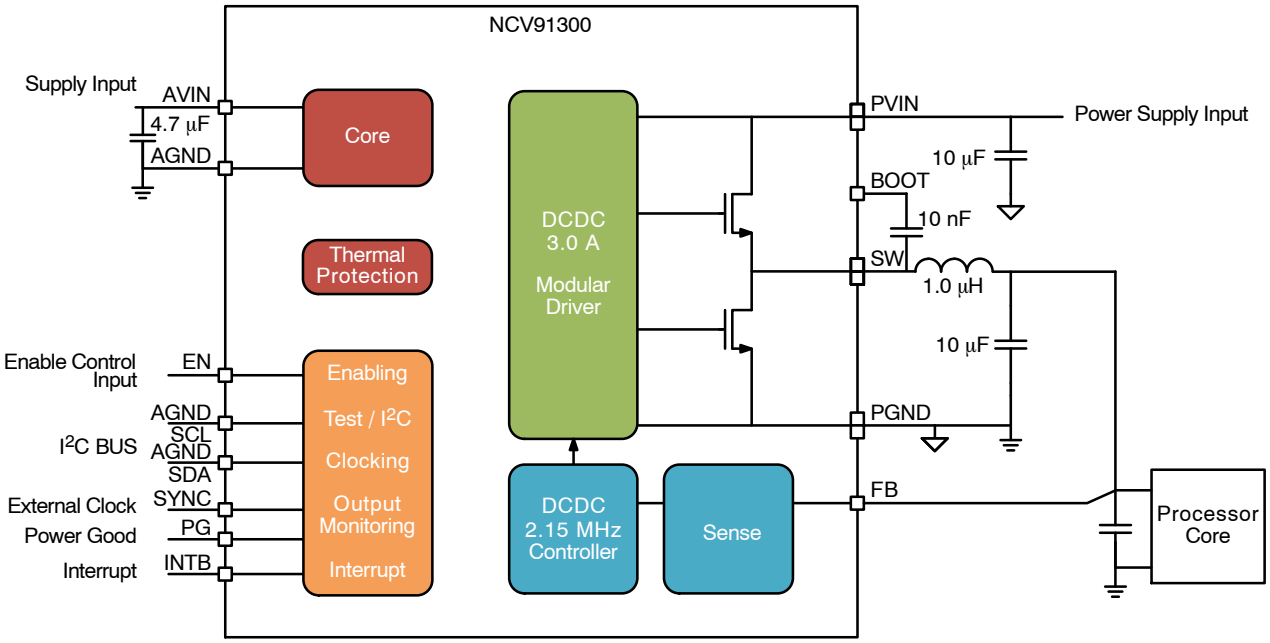

Figure 1. Typical Application Schematic

NCV91300 Data Sheet

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INTRODUCTION

The NCV91300 is a synchronous PWM buck converter optimized to supply the different sub systems of automotive applications post regulation system up to 5 V input. The device is able to deliver up to 3.0 A, with programmable output voltage from 0.6 V to 3.3 V. Operation at up to 2.15 MHz switching frequency allows the use of small components. Synchronous rectification and automatic PFM to PWM transitions improve overall solution efficiency. The NCV91300 is housed in low profile 3.0 x 3.0 mm QFN−16 package.

Content

The evaluation kit comes with 2 boards, associated cables and a self−extractable software.

Requirements

In order to operate properly, user should connect and configure the following components:

- Personal Computer (PC) with at least one USB port to communicate with the Interface Board. Microsoft ".NET Framework 3.5" at least has to be installed. The Graphical User Interface software is installed on this PC and, with this software; user will have full control of the NCV91300 on the evaluation board.
- Evaluation board PCB
- USB interface board. This board is a USB to I^2C interface. It receives from PC Graphical User Interface software all requests and converts it into NCV91300 understandable I^2C command that sets NCV91300 internal registers. If there is an error or if NCV91300 does not acknowledge the request as described in the I^2C specification, the interface board will detect it and will inform the PC Graphical User Interface software. NCV91300 registers are also read through this interface. In that case, the board translates I^2C format received from NCV91300 to USB readable standard. PC Graphical User Interface software will then display the result and NCV91300 configuration to the user.

Eval Kit Installation

To properly operate the eval kit, NCV91300 GUI should be installed:

NCV91300 GUI software installation (Refer to Section GUI Software Installation)

GUI Software Installation

Click on the self−extractable Setup_NCV91300.exe

The installation procedure will install all needed drivers and software. You may have to re−boot your computer after installation completion.

GETTING STARTED

Input / Output Description

This section describes the connectors and jumper settings for proper operation as well as the voltage appropriate range.

Table 1. EVALUATION BOARD OPERATING RANGE

Symbol	Parameter	Min	Typ	Max	Unit
P_{VIN}	Power Supply Range	1.9	3.3	5.5	V
A_{VIN}	Analog Supply Range	3.0	3.3	5.5	V

Table 2. CONFIGURATION CONNECTORS DESCRIPTION

Input / Output	Description	Default Setting
CN1 / CN2	Interface board connector	N/A
J1/J8	Banana Analog Supply Input (positive/negative)	N/A
J3/J8 J5	Banana Power Supply Input (positive/negative) SL5 connector Power supply input	N/A
J2	EN Level Settings • 1−2 EN = V_{BAT} • 2−3 EN = Driven by USB Interface Board	2−3
J9	SYNC Level Settings • 1−2 SYNC = connected to J6 SMA • 2−3 SYNC = Driven by USB Interface Board	2−3
J4	PG pull up	Closed
J7	INTB pull up	Closed
J13/J11 J12	Banana Output voltage (positive/negative) SL5 connector Output Voltage	N/A
J10	Inductor current sense measurement for differential probe (measured across R6 resistor)	N/A
J11	Load transient sense measurement for differential probe (measured across R10 resistor)	N/A
J15	CBOOT measurement for differential probe (measured across C13)	
J6	SMA for SYNC clock injection	N/A
JMP1 / JMP2	GND connector	N/A
S3	Input ferrite bead bypass	Closed
S1	SCL connection to interface board	Closed
S2	SDA connection to interface board	Closed
S4	Output ferrite bead bypass	Closed
S5	DCDC sense selection (local or remote)	Local

The evaluation board duplicates most important signals on test points to the user.

Table 3. TEST POINT

Test Points	Description
TP1	EN: Hardware Enable • EN = LOW: NCV91300 is disabled • EN = HIGH: NCV91300 is enabled
TP2	SYNC signal
TP3	PG: Power Good Signal • PG = LOW: Output voltage out of range • PG = HIGH: Output voltage in range
TP4	SDA: I^2C Data signal
TP5	SCL: I^2C Clock signal
TP6	SW: DC to DC converter switching node
TP7	INTB: Interrupt Signal • INTB = LOW: Interrupt detected • INTB = HIGH: No interrupt
TP8	PGND sense
TP9	PVIN Sense
TP10/TP11	Feedback loop for bode measurements (across R7)
TP12/TP13	VOUT: Output voltage sense (across C17)
TP14	Gate of the Q1 transistor used for Load Transient
TP15	AVIN Sense
TP16	Iout force

Setup

The following steps should be followed before the Evaluation Board is operated

1. Install the Graphical User Interface (GUI) Software on computer
2. Connect the Interface Board to the Board, using the ribbon cable or board to board connectors
3. Connect Output Voltage and Loads (if any) to the board
4. Configure all jumpers to Default Settings
5. Connect the interface board to computer with USB cable
6. Connect NCV91300 Board 2.5 V~5.5 V (See table 1) power supply to J3/J8 (J5) and J1/J8 connectors, pay attention to polarity of power supply and the V clamp of the power supply.
7. Turn power supply on
8. Run the NCV91300 Graphical User Interface Software

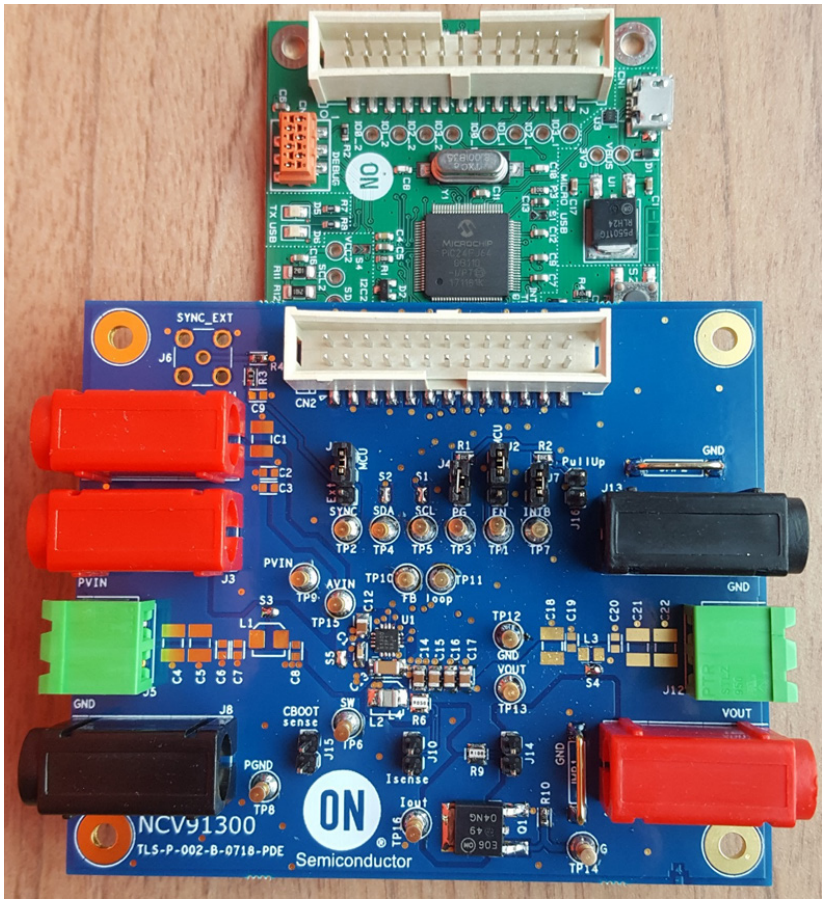

Figure 2. Hardware Setup of EVKit (Board To Board Connection)

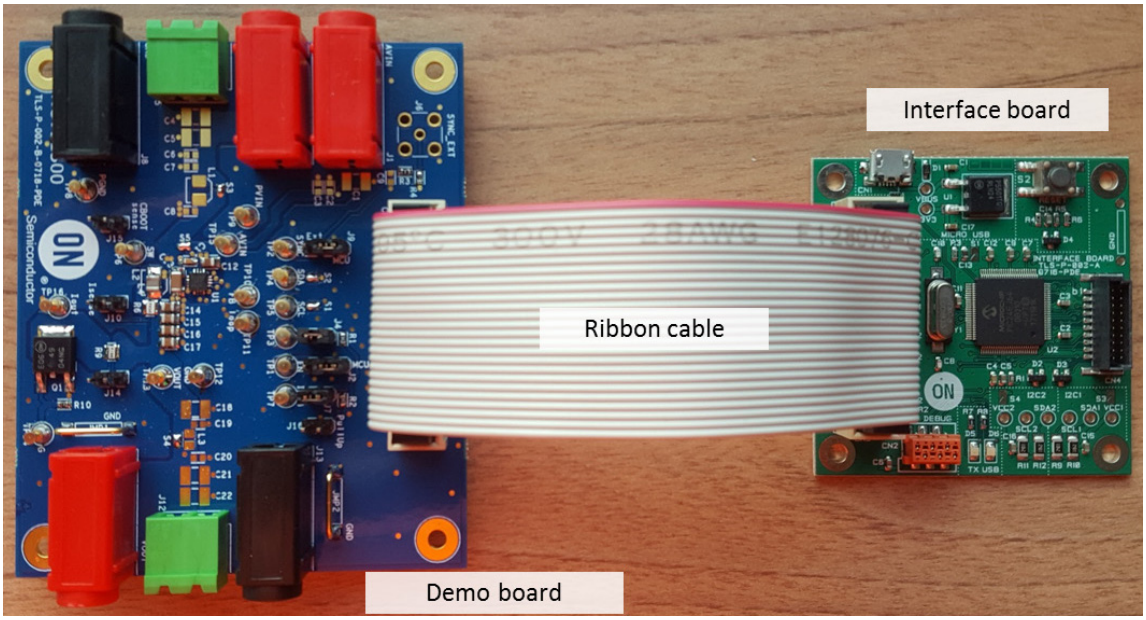

Figure 3. Hardware Setup of EVKit (Ribbon Cable Connection)

BOARD LAYOUT

This section includes the SST layer of PCB layout and EVB board pictures.

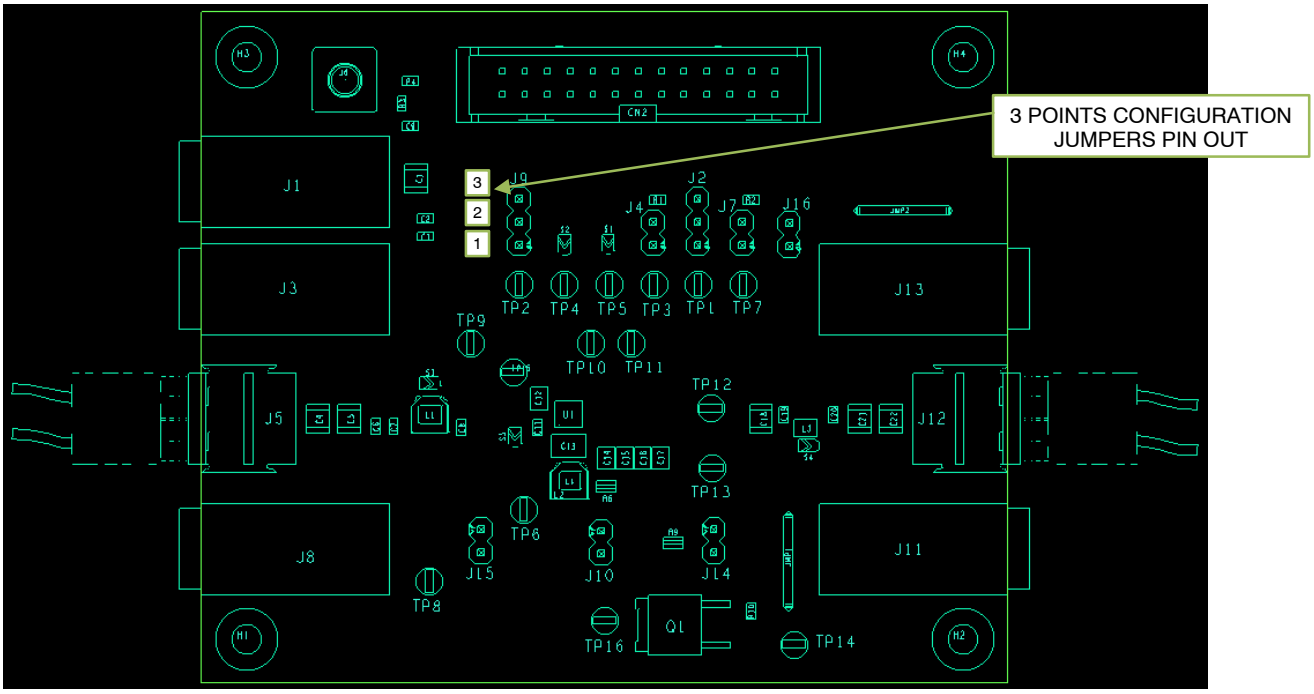

Figure 4. TOP Assembly

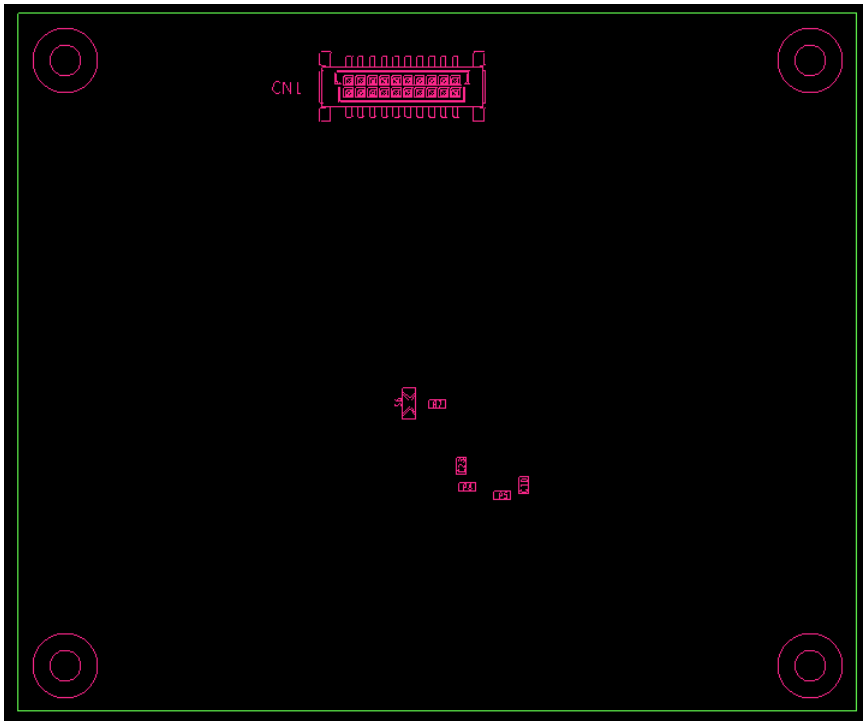

Figure 5. BOTTOM Assembly

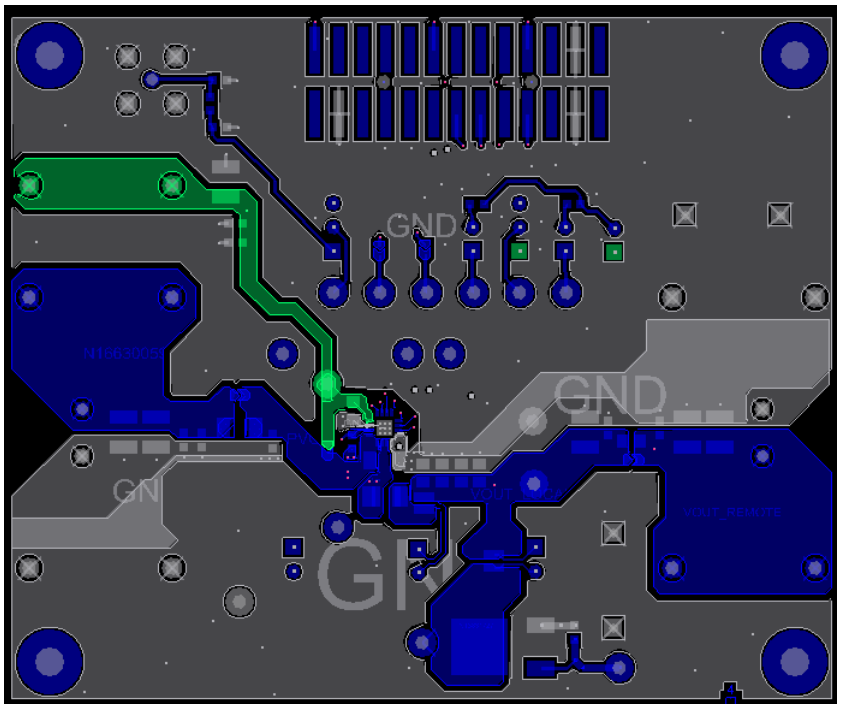

Figure 6. TOP

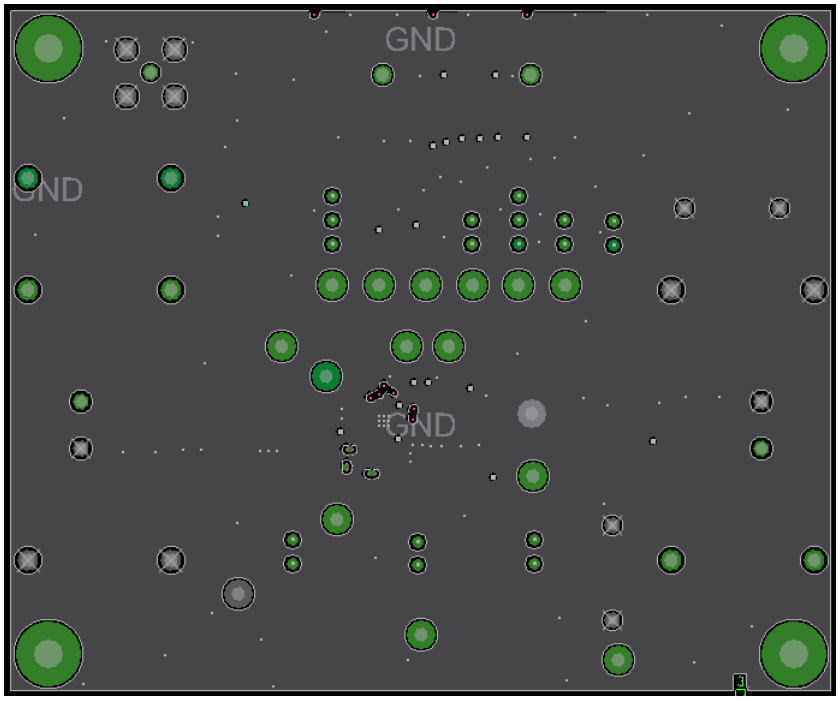

Figure 7. Inner 1

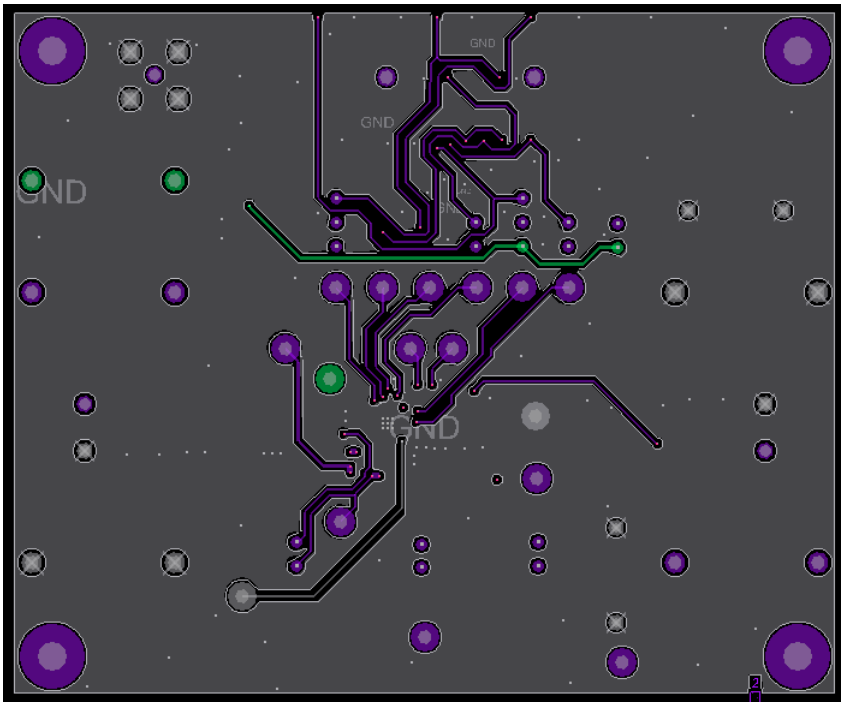

Figure 8. Inner 2

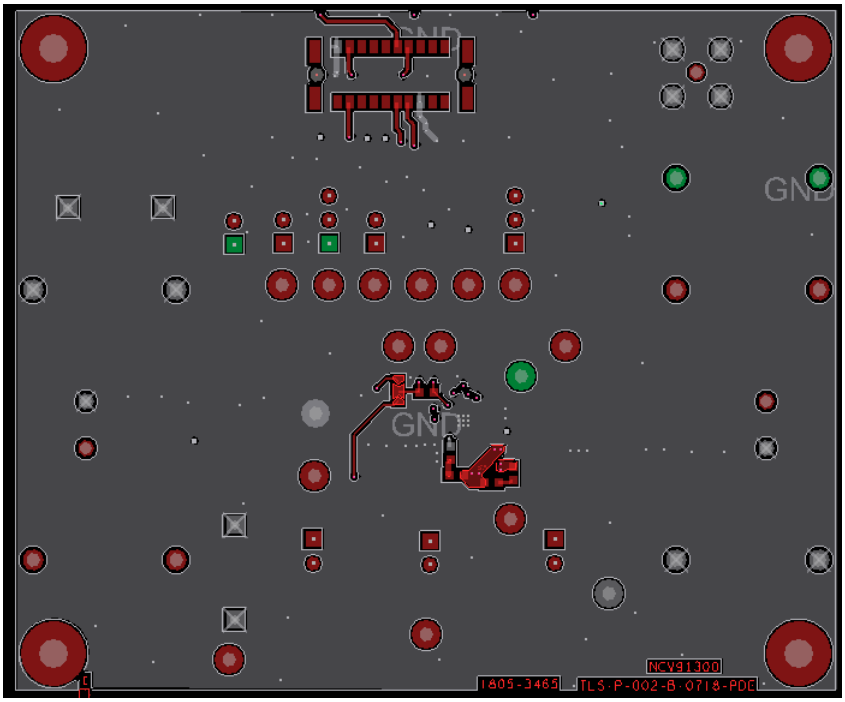

Figure 9. Bottom

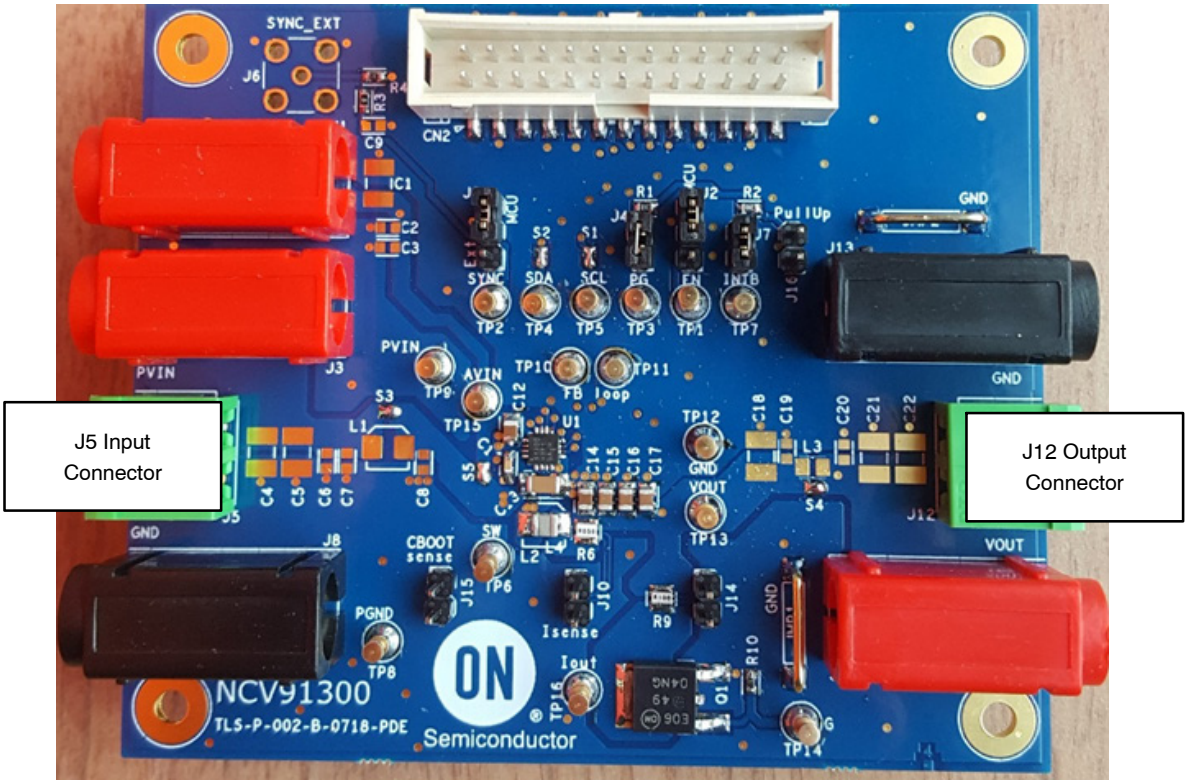

Figure 10. Board Picture TOP View

BOARD SCHEMATIC AND BOM

This section provides the board schematic as well as standard Bill of Material.

Schematic

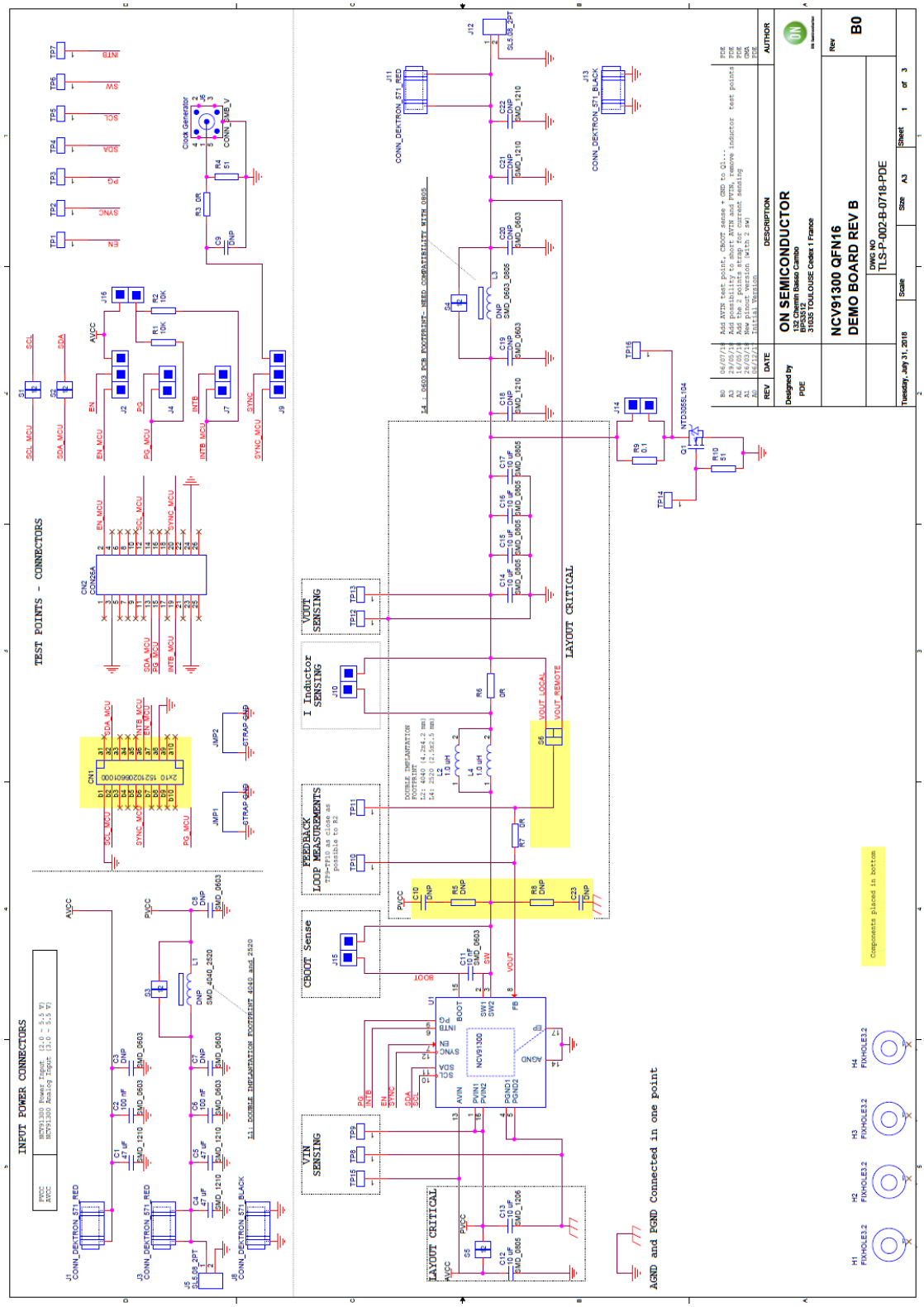

Figure 11. Board Schematic

Revision: 2.1

NCV91300 QFN16 REVC

25−Feb−20

Table 4. BILL OF MATERIAL

Item	Quantity	Reference	Value	Tolerance	Voltage	Techno	Part Number	Part Number (Alternate)	PCB Footprint
1	1	CN1	2x10 15210206601000				15210202601000		HEADER50−100−2x10_F
2	1	CN2	CON26A				HTST−113−01−T−DV−P−TR		HE10−26−SMALL−CI_REV2
3	3	C1,C4,C5	47 μF		6.3 V	X7S	CGA6P1X7S0J476M250AC	GCM32ER70J476ME19	SMD_1210
4	2	C2,C6	100 nF		50 V	X7R	CGA3E2X7R1H104K080A	GCJ188R71C104KA01	SMD_0603
5	8	C3, C7, C8, C9, C10 ,C19 ,C20, 23	DNP						SMD_0603
6	1	C11	10 nF		6.3 V	X7R	CGA3E2X7R2A103K080AA	GCM188R72A103KA37D	SMD_0603
7	5	C12, C14, C15, C16, C17	10 μF		6.3 V	X7R	CGA4J1X7R0J106K125AC	GCM21BR70J106KE22L	SMD_0805
8	1	C13	10 μF		6.3 V	X7R	CGA5L1X7R1E106K160AC	GCM31CR71C106KA64	SMD_1206
9	3	C18, C21, C22	DNP						SMD_1210
10	4	H1, H2, H3, H4	FIXHOLE3.2						FIX3v2H
11	2	JMP1, JMP2	STRAP GND						JUMPER400H
12	3	J1, J3, J11	CONN_DEKTRON_571_RED				DEKTRON_571−0500		BANANA_JACK_REV2
13	2	J2, J9	STRAP 3pins						STRAP3P
14	6	J4, J7, J10, J14, J15, J16	STRAP 2pins						HEADER_2_100H
15	2	J5, J12	SL5.08_2PT						CON2P−5v08_COUDE
16	1	J6	Clock Generator				131−3701−261		CONN_SMB_V
17	2	J8, J13	CONN_DEKTRON_571_BLACK				DEKTRON_571−0100		BANANA_JACK_REV2
18	1	L1	DNP						SMD_4040_2520
19	1	L2	1.0 μH				SPM4020−1R0M−D	FDSD0420D−1R0M	MURATA_4040
20	1	L3	DNP						SMD_0603_0805
21	1	L4	1.0 μH				TFM252012ALMA1R0MTAA	DFE2HCAH1R0MJ0	MURATA_2520
22	1	Q1	NTD3055L104						DPACK_1234
23	2	R1, R2	10K	0.05					SMD_0603
24	2	R3, R7	0R	0.05					SMD_0603
25	2	R4, R10	51	0.05					SMD_0603
26	2	R5, R8	DNP	0.05					SMD_0603
27	1	R6	0.01R	5%			KRL2012E−M−R010−F−T1		SMD_1220
28	1	R9	0.1	5%					SMD_1220
29	5	S1, S2, S3, S4, S5	STRAP PCB						STRAP_PCB
30	1	S6	Strap_PCB_3						STRAP_PCB3
31	16	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16	TEST_POINT						TP_T2_16
32	1	U1	NCV91300						QFN16_3x3_05

GUI SOFTWARE

Once hardware is properly installed and set up, user may use the Graphical User Interface software (GUI in the rest of the document) to set up NCV91300 and read configurations

At start up, the GUI will first read NCV91300 configuration. Please make sure that hardware is supplied prior to GUI startup. Otherwise, the following error will be displayed

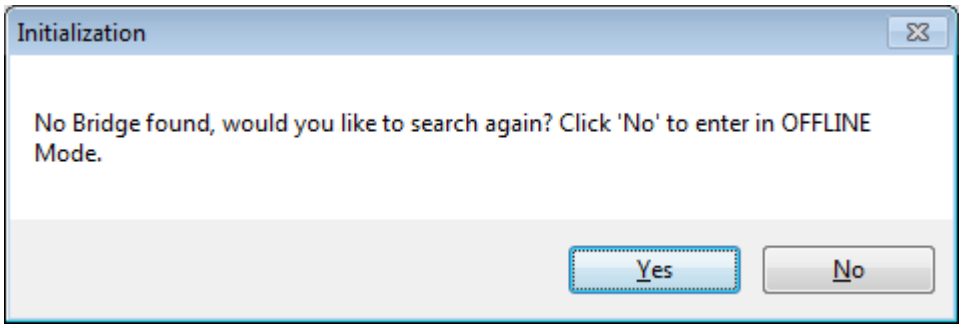

Figure 12.

If during software power up, all the controls are empty, please verified I^2C address and ribbon cable insertion or board to board connection.

Then, the main GUI screen is displayed

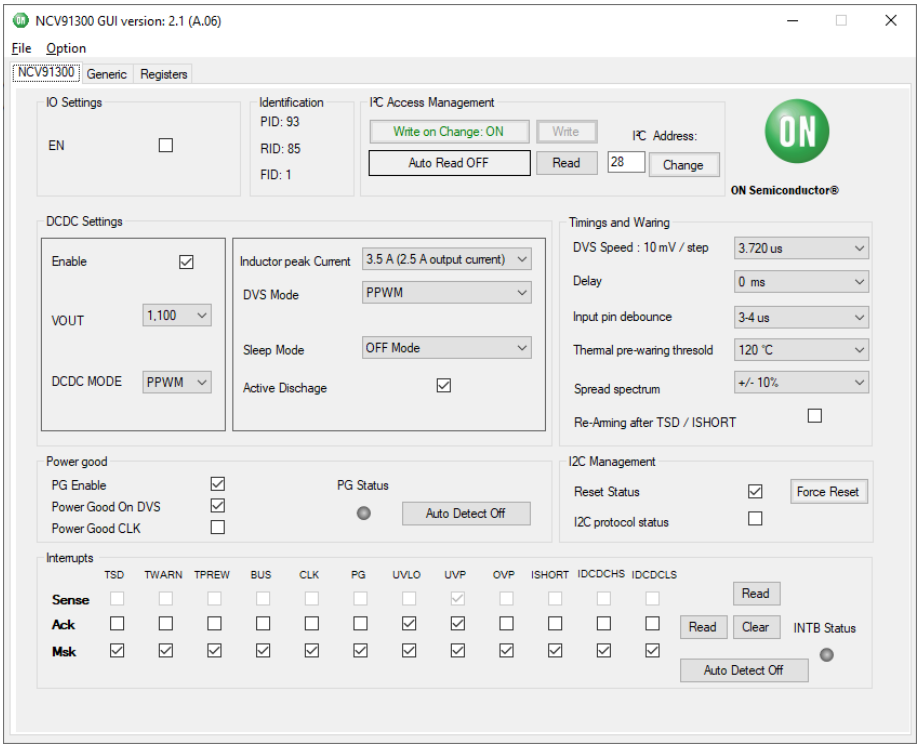

Figure 13. GUI Main Screen

You can click on the Generic tab to access to the generic window, where individual register can be addressed

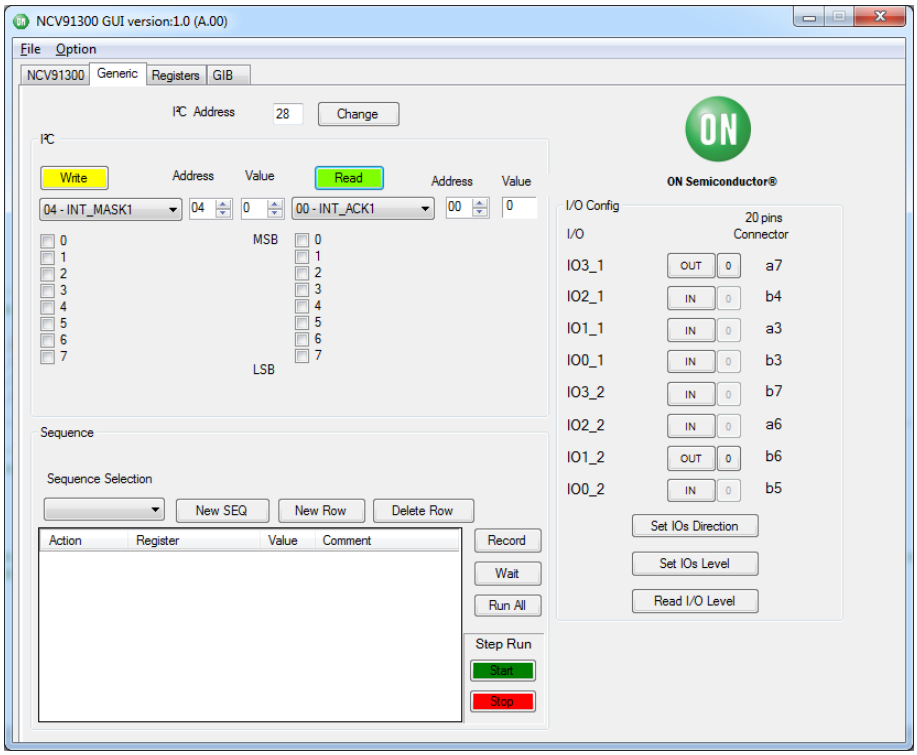

Figure 14. Generic Window

You can click on the Register tab to access to the Register window, where all register can be read and write

Figure 15. Register Window

NCV91300 CONFIGURATION

Table 5. NCV91300 CONFIGURATION

Configuration	3.5 A NCV91300A	2.5 A NCV91300B
Default I²C address PID product identification RID revision identification FID feature identification	ADD1 – 14h : 0010100R/W 93h Metal 00h	ADD1 – 14h : 0010100R/W 93h Metal 01h
Default VOUT	1.25 V	1.1 V
Default MODE	Forced PWM	Forced PWM
Default IPEAK	4.5 A	3.5 A
OPN	NCV91300MNWATXG	NCV91300MNWBTXG
Marking	WA	W3
Output filter	4 x 10 μF	4 x 10 μF

Table 6. I²C REGISTERS MAP CONFIGURATION (NCV91300MNWATXG)

Add.	Register Name	Type	Def.	Function
00h	INT_ACK1	W1C	*00h*	Interrupt register 1
01h	INT_ACK2	W1C	*00h*	Interrupt register 2
02h	INT_SEN1	R	*00h*	Sense register 1 (real time status)
03h	INT_SEN2	R	*00h*	Sense register 2 (real time status)
04h	INT_MSK1	RW	FFh	Mask register 1 to enable or disable interrupt sources (trim)
05h	INT_MSK2	RW	FFh	Mask register 2 to enable or disable interrupt sources (trim)
06h	PID	R	*93h*	Product Identification
07h	RID	R	*Metal*	Revision Identification
08h	FID	R	*00h*	Features Identification (trim)
09h	PROG	RW	*69h*	Output voltage settings (trim)
0Ah	COMMAND	RW	*D7h*	Operating mode, Power good and active discharge settings register (trim)
0Bh	TIME	RW	*27h*	Enabling and DVS timings register (trim)
0Ch	LIMCONF	RW	*D2h*	Reset and limit configuration register (trim)
0Dh to FFh	–	–	–	Reserved. Test Registers

Table 7. I²C REGISTERS MAP CONFIGURATION (NCV91300MNWBTXG)

Add.	Register Name	Type	Def.	Function
00h	INT_ACK1	W1C	*00h*	Interrupt register 1
01h	INT_ACK2	W1C	*00h*	Interrupt register 2
02h	INT_SEN1	R	*00h*	Sense register 1 (real time status)
03h	INT_SEN2	R	*00h*	Sense register 2 (real time status)
04h	INT_MSK1	RW	FFh	Mask register 1 to enable or disable interrupt sources (trim)
05h	INT_MSK2	RW	FFh	Mask register 2 to enable or disable interrupt sources (trim)
06h	PID	R	*93h*	Product Identification
07h	RID	R	*Metal*	Revision Identification
08h	FID	R	*01h*	Features Identification (trim)
09h	PROG	RW	*5Ah*	Output voltage settings (trim)
0Ah	COMMAND	RW	*D7h*	Operating mode, Power good and active discharge settings register (trim)
0Bh	TIME	RW	*2F*	Enabling and DVS timings register (trim)
0Ch	LIMCONF	RW	*52h*	Reset and limit configuration register (trim)
0Dh to FFh	–	–	–	Reserved. Test Registers

REGISTERS DESCRIPTION

The tables below describe the I2C registers.

Registers / Bits Operations:

R	Read only register
W1C	Write to 1 to Clear
RW	Read and Write register
Reserved	Address is reserved and register / bit is not physically designed
Spare	Address is reserved and register / bit is physically designed

In **bold** default can be factory programmed upon request.

Table 8. INTERRUPT ACKNOWLEDGE REGISTER 1

Name: INTACK1				**Address: 00h**			
Type: W1C				**Default: 00000000b (00h)**			
Trigger: Dual Edge [D7..D0]							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	ACK_UVLO	ACK_UVP	ACK_OVP	Spare = 0	ACK_ISHORT	ACK_IDCDCHS	ACK_IDCDCLS

Bit	**Bit Description**
ACK_IDCDCLS	DC−DC Negative Over Current Sense Acknowledgement 0: Cleared 1: DC−DC Negative Over Current Event detected
ACK_IDCDCHS	DC−DC Over Current Sense Acknowledgement 0: Cleared 1: DC−DC Over Current Event detected
ACK_ISHORT	DC−DC Short−Circuit Protection Sense Acknowledgement 0: Cleared 1: DC−DC Short circuit protection detected
ACK_OVP	PV_{IN} Overvoltage Protection Sense Acknowledgement 0: Cleared 1: OVP Event detected
ACK_UVP	PV_{IN} Undervoltage Protection Sense Acknowledgement 0: Cleared 1: UVP Event detected
ACK_UVLO	Under Voltage Sense Acknowledgement 0: Cleared 1: Under Voltage Event detected

Table 9. INTERRUPT ACKNOWLEDGE REGISTER 2

Name: INTACK2				**Address: 01h**			
Type: W1C				**Default: 00000000b (00h)**			
Trigger: Dual Edge [D7..D0]							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	ACK_TSD	ACK_TWARN	ACK_TPREW	Spare = 0	ACK_BUS	ACK_CLK	ACK_PG

Bit	**Bit Description**
ACK_PG	Power Good Sense Acknowledgement 0: Cleared 1: DC−DC Power Good Event detected
ACK_CLK	Working Clock Indicator Acknowledgement 0: Cleared 1: DC−DC switching frequency source changed
ACK_BUS	Double write Error Acknowledgement 0: Cleared 1: Invalid double write access
ACK_TPREW	Thermal Pre Warning Sense Acknowledgement 0: Cleared 1: Thermal Pre Warning Event detected
ACK_TWARN	Thermal Warning Sense Acknowledgement 0: Cleared 1: Thermal Warning Event detected
ACK_TSD	Thermal Shutdown Sense Acknowledgement 0: Cleared 1: Thermal Shutdown Event detected

Table 10. INTERRUPT SENSE REGISTER 1

Name: INTSEN1				**Address: 02h**			
Type: R				**Default: 00000000b (00h)**			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	SEN_UVLO	SEN_UVP	SEN_OVP	Spare = 0	Spare= 0	SEN_IDCDCHS	SEN_IDCDCLS

Bit	**Bit Description**
SEN_IDCDCLS	DC−DC negative over current sense 0: DC−DC negative current is below limit 1: DC−DC negative current is over limit
SEN_IDCDCHS	DC−DC over current sense 0: DC−DC output current is below limit 1: DC−DC output current is over limit
SEN_OVP	PV_{IN} Overvoltage Protection Sense 0: OVP not detected 1: OVP detected
SEN_UVP	PV_{IN} Undervoltage Protection Sense 0: UVP not detected 1: UVP detected
SEN_UVLO	Under Voltage Sense 0: Input Voltage higher than UVLO threshold 1: Input Voltage lower than UVLO threshold

Table 11. INTERRUPT SENSE REGISTER 2

Name: INTSEN2				**Address: 03h**			
Type: R				**Default: 00000000b (00h)**			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 0	SEN_TSD	SEN_TWARN	SEN_TPREW	Spare = 0	SEN_BUS	SEN_CLK	SEN_PG

Bit	**Bit Description**
SEN_PG	Power Good Sense 0: DC−DC Output Voltage below target 1: DC−DC Output Voltage within nominal range
SNS_CLK	Working Clock Indicator Sense 0: DC−DC switching frequency follows the Internal Oscillator 1: DC−DC switching frequency follows the SYNC pin
SEN_BUS	Double write Error Sense 0: No error 1: Invalid double write access
SEN_TPREW	Thermal Pre Warning Sense 0: Junction temperature below thermal pre−warning limit 1: Junction temperature over thermal pre−warning limit
SEN_TWARN	Thermal Warning Sense 0: Junction temperature below thermal warning limit 1: Junction temperature over thermal warning limit
SEN_TSD	Thermal Shutdown Sense 0: Junction temperature below thermal shutdown limit 1: Junction temperature over thermal shutdown limit

Table 12. INTERRUPT MASK REGISTER 1

Name: INTMSK1				**Address: 04h**			
Type: RW				**Default: See Register map**			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 1	**MSK_UVLO**	**MSK_UVP**	**MSK_OVP**	Spare = 1	**MSK_ISHORT**	**MSK_IDCDCHS**	**MSK_IDCDCLS**

Bit	**Bit Description**
MSK_IDCDCLS	DC−DC negative over current interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_IDCDCHS	DC−DC over current interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_ISHORT	DC−DC Short−Circuit Protection mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_OVP	PV_{IN} Over Voltage interrupt Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_UVP	PV_{IN} Under Voltage interrupt Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_UVLO	Under Voltage interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked

Table 13. INTERRUPT MASK REGISTER 2

Name: INTMSK2				**Address: 05h**			
Type: RW				**Default: See Register map**			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare = 1	**MSK_TSD**	**MSK_TWARN**	**MSK_TPREW**	Spare = 1	**MSK_BUS**	**MSK_CLK**	**MSK_PG**

Bit	**Bit Description**
MSK_PG	Power Good interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_CLK	Working Clock Indicator interrupt Mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_BUS	Double write Error interrupt source mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_TPREW	Thermal Pre Warning interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_TWARN	Thermal Warning interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked
MSK_TSD	Thermal Shutdown interrupt mask 0: Interrupt is Enabled 1: Interrupt is Masked

Table 14. PRODUCT ID REGISTER

Name: PID				**Address: 06h**			
Type: R				**Default: 00011011b (93h)**			
Trigger: N/A				**Reset on N/A**			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Table 15. REVISION ID REGISTER

Name: RID				**Address: 07h**			
Type: R				**Default: Metal**			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
RID_7	RID_6	RID_5	RID_4	RID_3	RID_2	RID_1	RID_0

Bit	**Bit Description**
RID[7..0]	Revision Identification 10000000: V3P1 00100000: V1TC 10000100: Pass 2.0

Table 16. FEATURE ID REGISTER

Name: FID				**Address: 08h**			
Type: R				**Default: See Register map**			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Spare	Spare	Spare	Spare	FID_3	FID_2	FID_1	FID_0

Bit	**Bit Description**
FID[3..0]	Feature Identification

Table 17. DC−DC VOLTAGE PROG REGISTER

Name: PROG				**Address: 09h**			
Type: RW				**Default: See Register map**			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Vout [7..0]							

Bit	**Bit Description**
Vout [7..0]	Sets the DC−DC converter output voltage 00000000b = 600 mV (5mV step) 00000001b = 605 mV (5 mV step) … 01001111b = 950 mV (5 mV step) 01010000b = 1000 mV (10 mV step) 01010001b = 1010 mV (10 mV step) … 10110011b = 1990 mV (10 mV step) 10110100b = 2000 mV (20 mV step) 10110101b = 2020 mV (20 mV step) … 11110100b = 3280 mV (20 mV step) 11110101b = 3300 mV (20 mV step) … 11111111b = 3300 mV

Table 18. COMMAND

Name: COMMAND				Address: 0Ah			
Type: RW				Default: See Register map			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DVSMODE	**PWM**	**SLEEP_MODE**	**DISCHG**	**PGCLK**	**ENABLE**	**PGDVS**	**PGDCDC**

Bit	Bit Description
PGDCDC	Power Good Enabling 0 = Disabled 1 = Enabled
PGDVS	Power Good Active On DVS 0 = Disabled 1 = Enabled
ENABLE	EN Pin Gating 0: Disabled 1: Enabled
PGCLK	Power Good CLK Enabling 0 = Disabled 1 = Enabled
DISCHG	Active discharge bit Enabling 0 = Discharge path disabled 1 = Discharge path enabled
SLEEP_MODE	Sleep mode 0 = Low Iq mode when EN low 1 = Force product in sleep mode
PWM	Operating mode selection 0 = Auto 1 = Forced PWM
DVSMODE	DVS transition mode selection 0 = Auto 1 = Forced PWM

Table 19. TIMING REGISTER

Name: TIME				Address: 0Bh			
Type: RW				Default: See Register map			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DELAY[1..0]		**F_SPREAD[1..0]**		**DVS[1..0]**		**DBN_Time[1..0]**	

Bit	Bit Description
DBN_Time[1..0]	EN debounce time 00 = 1−2 μs 01 = 1−2 μs 10 = 2−3 μs 11 = 3−4 μs
DVS[1..0]	DVS Speed 00 = 10 mV step / 0.465 μs 01 = 10 mV step / 0.930 μs 10 = 10 mV step / 1.860 μs 11 = 10 mV step / 3.720 μs
F_SPREAD[1..0]	Spread Spectrum 00 = No Spread Spectrum 01 = ±5 % spread spectrum 10 = ±10 % spread spectrum 11 = ±10 % spread spectrum
DELAY[1..0]	Delay applied upon enabling (ms) 00b = 0 ms − 11b = 6 ms (Steps of 2 ms)

Table 20. LIMITS CONFIGURATION REGISTER

Name: LIMCONF				**Address: 0Ch**			
Type: RW				**Default: See Register map**			
Trigger: N/A							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
IPEAK[1..0]		**TPWTH[1..0]**		**ROBUSTI2C**	FORCERST	RSTSTATUS	**REARM**
Bit		**Bit Description**					
REARM		Rearming of device after TSD / ISHORT 0: No re−arming after TSD / ISHORT 1: Re−arming active after TSD / ISHORT with no reset of I^2C registers: FPUS (Fast power up sequence) is initiated with previously programmed I^2C registers values					
RSTSTATUS		Reset Indicator Bit 0: Must be written to 0 after register reset 1: Default (loaded after Registers reset)					
FORCERST		Force Reset Bit 0 = Default value. Self−cleared to 0 1: Force reset of internal registers to default					
TPWTH[1..0]		Thermal pre−Warning threshold settings 00 = 110°C 01 = 120°C 10 = 130°C 11 = 140°C					
ROBUSTI2C		I^2C protocol setting 0 : Classic I^2C protocol 1: Double write access I^2C protocol					
IPEAK		Inductor peak current settings 00 = 3.0 A (for 2.0 A output current) 01 = 3.5 A (for 2.5 A output current) 10 = 4.0 A (for 3.0 A output current) 11 = 4.5 A (for 3.5 A output current)					

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