Capacitive behaviour in Super Junction Trench MOSFET devices

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***Abstract*— This paper exploits for the first time the capacitive behaviour of Super Junction (SJ) Trench Power MOSFETs as a characterization method to determine their Charge Balance (CB). Differently from blocking voltage methods, the capacitive method allows the CB extraction in 800 V SJ devices by using low voltage systems (<30 V) to extract the drain-source capacitance (C_{ds}) in function of the drain-source voltage (V_{ds}). Hence, the device-under-test is never stressed in avalanche, avoiding device degradation and/or destruction. The correlation between the minimum C_{ds} value at 25 V and the optimum CB is demonstrated by TCAD simulations and measurements. As a result, the highest breakdown voltage (V_{bd}), corresponding to the optimum CB, is determined by measuring C_{ds} at 25 V. Moreover, the maximum V_{ds} pinch voltage (V_{pinch}) exhibits a maximum value when C_{ds} at 25 V is minimum, thus also being an interesting parameter to monitor.**

Keywords — Trench, Super-Junction, Charge Balance

I. INTRODUCTION

One of the key parameters in a conventional power MOSFET is the specific on resistance value ($R_{DS}{\cdot}A$), which has been improved with the Super Junction (SJ) concept. It consists of the substitution of the low doped N drift region by alternating thin columns of opposite doping type. The addition of the P column modifies the depletion process and the electric field distribution. The highest V_{bd} is reached when a charge balance (CB) of both N and P columns is set [1,2,3].

In this work, a method to determine the real CB in a fabricated SJ structure is proposed, avoiding the possible destruction of the device by the conventional V_{bd} measurement technique. The SJ trench MOSFET is briefly described and its depletion at low drain bias is analyzed. It is demonstrated by TCAD simulations and measurements that the V_{bd} value can be estimated by measuring the drain-source capacitance (C_{ds}) at 25 V.

II. DEVICE STRUCTURE AND MEASUREMENT SET-UP DESCRIPTION

A. *Device structure*

A SJ trench MOSFET [4, 5] has been studied and fabricated, in contrast to using the multi-epitaxial/multi-implant process (as the so-called CoolMOS [6]). The SJ trench structure, shown in Fig. 1, consists on vertical N and P-type layers selectively grown on the sidewalls of a deep trench, which is implemented in a lightly doped substrate (N^-_{epi}). The trench is sealed with oxide after the last epitaxial layer growth. The bottom of the N^+ pillar is connected to the high doped substrate N^+_{sub}. The P_{body} diffusion is connected to the source electrode and implements the channel of the MOSFET. The top of the P pillar is connected to the P_{body} diffusion. The N_{link} diffusion allows the connection between the N pillar and the bottom of the gate trench. In the on-state the current will flow from the N_{link} and it will go into the N pillar. In the off-state the N^-_{epi} layer handles the high drain voltage.

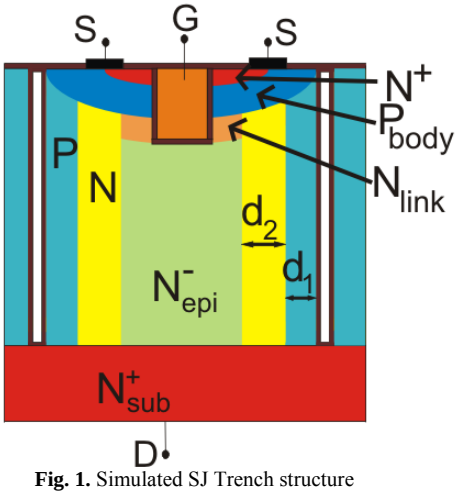

Fig. 1. Simulated SJ Trench structure

The device has different N and P regions, and the charge between all of them has to be balanced to obtain an equipotential lines distribution perfectly horizontal in the depleted region, at high drain applied bias. The result of this balance is a high V_{bd} when the optimum CB is set, obtaining a lower R_{ON} than a conventional VDMOS due to the high N pillar donor concentration. The CB is set according to Eq. 1 (normally expressed in %). The concentration of the N pillar is defined as N_{dose} and the concentration of the P pillar as P_{dose}.

$$CB = \frac{(P_{dose} * d1) - (N_{dose} * d2)}{(N_{dose} * d2)} \quad (1)$$

B. *Measurement set-up*

TCAD simulations have been performed in the SJ Trench Power MOSFET structure. The DIOS platform [7] is used to simulate the technological process flow of the structure plotted in Fig.1, whereas the SDevice is used to electrically simulate the structure obtained from the DIOS simulation, extracting the V_{bd} value and the C_{ds}-V_{ds} curve. The reported simulations and measurements are obtained from a transistor structure, sweeping the drain with grounded source and floating gate. The voltage sweep applied to the device to extract the C_{ds}-V_{ds} curve has been done from 0 to 25 V with 0.5 V steps. The applied AC signal has a level of 0.26 V with a 10 kHz frequency.

The DIOS simulations were performed according to the splits on the pillar doping level of the processed wafers, and compared with the experimental electrical performance to ensure accurate simulation results. Fig.2 shows a comparison between measured C_{ds}-V_{ds} and two simulated curves for different CB conditions. Notice that the experimental curve shape is very well replicated by the simulated ones.

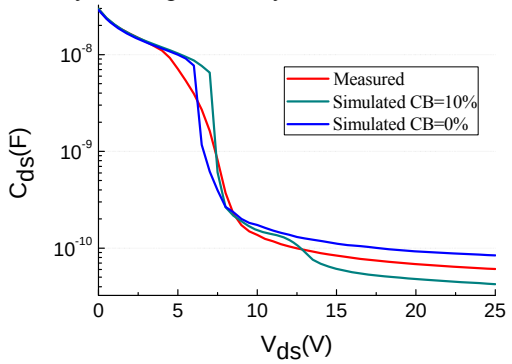

Fig. 2: Comparison between measured and simulated C_{ds}-V_{ds} curves

The electrical parameters extracted from the C_{ds}-V_{ds} curves are the capacitance at 0V (C@0 V), the capacitance at 25 V (C@25V) and V_{ds} pinch voltage (V_{pinch}), that is the voltage at which the capacitance has the maximum slope in the C_{ds}-V_{ds} curve. A dC_{ds}/C_{ds} curve used to determine the V_{pinch} value from the C_{ds}-V_{ds} curve is calculated in one of the measured devices and shown in Fig. 3. The maximum dC_{ds}/C_{ds} value is set as V_{pinch}.

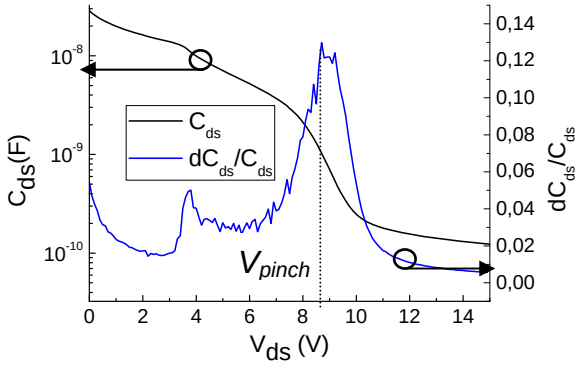

Fig. 3: Extraction of V_{pinch} from a C_{ds}-V_{ds} measured curve. In this case V_{pinch}=8.8 V.

III. DEPLETION BEHAVIOUR IN THE SJ TRENCH DEVICE

The depletion behaviour of the SJ trench device has been analyzed from TCAD simulations in three different CB conditions: positive, negative and optimum. The C_{ds}-V_{ds} curves for the three cases are shown in Fig. 4. All the curves exhibit an initial decrease of almost 2 decades at low drain applied bias (lower than 15V) because of the merging of the vertical and horizontal depletion regions. Nevertheless, the depletion expands into the N^-_{epi} layer in a different way depending on the CB between the pillars, as reported in this section.

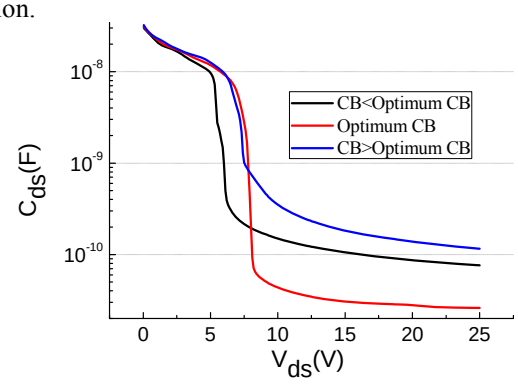

Fig. 4: Simulated C_{ds}-V_{ds} curves for different CB conditions. Notice that the minimal C@25V is reached when the CB is optimum.

The capacitance at high voltage (100 V) is the same for all cases since the capacitance can be deduced from Eq. 2 (being *d* the depletion width and *l* the extension of the depletion) [8].

$$C_{ds} = \varepsilon_{si} \frac{l}{d} \tag{2}$$

The snapshots presented in Figs. 5-8 have been taken from the simulation of the C_{ds}-V_{ds} curve at the region where C_{ds} drops with V_{ds}. The white lines in the captured snapshots delimit the extension of the depletion region of the structure for an applied drain bias. It can be noticed that the separation between lines increases with the drain voltage, so C_{ds} will be lower as a consequence of the increase of *d*. The capacitance value does not depend on *l* since it is maximum from the very beginning. The *d* value is maximal at 25 V when the CB is optimum, leading to the minimum C_{ds} value.

A. *Optimum CB (10 %< CB<20%)*

The expansion of the depletion process of both P and N pillars is completely symmetrical. The sharp drop of the C_{ds} curve occurs at a drain bias between 7 and 8 V, once the depletion region has reached the trench oxide in the right edge of the plotted structure. The N^-_{epi} region is depleted due to the P pillar and the P_{body} donor compensation, after the top of the N pillar and the N_{link} are depleted. In Fig. 5 the fully depletion of the N pillar at the region close to the N_{link} can be observed, in which voltage the structure starts depleting vertically in the N^-_{epi} layer.

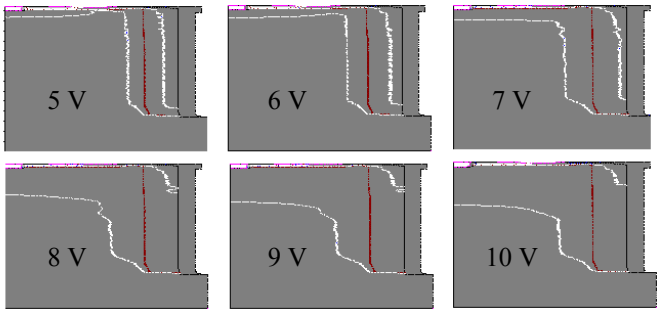

Fig. 5: Depletion in a SJ Trench structure at the Optimum CB case. X and Y are not drawn to scale.

B. Higher P_{dose} than N_{dose} (CB >Optimum CB)

With positive CB, the depleted region does not reach the trench oxide until high drain voltage values are applied to the drain since more donors are needed to compensate the total charge of the P column. It can be envisaged from the snapshots of Fig. 6 that as the drain potential increases, the N_{link} diffusion and the N column are depleted and, before the extension of the depletion region reaches the trench oxide, the N^-_{epi} is already depleted. As a consequence, the C_{ds} drop is not so sharp since the lateral depletion through the P column is not completed, thus *d* is not maximal.

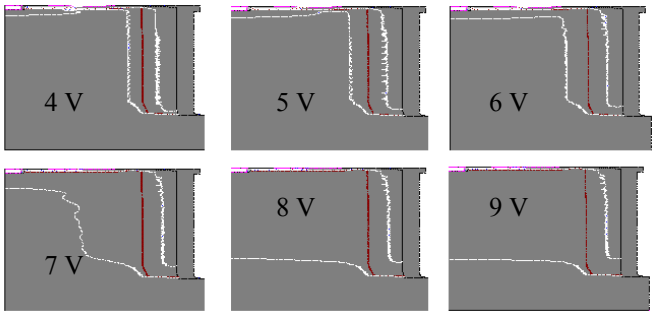

Fig. 6: Depletion in a SJ Trench structure at the *Higher P_{dose} than N_{dose} case.* X and Y are not drawn to scale.

C. Higher N_{dose} than P_{dose} (CB <Optimum CB)

As in the previous cases, the P_{body} region helps to deplete the N_{link} region. The N_{link} is fully depleted before the N-column starts depleting, and that is when the vertical depletion between P_{body} and N^-_{epi} also starts. The C_{ds} drop happens when the vertical and lateral extension of the depletion region merge (between 5 and 6 V, as shown in the zoom of Fig. 7), since the maximal *d* can be taken into account in the top region of the N pillar. The snapshots of Fig. 8 clearly indicate that the N^-_{epi} region is not depleted at low drain bias.

Fig. 7: Depletion zoom in a SJ Trench structure at the *Higher N_{dose} than P_{dose} case.* X and Y are not drawn to scale.

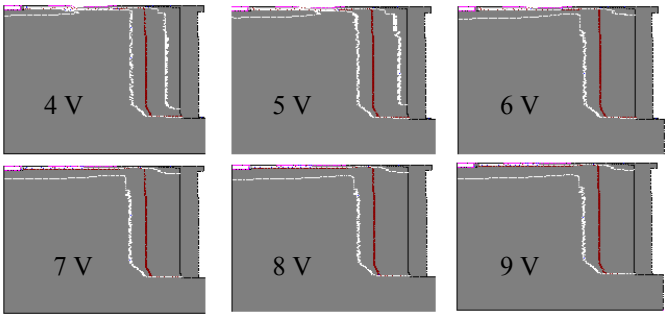

Fig. 8: Depletion in a SJ Trench structure at the *Higher N_{dose} than P_{dose} case.* X and Y are not drawn to scale.

It can be concluded that V_{bd} is maximal when C_{ds} is minimal due to the highest depletion of the lateral and vertical junctions. The sharp decrease observed in the C_{ds}-V_{ds} curve is due to the merge of the lateral and vertical depletion regions. Moreover, the depletion of the N_{link} is faster with CB < Optimum CB than with CB ≥ Optimum CB since more potential is needed to deplete the N pillar. It leads to a faster merging of the vertical and the lateral junctions; hence the C_{ds}-V_{ds} curve drops at lower drain voltage values. Finally, in the negative CB case the depletion of the P pillar is almost complete at low drain bias, and it contributes increasing the *d* parameter, thus decreasing the C_{ds} value.

IV. C_{DS}- V_{DS} AND TECHNOLOGICAL PARAMETERS

The C_{ds}-V_{ds} simulated curves for different N_{dose} and CB=10% are plotted in Fig. 9. The capacitance curve shifts to the right when increasing the N_{dose}, since more potential is needed to deplete the same area as with lower N_{dose}. The shape of all curves is the same since the P_{dose} is also proportionally increased (same CB for all of them). The V_{pinch} values as a function of the N_{dose} from simulations and measurements are also plotted in Fig. 9. The small difference in the V_{pinch} values between simulations and measurements, depending on the N_{dose}, is due to the fact that in the fabricated transistors the N_{dose} is a little bit lower than expected. In both cases, the V_{pinch} value increases with the N_{dose} and, since V_{bd} increases when decreasing the N_{dose} as shown in Fig. 10, a trade-off between N_{dose} and V_{bd} has to be set, taking into account that a low N_{dose} leads to a high R_{on}. The CB is set to the 10%, since not just the pillars but the N^-_{epi} region have to be also depleted, thus more P is needed.

The relation between V_{pinch} and V_{bd} is shown in Fig. 11, where the results of the measurements on devices implemented on wafers with different N_{dose} and different CB are plotted. From this graph it can be concluded that the lower V_{pinch} leads to a high V_{bd}. It makes sense since a low V_{pinch} means a low N_{dose}, thus for the non-optimal CB, the V_{bd} is higher (see Fig.10).

The evolution of C_{ds}@25 V, V_{pinch} and V_{bd} (scaled as V_{bd}/50) over a whole row in a wafer of SJ Trench transistors is plotted in Fig. 12. The wafer was processed to do not have a

uniform CB over the whole wafer, corroborating that C_{ds}@25 V is minimal when V_{bd} is maximal. It can also be inferred that as expected, V_{pinch} is following the C_{ds} curve since the minimal V_{pinch} corresponds to the maximal V_{bd}.

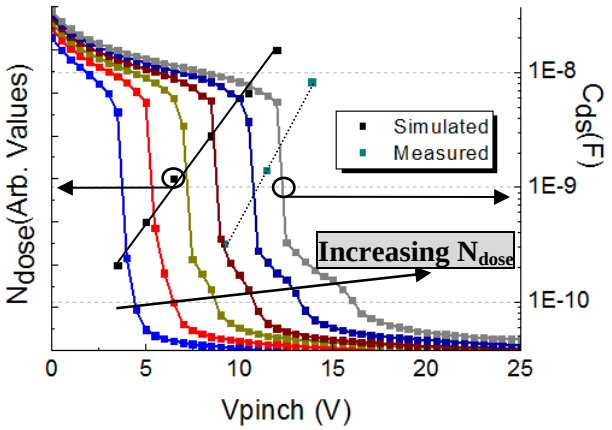

Fig. 9: Simulated C_{ds}-V_{ds} curves for different N_{dose} (being N_{dose}1 the lower level and N_{dose}6 the higher). The squares correspond to V_{pinch} simulated and measured values for different N_{dose} level (left axis). Note that the tendency is the same for measurements and simulations.

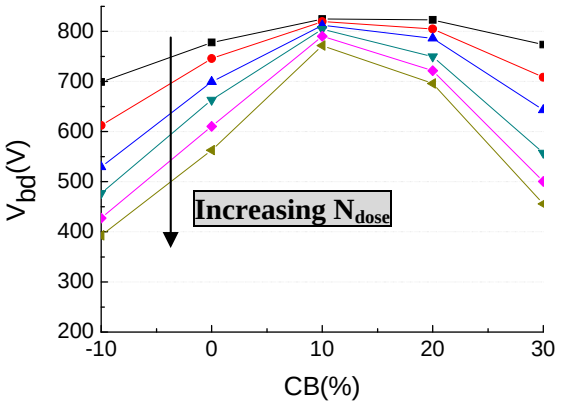

Fig. 10: Simulated CB-V_{bd} trade-off for different N_{dose} level. The maximum V_{bd} value is reached when the optimum CB is set.

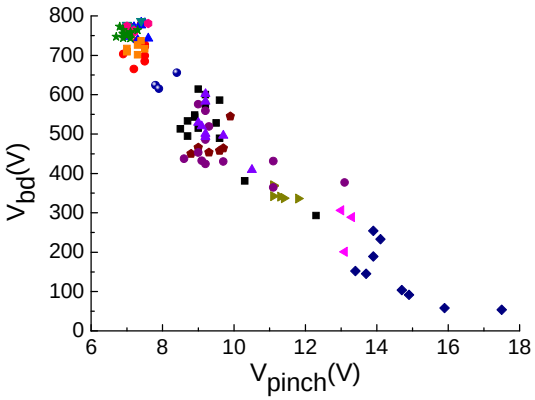

Fig. 11: V_{bd} -V_{pinch} relation for measured SJ Trench transistors in the central row of processed wafers with different N_{dose}

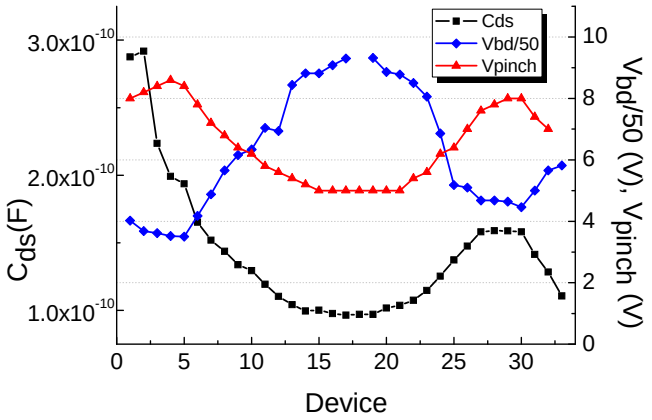

Fig. 12: V_{bd}/50, V_{pinch} and C_{ds}@25V for SJ Trench transistors in the central row of a wafer

V. CONCLUSION

The capacitive behaviour in Super Junction power MOSFETs has been studied to extract the charge balance and to predict the voltage capability of fabricated transistors without degrading the device. A relation between C_{ds}-V_{ds} curves, V_{pinch} and V_{bd} has been demonstrated with simulations and measurements on fabricated SJ trench power MOSFET devices. The capacitive behaviour has been described by the evolution of the depletion region when low drain voltage is applied. A good correlation between TCAD simulations and measurements has been obtained.

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