

An Efficient Nonisolated DC-DC Converter and a Review of the More Common Topologies

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Abstract---There are several approaches to nonisolated dc-dc conversion for use when the input varies above and below the output. Among these are the SEPIC, buck-boost and others involving a combination of buck and boost circuits. This paper contains an analysis of four types, with particular attention to the efficiency in a typical application.

INTRODUCTION

Of the several ways to produce a regulated output voltage (without input-output isolation), most have a fundamental drawback: Their efficiency is no better when the input is equal to the output than it is when they are quite different. In looking at the popular approaches such as the SEPIC, C'uk and combination buck + boost circuits, it is obvious that this can be expected. Even when the input voltage is close or equal to the output voltage, the same amount of switched-mode processing occurs as when the voltages are substantially different. It was learned that a cascade of the classic buck and boost circuits, when properly controlled, is by far more efficient than the others when the input is near or equal to the output voltage. This is not an invention, as this approach has been documented and is actually in use [1]. But, because of the application not being in the mainstream of dc-dc applications, it appears that this valuable technique has been largely overlooked. The application described in the above-referenced paper is a high-power three-phase power correction system for large main-frame computers. It is not surprising that it does not show up in a casual search for dc-dc conversion techniques!

This paper contains an analysis of four topologies---three combination buck + boost circuits and the single-ended primary inductance converter (SEPIC). In each case, typical components are used, with their parasitic losses included. The classic buck-boost converter and the C'uk converter were not included, because in the nonisolated versions the output is of opposite polarity to the input.

CIRCUIT DIAGRAMS

Figures 1 through 4 illustrate the boost + buck, SEPIC, buck + boost, and a second version of the buck + boost with both switches driven simultaneously. D1 and D2 are the duty ratios of switches S1 and S2, respectively.

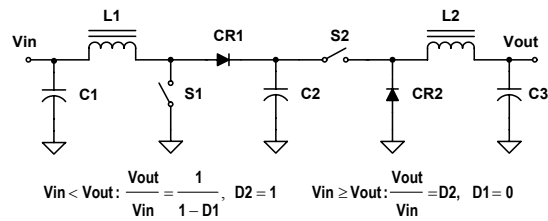


Figure 1. Boost + buck converter.

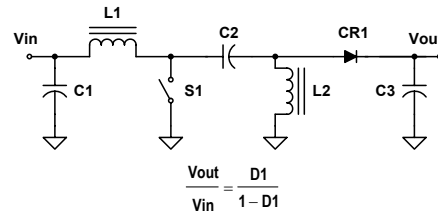


Figure 2. SEPIC.

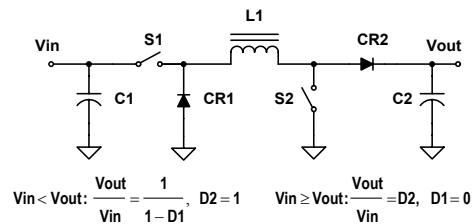


Figure 3. Buck + boost converter.

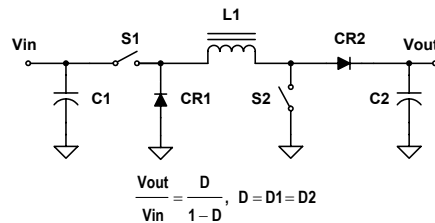


Figure 4. Buck + boost with D1 = D2.

CIRCUIT OPERATION

Figure 1 – boost + buck converter

The circuit of Figure 1, although the most complex of the four, has several advantages. Both the input current and output current are smoothed by inductors, minimizing the ripple current at the input and output terminals and minimizing the ripple current stress on capacitors C1 and C3. Nothing is free, however, as capacitor C2 has discontinuous current either from CR1 when $V_{in} < V_{out}$ or from S2 when $V_{in} > V_{out}$. It also, unlike the other three circuits, requires two inductors.

Although the circuit will work with both switches driven simultaneously (resulting in the same transfer equation as given in Figure 4), the most efficient control method is to drive S1 via pulse-width modulation (PWM) when the boost function is needed ($V_{in} < V_{out}$) while holding S2 on continuously, and to drive (via PWM) S2 when the buck function is needed ($V_{in} > V_{out}$) while holding S1 off. This is a very good scheme, because when $V_{in} = V_{out}$ no switched-mode power processing is needed. S1 is off, and S2 is on, and power is simply transferred from the input to the output in a dc circuit. Furthermore, when the input is nearly equal to the output, a minimum of switched-mode power processing is required.

Figure 2 – SEPIC

The classic single-ended primary inductor converter (SEPIC) is shown in Figure 2. This is clearly the simplest circuit of the four in terms of the total number of parts, requiring only one switch and one diode. However, it does require two inductors (or an integrated one, with one core and two windings).

As evidenced in the transfer equation, When the duty ratio D1 equals 0.5, the input and output will be equal, and the entire power being transferred from input to output is processed in the switched mode. Furthermore, all power is transferred through the capacitor C2. This requires that C2 be chosen carefully for its ripple-current handling ability. It can be a low-impedance electrolytic type, and today there are some excellent choices available. Its terminal voltage is equal to the input voltage. This is obvious when one realizes that L1 is connected to the input and L2 is connected to ground, and the average voltage across an inductor must be zero. The SEPIC is, in the author's opinion, underutilized in the industry. This may be a result of its somewhat unorthodox configuration, requiring more analysis and thought on the part of the designer than the simple buck or boost circuits. See reference [2] for more details.

Figure 3 – buck + boost converter

A circuit that functions much like the one in Figure 1 is shown in Figure 3. In this case the buck section comes first, followed by the boost section, hence the name, "buck + boost," as opposed to "boost + buck." As will be shown later in this paper, it is the most efficient one when the input voltage is close to the output voltage. When $V_{in} = V_{out}$, no switched-mode processing is required; S1 is on, and S2 is off. Another advantage is that it requires only one inductor. The disadvantage is that both the input current and output current are discontinuous, so the input and output capacitors must be chosen to handle the ripple currents. As in the circuit of Figure 1, when V_{in} is less than V_{out} , S1 is held on, while S2 functions as a PWM boost converter. When V_{in} is greater than V_{out} , S1 functions as a PWM buck converter, while S2 is held off.

Figure 4 – buck + boost again, but D1 = D2

This circuit configuration is identical to the one in Figure 3, but the operation is entirely different. In this case, switches S1 and S2 are both driven from the same controller, such that they are both on at the same time and off at the same time. The advantage, of course, is that the controller is much simpler than the one required for Figures 1 and 3. It is more complex than the SEPIC controller, because two switches must be driven, and only one of them is based at ground potential.

There are several IC controllers on the market that are well-suited for this circuit. An example is given in Reference [3].

The simplicity of the drive scheme is the advantage of this circuit, but its disadvantage of poor efficiency often deters its usage. Because of the simultaneous drive to the two switches and the fact that when the input voltage equals the output voltage the duty ratio D is 50%, excessive energy is circulated within the converter. For example, when $V_{in} = V_{out}$ (and $D = 50\%$), the inductor L1 conducts twice the input (and output) current. This is obvious by inspection. At the input, S1 is on for 50% of the time, forcing it to conduct twice the average input current. This current is, of course, coming from L1. Similarly, at the output, CR2 conducts 50% of the time, again getting its current from the inductor. It is also true that all four switching components (S1, CR1, S2 and CR2) conduct twice the input – output current when they are conducting. The result is excessive power losses, making this circuit the "inefficiency champion" of the four circuits. It is, however, undeniably simple and a candidate for low-current applications.

CIRCUIT SIMULATIONS

Component choices

The four circuits were simulated using the loss characteristics of a set of components suitable for a converter with an output of 24 V dc at 2 A, and an input range of 18 to 44 V dc. These parameters were entered into a spread sheet, along with expressions for the currents and voltages present. Then, the results were plotted to show the comparisons. The operating frequency is 100 kHz. In the case of the switches S1 and S2, the ground-based switch was an N-channel FET, and the elevated one was a P-channel FET. The diodes are Schottky types, with an assumed forward voltage of 0.6 V. The inductors are 150 uH, 4 A ones with an internal resistance of 0.1 ohm. The capacitors are high-quality, low-impedance types, but their losses were calculated and shown to be negligible. Switching losses of the FETs were approximated, assuming the switching time of 100 ns. Switching losses of the diodes were neglected. Control circuit losses were assumed negligible.

The FET characteristics are as follows:

P-channel:

ON Semi. MTD5P06V, $R_{DS(on)} = 0.45 \Omega$

N-channel:

ON Semi. NTD15N06, $R_{DS(on)} = 0.09 \Omega$

The inductor value of 150 uH was chosen to result in ripple current of approximately 20% in the inductors and other components, allowing one to neglect the "tilt" in the current waveforms and treat them as if they were flat-top pulses of current.

Loss calculations

Spread sheets were developed for each of the four circuits, calculating the performance at 2-volt intervals of input voltage with the output of 24 V at 2 A. In the case of the SEPIC and the circuit of Figure 4 ($D1 = D2$), the process was simplified by the fact that the transfer function (V_{out} / V_{in}) is the same when the input voltage is below or above the output voltage. In the other two circuits, separate equations were applied, depending on whether the input was less than or greater than the output.

Because the conduction losses in the FETs are resistive, the currents during conduction were calculated, squared, and multiplied by the resistance, then multiplied by the conduction duty ratio (D), to arrive at the average loss over the switching period. The transfer functions given at the bottom of Figures 1 through 4 were used to determine the operating conditions on

each of the components (with careful analysis of the operational details of each circuit).

Sample calculations

The entire set of equations is too long to include in this paper, but here is a sample from the 18 V input case of the circuit of Figure 1.

$$\begin{aligned}
 V_{in} &= 18 \\
 I_{in} &= (V_{out} \cdot I_{out}) / V_{in} \\
 D1 &= (V_{out} - V_{in}) / V_{out} \\
 D2 &= 1 \quad (\text{circuit is operating in the boost mode.}) \\
 I_{L1} &= I_{in} \\
 I_{S1 ON} &= I_{in} \\
 I_{S1 AVE.} &= I_{in} \cdot D1 \\
 I_{S2 ON} &= I_{out} \\
 I_{S2 AVE.} &= I_{out} \\
 I_{CR1 ON} &= I_{in} \\
 I_{CR1 AVE} &= I_{in} \cdot (1 - D1) \\
 I_{CR2} &= 0 \\
 I_{L2} &= I_{out} \\
 P_{CR1} &= V_f \cdot I_{CR1 AVE} \\
 P_{CR2} &= 0 \\
 P_{L1} &= I_{in}^2 \cdot 0.1 \\
 P_{L2} &= I_{out}^2 \cdot 0.1 \\
 P_{S1 dc} &= I_{S1 ON}^2 \cdot R_{DS(on)} \cdot D1 \\
 P_{S1 ac} &= V_{out} \cdot I_{L1} \cdot 0.01 \\
 &\quad (100 \text{ ns} / 2 \cdot 2 \cdot 100 \text{ kHz} = 0.01) \\
 P_{S2 dc} &= I_{S2 ON}^2 \cdot R_{DS(on)} \cdot D2 \\
 P_{S2 ac} &= 0 \\
 P_{dc} &= P_{CR1} + P_{CR2} + P_{L1} + P_{L2} + P_{S1 dc} + P_{S2 dc} \\
 P_{ac} &= P_{S1 ac} + P_{S2 ac} \\
 P_{total} &= P_{dc} + P_{ac}
 \end{aligned}$$

$$\text{Efficiency} = V_{out} \cdot I_{out} / (V_{out} \cdot I_{out} + P_{total})$$

The above equations apply when V_{in} is less than or equal to V_{out} , since the converter is operating in the boost mode, with the buck function disabled by holding S2 on continuously.

PERFORMANCE OF THE CIRCUITS

Figure 5 shows the performance of the four circuits. Note the superior performance of the two bimodal circuits, especially their efficiency when the input voltage is nearly equal to the output voltage (24 V). The SEPIC, while quite efficient also, is no better with its input near the output voltage. It simply becomes more efficient as the input voltage increases, due to the decrease in input current. Also note the relatively poor efficiency of the buck + boost circuit with the switches driven simultaneously (D1 = D2).

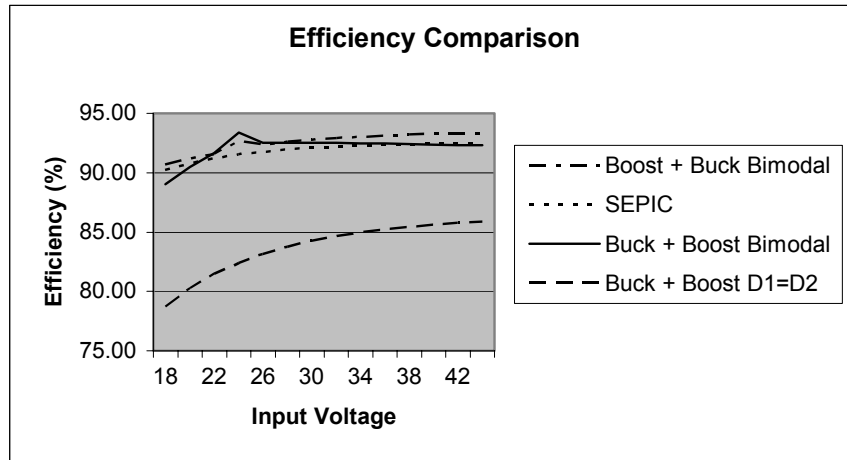


Figure 5. Efficiencies of the four circuits at 24 V, 2 A output, over the input range of 18 to 44 V dc.

Figure 6 shows the same data, but without the fourth circuit, so the vertical scale could be expanded to compare the first four circuits in more detail.

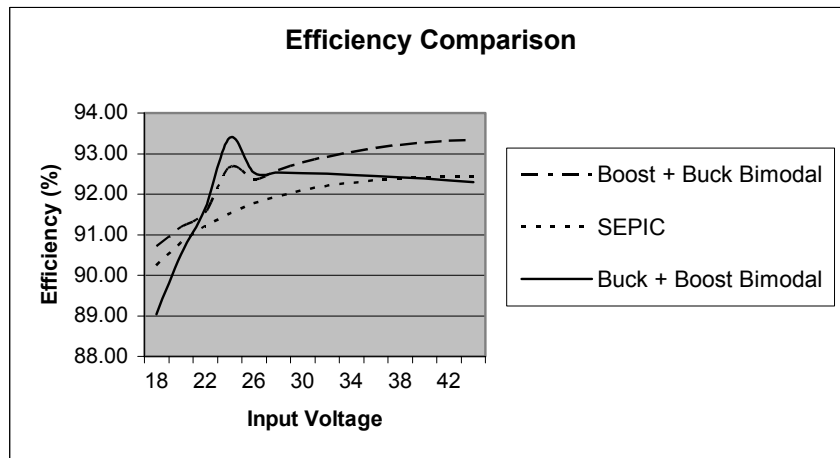


Figure 6. Efficiencies of the first three circuits at 24 V, 2 A output, over the input range of 18 to 44 V dc.

Note the better efficiency of the boost + buck bimodal converter when its input voltage is below and above the output voltage. This is attributable to the decreased component stress due to the smooth input current and output current. Although the center capacitor is subjected to ripple current, the effect is negligible, with today's low-impedance electrolytic capacitors.

MEASURED PERFORMANCE

Figure 8 shows measured performance of a buck + boost bimodal converter similar to that of Figure 3, with an output of 24 V at 2.4 A. Compare this to the graph in Figure 6 for the buck + boost bimodal converter.

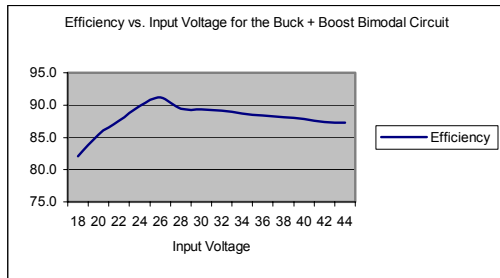


Figure 8. Buck + boost circuit efficiency (measured).

CONCLUSION

Performance of four sample circuits has been modelled, and laboratory test data shown for a prototype buck + boost bimodal converter. It has been shown that this circuit exhibits superior performance when the input voltage is nearly equal to the output voltage, while the boost + buck bimodal converter has superior performance over a wider input voltage range.

The SEPIC is a simpler circuit, with comparable, but not quite as efficient, performance. The buck + boost circuit with both switches driven simultaneously is simple to control (but not as simple as the SEPIC) and has inferior efficiency. References are provided for additional background of the circuits discussed.

REFERENCES

- [1] Ray Ridley, Siegfried Kern, Berthold Fuld, "Analysis and Design of a Wide Input Range Power Factor Correction Circuit for Three-Phase Applications," Proceedings of APEC 1993, pp. 299 – 305.
- [2] Mullett, Chuck, "DC-DC Converter for Driving High-Intensity Light-Emitting Diodes with the SEPIC Circuit," Application Note AND8138/D, available from ON Semiconductor (www.onsemi.com).
- [3] "A Unique Converter Configuration Provides Step Up/Down Functions," Application Note AN954, available from ON Semiconductor (www.onsemi.com).