RESIDUAL STRESS OF THIN FILMS OF POLYCRYSTALLINE AND AMORPHOUS SILICON

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The strong competitive conduct in IC industry forces the producers of the raw silicon wafers to the continuous price-cutting behavior. Therefore, projects leading to decreasing of the wafer unit cost are unavoidable in order to be able to compete. One of the most effective method leading to significant reduction of the unit cost of silicon wafer is decreasing of the wafer thickness. However, decreasing of the wafer thickness results in the excessive wafer warping if polycrystalline silicon layer is deposited on the wafer back side (Fig. 1).

This phenomenon is caused by high residual stress of the polycrystalline silicon layers. Knowledge of the dependences of the residual stress on the deposition conditions is than necessary for development of the process of deposition of the polycrystalline silicon layers allowing controlled wafer shaping.

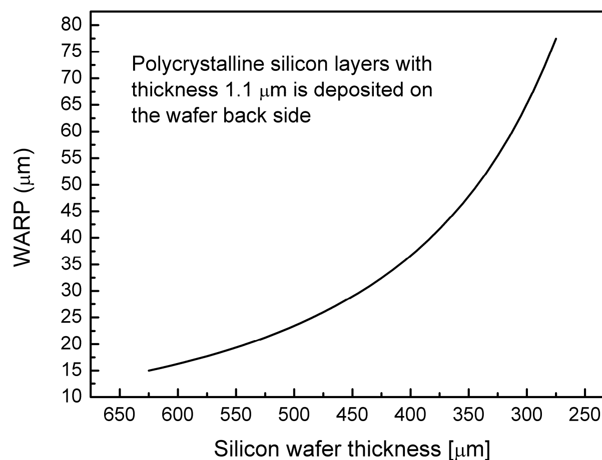

Fig. 1: Dependence of the silicon wafer warping on the thickness of the silicon wafer. Wafer warping is caused by polycrystalline silicon layer deposited on the wafer backside. WARP is parameter characterizing warping of the wafer [1].

LPCVD (Low Pressure Chemical Vapor Deposition) technique was used for deposition of the polycrystalline silicon layers on the wafer back side. The most important parameters of this technique are deposition temperature and deposition pressure.

Dependences of the residual stress of the polycrystalline silicon layers on the deposition temperature were measured for two constant deposition pressures 110 and 280 mTorr. The range of the deposition temperature was from 570 to 627°C. Deposition temperatures below 600°C were taken intentionally in order to get amorphous silicon layers. The thickness of the layers was 1.1 μm. Residual stress of the polycrystalline silicon layer σ_f was calculated from the curvature radius R of the wafer using Stoney's equation:

$$\sigma_f = \frac{E}{6(1-\nu)} \cdot \frac{t_s^2}{t_f} \cdot \left(\frac{1}{R} - \frac{1}{R_0} \right) \quad (1)$$

where E is Young's modulus, ν is Poisson's ratio, t_s is thickness of the silicon wafer and t_f is thickness of the layer.

From the dependences of the residual stress on deposition temperature (Fig. 2) is evident that layers deposited at temperatures above 600°C for deposition pressure 280 mTorr as well as layers deposited above 580°C for deposition pressure 110 mTorr induce compressive residual stress. Compressive stress is denoted by the negative sign. Those layers (right from the grey areas in Fig. 2) are polycrystalline. Compressive stress of the polycrystalline silicon layers is the consequence of Vollmer – Weber mode of thin film growth. Residual stress of the polycrystalline silicon layers decreases with increasing deposition temperature.

Layers deposited below 580°C for deposition pressure 280 mTorr are amorphous and induce compressive residual stress. Layers deposited below 585°C for deposition pressure 110 mTorr are amorphous and induce tensile residual stress (denoted by the positive sign). Layer deposited at 585°C and 280 mTorr is amorphous and induces tensile residual stress as well. Tensile stress of the amorphous layers is a result of the partial crystallization of the amorphous layer during its deposition. Crystallization of amorphous silicon is followed by volume contraction of the layer which results in tensile stress.

Resolutions whether layer is polycrystalline or amorphous were done using SEM and is reported elsewhere [2].

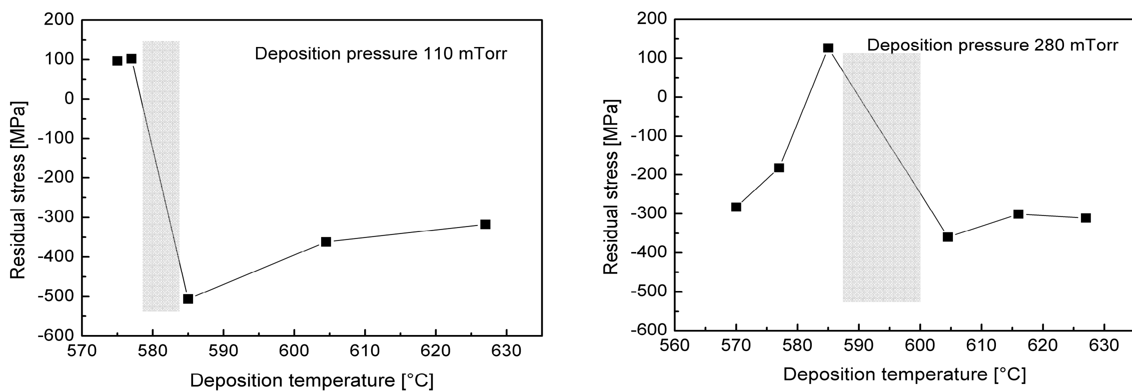

Fig. 2: Residual stress of the amorphous and polycrystalline silicon layers deposited on the backside of the silicon wafer. On the left side from the grey areas were layers amorphous. Grey areas denote transition region between amorphous and polycrystalline silicon. Polycrystalline layers are right from the grey area.

[1] MF657, *Standard Test Method for Measuring Warp and Total Thickness Variation on Silicon Slices and Wafers by a Non-contact Scaning Method*, Semiconductor Equipment and Materials International (SEMI) 2007.

[2] D. Lysáček, *Thin films of polycrystalline silicon*, Doctoral thesis, Brno University of Technology, 2010.