ON Semiconductor Utilizes Questa OVM for Efficient Functional Verification of System-Based Chips

Mentor's Questa® mix-language simulator and Open Verification Methodology (OVM) library accelerated the adoption and successful application of automated constraint-driven stimuli generation and coverage data collection. With these advanced verification technologies, ON Semiconductor reached 100 percent functional coverage cut testbench development time in half, and delivered a high quality SoC on time.

ON Semiconductor™ is a leader in power efficient semiconductor solutions for a wide range of markets. The company's broad portfolio of products includes power, analog, DSP, mixed-signal, advance logic, clock management, and standard component devices.

While the company's corporate headquarters is located in Phoenix, Arizona, it operates a worldwide network of manufacturing facilities, sales offices, and design centers in key markets throughout North America, the Asia Pacific regions, Europe, and the Middle East.

The company's Automotive Power Group division in Brno, Czech Republic, produces high-performance, power efficient, system-on-chips (SoCs) with best-in-class EMC and ESD automotive requirements. These SoCs utilize top-in-class Intellectual Property (IP) ranging from in-vehicle network (IVN) standalone transceiver IP (CAN, LIN, Flexray) and power switching IP, to precise regulator and DC/DC converter IP, along with the integration of analog and digital processing of various sensor interface signals. Recently, ON Semiconductor successfully designed a new mixed-signal, multi-function SoC within a tight six-month timeframe.

Like so many other leading-edge design shops, ON Semiconductor's Brno team faced the daunting challenge of not only designing this complex, multi-function chip but also adopting more reliable and sophisticated technologies to verify it. There is no room for error in today's highly competitive automotive market.

The ON Semiconductor digital design team wanted to adopt a coverage driven verification (CDV) methodology to increase verification productivity and quality. However, CDV was not supported by VHDL (their digital design language), so they wanted to adopt SystemVerilog for its built-in functional coverage features and assertions mechanism (SVA).

As a long-standing Mentor customer, the ON Semiconductor team was already familiar with Questa's CDV support and the benefits of using the Advanced Verification Methodology (AVM). So, they decided to stick with Questa for their mixed-language simulation and migrate to the OVM as the basis for their top-level testbench. Questa and the OVM provided automated, constraint-driven generation of stimuli and coverage data collection,

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Hubert Pierscinski
Digital Project Leader
ON Semiconductor

Hubert Pierscinski and Petr Tichy of ON Semiconductor.

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enabling ON Semiconductor to achieve 100 percent functional coverage and build a more sophisticated testbench in half the time it took to build their previous, directed test environments.

Building a Better Verification Environment

The new ON Semiconductor design integrated onto a single chip several functional blocks that typically existed on six separate chips. The main functional blocks included regulators, transceivers, and a system watchdog. Combining all of these functions onto a single SoC, as opposed to separate components, significantly lowers the cost of the full solution. Also, this integration provides their customers with a better quality level (sub ppm defect level), lower power consumption, and reduced PCB footprint.

This high voltage (80 V) SoC serves as a gateway for communication between the control unit and other devices in the in-vehicle network (IVN), interfacing between several standard communication buses. The ON Semiconductor team had to design and verify this complex mixed-signal SoC within only six months with the expectation of delivering error-free silicon on the first pass.

On the digital side of this mixed-signal device, the burden of this task fell on the shoulders of the three person team at ON Semiconductor: Digital Project Leader Hubert Pierscinski, Verification Specialist Petr Tichy, and Digital Group Leader Marek Hustava.

"Our chief motivation was a reduction of effort and time," recalls Hustava. "We also thought we could increase design quality if we were able to report directly from the tool when we reached 100 percent functional coverage."

The ON Semiconductor team saw CDV as the most effective way to fulfill these goals. They had tried doing this with automated checkers, but writing them in pure VHDL was extremely complex and took too much time. System Verilog Assertions (SVA) and cover groups allowed them to get the information they needed concerning functional coverage.

"With assertion-based CDV this was quite easy," said Tichy. "It was easy to review if the assertion is doing what it was originally proposed to do."

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ON Semiconductor

To speed adoption and facilitate the use of this new language, they needed a non-proprietary methodology. Because of their previous good experience using AVM, it was logical for them to adopt the OVM. The OVM provided them with ready-made, proven foundations for complex testbenches that could be easily modified, expanded and reused.

"The OVM allowed us to implement the best-practices SystemVerilog verification methodology," explained Pierscinski, "thus minimizing the time needed for adoption of CDV on our designs."

Responsive customer support meant they were able to quickly solve issues related to the application of new methodologies and beta releases. Mentor also provided an on-site OVM workshop and was helpful during the investigation of issues they faced during the application of OVM on their project.

"Mentor's customer support gave us efficient planning for OVM," said Tichy. "But a more frequent benefit was that each time we had a question concerning simulator performance or the OVM, Mentor was responsive and we always got the answer to our question fast."

Specification Driven Verification

The resulting verification flow consisted of automated, constraint-driven stimuli generation, using the high-performance constraint solver in Questa, and validation of correctness of the implementation using SVA.

The OVM supports specification driven verification. Early in the design process, an exhaustive specification of the SoC was defined — the complete system analyzed in detail and the best implementation and test strategy selected. The design specification was analyzed to extract use cases systematically and exhaustively to form verification scenarios. Each hardware requirement was described using an SVA (if applicable) or cover group and tagged with a unique identifier that is easily traceable in the simulation transcript, coverage matrix, and verification test plan. Based on the specification captured in the SVA, the verification test plan was prepared by the digital verification engineer.

Questa automatically generates stimuli based on the defined constraints, and the constraints are updated based on the coverage results. The OVM test bench environment uses cover groups (named assertions) to collect coverage data during verification. Assertions are used for the validation of the correctness of the implementation and can be combined with automated checkers.

Automated linking of Excel with Questa binds the verification test plan with the coverage results - allowing the team to easily generate customizable verification status reports.

"What is really useful in Questa is that we can directly link the Excel spreadsheet with data imported from the Questa Unified Coverage DataBase," explained Pierscinski. "In this way, we generated a useful table for functional coverage reports. This was beneficial for us because we could see whether specific assertions were covered in the simulation or not - then, based on our verification test plan, automatically generate the coverage report."

Creating Confidence and Time

The ON Semiconductor team found the OVM testbench to be easy to reuse, reliable, and efficient, saving them effort and cost.

"With OVM we were able to prepare the testbench two times faster than the traditional way," Pierscinski estimated. "Questa and OVM provided us with the SystemVerilog CDV solution, which fit all of our needs, and helped us reduce the effort needed to develop the verification environment and stimuli."

According to Tichy, "The OVM let us make a visible step towards efficient functional verification. It proved its strength and flexibility for testing our transceiver chips. The TLM-based, constraint-driven stimuli mechanism enabled us to test virtually an infinite number of input combinations in a reasonable time."

In other words, by starting with the OVM testbench, through reuse and coverage driven verification, ON Semiconductor was able to shorten their overall verification cycle while maintaining excellent quality.

"It shortened the cycle in part because there was good user documentation for the OVM," said Pierscinski. "The testbench architecture was provided in the documentation. So we didn't need to spend time thinking of how to implement simulator checkers and so on. You could focus on functional coverage, as opposed to building these modules that are already available, and in this way gain time."

Because 100 percent functional coverage was reached in digital verification, the verification team was able to confidently identify all issues prior to mix-signal simulation. Therefore, it was no surprise that during mix-signal simulation no digital issues were detected. This significantly reduced the overall design and verification time.

"We were sure that the only issues we were targeting during mixed-signal verification were on the interconnects between the digital and analog," said Hustava. "If you find a problem, you do not need to verify the digital part of the design because you are already 100 percent confident that it is fully covered."

Using OVM methodology, ON Semiconductor has been able to produce a high quality IC in a significantly shorter timeframe compared to a traditional digital design and verification methodology.

"Using the OVM, we were able to produce a high-quality IC in a visibly shorter time in comparison to a traditional digital design and verification methodology."

Petr Tichy
Verification Specialist
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