A Novel Hysteretic Control Circuit

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Abstract

The use of hysteretic control for current regulators is very applicable to LED drivers. It is easy to sense the current in the FET but this is comprised of only the positive ramp. The FET current waveform makes it simple to turn the switch off at the correct peak value of drain current; however, the information from the negative ramp is not available in the path of the FET. This paper examines a novel method of synthesizing the information from the positive ramp, to determine the correct off-time required to hold the valley current constant. This technique allows for a simple integrated circuit to be manufactured with all of the advantages of hysteretic control, and a very simple current sensing circuit.

Background

Current high-intensity LEDs require between 350 and 750 mA for optimum brightness. Devices requiring well over an amp are being designed and will be on the market shortly. LEDs require a constant current source for reliable operation. As current levels increase, linear regulators no longer offer the required efficiency for such systems. Switching regulators offer better efficiency over a wide operating range of input voltage.

A low cost converter would require minimal external components and good current regulation. One obvious solution for the control circuit is a hysteretic control system. This type of control offers good regulation and transient response over a wide range of input and output voltages. While fast transient response is not critical for many applications, there are some systems that need to deal with fast changes of the input voltage, or that switch some combination of the load LEDs on and off.

For a true hysteretic controller, the inductor current must be sensed so that the peak and valley current levels are available to the control loop. Unfortunately this would require a complicated current sensing circuit to measure the dc inductor current and level shift it to a ground referenced signal that can be fed into the controller.

Sensing the current in the FET path is simple and inexpensive and can be accomplished with a resistive current shunt. To further reduce system cost, a SENSEFET™ can be used for the switch which allows for an inexpensive chip resistor to sense the current rather than a low impedance, power resistor.

Problem

The hysteretic control circuit turns the switch off when the current reaches the upper limit point and back on when it reaches the lower limit point. For turn off, sensing the current in the FET works well. It can be seen from the current waveforms in Figure 1,

that the peak current is available in the switch waveform. When the current reaches a pre-determined level the switch will turn off and the inductor current will ramp down. When the negative ramp reaches the lower level, the controller should turn the switch on. If the switch current is being sensed, the current level is not known once the switch is turned off, until it is turned back on. This is the inherent problem with this combination of this topology and control circuit.

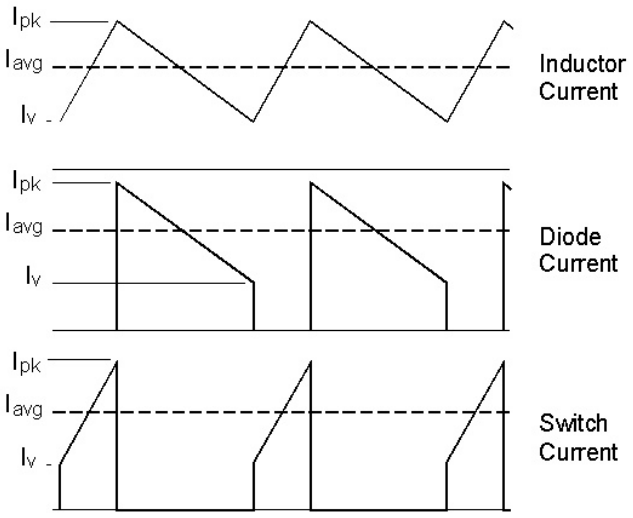

Figure 1. Current Waveforms for a Buck Converter

Solution

One solution is to use a timing circuit that determines the off time of the switch that would be required to turn the switch back on at the desired current level. For this circuit a capacitor will be used to store a dc level that will determine the off time. Such a circuit is shown in Figure 2.

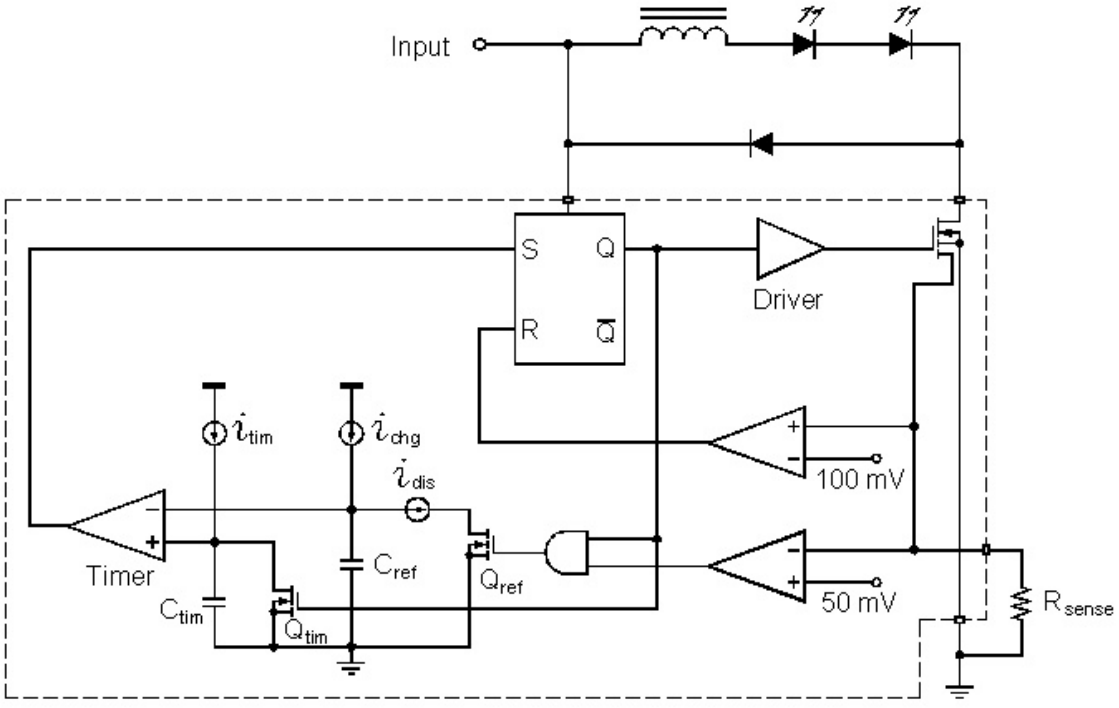

Figure 2. Hysteretic Control Circuit with Off Time Calculation

The heart of this solution is a variable timer which includes a feedback loop to determine the correct off time. The timing circuit turns on FET Q_{tim} while the power switch is on. This discharges capacitor C_{tim}. When the switch turns off, the gate to Q_{tim} goes low and C_{tim} begins to charge. When its level reaches that of C_{ref}, the timer comparator changes state and sends a logic high signal to the set input of the flip-flop, which turns on the power switch.

The reference signal determines the off time of the switch. This capacitor is constantly being charged at a rate of i_{chg}. In steady state operation, it must be discharged such that the magnitude of the discharge voltage ramp is equal to that of the charge voltage ramp. Discharge occurs when the FET is on and the level of the current is below the preset level. For this example, the peak current must correspond to a 100 mV reference and the valley current must correspond to a 50 mV reference. This means that the valley current is 50% of the level of the peak current.

The discharge current should be much greater than the charging current for the reference capacitor. This is because during the discharge period, the inductor current is below the 50% level, which causes some error in the average current. A short discharge pulse will minimize that time that the current is below the desired valley level, which results in tight regulation.

The time constant for the reference circuit should be much greater than the one for the timing circuit. The reference signal should approximate a dc level, while the timing circuit needs to ramp from zero volts, to the reference level on each cycle. Typical waveforms are shown in figure 3.

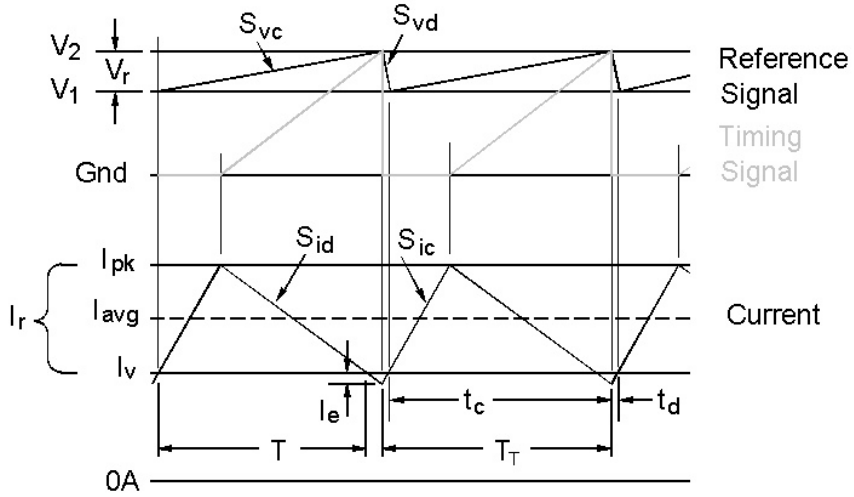

Figure 4. Current and Timing Waveforms

The feedback portion of this circuit works much like a linear, analog feedback loop. When off time loop has an effective 180° phase shift that adjusts the off time for the correct valley current. When the valley current is less than the desired level and the switch is on, the reference voltage is reduced. The lower reference voltage reduces the off time on the following cycle. The shortened off time gives the negative current ramp

less time to fall and the valley current is higher on the next cycle. If the loop is stable, the timer will find the correct off time after a few cycles and the current will be in regulation.

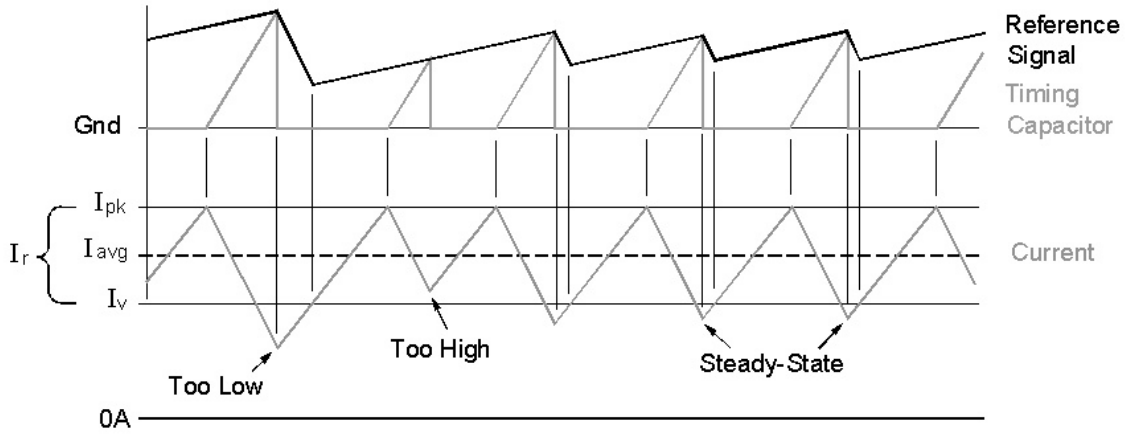

Figure 5. Transient Response of Timer Waveforms

Loop Characteristics

The off-time circuit is a negative feedback loop and has a gain and stability criteria just like a linear analog feedback circuit.

Gain

The gain of this circuit is dependant on the rising and falling slopes of the reference signal. It has been shown that the valley current must be below the theoretical valley level for some period of time, since this is when the reference signal discharges and therefore corrects its average level. The shorter the discharge time is, the less time that is required for the current to be below the theoretical valley level and less time below the theoretical valley level translates to less error current (Ie) as shown in figure 4.

This implies that a slow charge rate and fast discharge rate result in low error current. A slow charge rate will result in a small value of voltage change in the reference signal, and a fast discharge rate will reduce the amount of time required to bring the reference voltage back to its level at the beginning of the cycle.

The following analysis refers to the waveforms in figure 4. T is the ideal period for the circuit with no error. T_T is the total period with the error current included to drive the reset timing circuit.

Timing Circuit:

$$S_{vc} = \frac{dv_c}{dt} = \frac{i_{ch}}{C_{ref}}$$

$$S_{vd} = \frac{dv_d}{dt} = \frac{i_{dis}}{C_{ref}}$$

For steady-state $dv_d = dv_c$, so: $dv_d = S_{vd} \cdot t_d = dv_c = S_{vc} \cdot t_c$

$$S_{vd} \cdot t_d = S_{vc} \cdot (T_T - t_d) = S_{vc} \cdot T_T - S_{vc} \cdot t_d$$

$$(S_{vd} + S_{vc}) \cdot t_d = S_{vc} \cdot T_T$$

$$t_d = \frac{T_T \cdot S_{vc}}{S_{vc} + S_{vd}}$$

Current Ramp:

$$t_{on} = \frac{I_r}{S_{ic}} = I_r / \left(\frac{V_{in} - V_L}{L} \right) = \frac{I_r \cdot L}{V_{in} - V_L}$$

$$t_{off} = \frac{I_r}{S_{id}} = I_r / \left(\frac{V_L}{L} \right) = \frac{I_r \cdot L}{V_L}$$

$$T = t_{on} + t_{off} = \frac{I_r \cdot L}{V_{in} - V_L} + \frac{I_r \cdot L}{V_L} = \frac{I_r \cdot L \cdot V_L}{V_L (V_{in} - V_L)} + \frac{I_r \cdot L \cdot (V_{in} - V_L)}{V_L (V_{in} - V_L)}$$

$$T = \frac{I_r \cdot L \cdot (V_L + (V_{in} - V_L))}{V_L (V_{in} - V_L)}$$

$$\boxed{T = \frac{I_r \cdot L \cdot V_{in}}{V_L (V_{in} - V_L)}}$$ This is the theoretical period without the error included.

For the on time:

$$I_r = \frac{(V_{in} - V_L) \cdot t_{on}}{L}$$

$$\boxed{t_{on} = \frac{I_r \cdot L}{V_{in} - V_L}}$$

The error current can be expressed as:

$$I_e = t_d \cdot S_{ic} = t_d \cdot \frac{V_{in} - V_L}{L}$$

$$I_e = \frac{V_{in} - V_L}{L} \cdot \frac{T_T \cdot S_{vc}}{S_{vc} + S_{vd}} \cdot = \frac{V_{in} - V_L}{L} \cdot \frac{S_{vc}}{S_{vc} + S_{vd}} \cdot \frac{(I_r + I_e) \cdot L \cdot V_{in}}{V_L (V_{in} - V_L)}$$ (Ie has been added to the ramp current of the ideal current ramp.)

$$\frac{I_e}{I_r + I_e} = \frac{V_{in} - V_L}{L} \cdot \frac{S_{vc}}{S_{vc} + S_{vd}} \cdot \frac{L \cdot V_{in}}{V_L (V_{in} - V_L)} = \frac{S_{vc} \cdot V_{in}}{(S_{vc} + S_{vd}) \cdot V_L}$$

$$\frac{I_r + I_e}{I_e} = \frac{I_r}{I_e} + \frac{I_e}{I_e} = \frac{I_r}{I_e} + 1 = \frac{(S_{vc} + S_{vd}) \cdot V_L}{S_{vc} \cdot V_{in}}$$

$$\frac{I_r}{I_e} = \frac{(S_{vc} + S_{vd}) \cdot V_L}{S_{vc} \cdot V_{in}} - \frac{S_{vc} \cdot V_{in}}{S_{vc} \cdot V_{in}} = \frac{(S_{vc} + S_{vd}) \cdot V_L - (S_{vc} \cdot V_{in})}{S_{vc} \cdot V_{in}}$$

$$I_e = \frac{S_{vc} \cdot V_{in} \cdot I_r}{(S_{vc} + S_{vd}) \cdot V_L - (S_{vc} \cdot V_{in})}$$ Replacing s with i/C for both the charging and discharging modes, yields:

$$I_e = \frac{i_{ch} \cdot V_{in} \cdot I_r}{(i_{ch} + i_{dis}) \cdot V_L - (i_{ch} \cdot V_{in})}$$

$$I_e = \frac{V_{in} \cdot I_r}{\left(1 + \frac{i_{dis}}{i_{ch}}\right) \cdot V_L - V_{in}}$$ or,

$$\boxed{\frac{I_e}{I_r} = \frac{1}{\left(1 + \frac{i_{dis}}{i_{ch}}\right) \cdot \frac{V_L}{V_{in}} - 1}}$$

This equation shows that a large value of i_{dis}/i_{chg} will yield a small ratio of I_e/I_r, which is equivalent to high gain (low error). While high gain results in better regulation, it also can make the circuit become unstable. It also necessitates a very fast discharge circuit, since the higher the gain, the shorter the discharge time. For example a ratio of 40 for the discharge and charge currents requires that the discharge time be 1/40 of the charge time. For 100 kHz operation, that means the discharge time is 10us/40 or 250 ns. A 250 ns response time is fairly easy to accomplish, but it should be noted that higher gains will require faster circuits.

For the above equations:

S_{vc} is the slope of the voltage for the charging ramp on the reference capacitor.
S_{vd} is the slope of the voltage for the discharging ramp on the reference capacitor.
i_{ch} is the charging current for the reference capacitor.
I_{dis} is the discharging current for the reference capacitor.
C_{ref} is the reference capacitor value.
T is the theoretical period of the switching waveform without the time of the error current included.
T_T is the total switching period of the switching waveform.
t_d is the time for the discharge current beginning when the power switch turns on and ending when the reset pulse is terminated.
I_r is the peak-to-peak ramp current in the LED.
I_e is the error current – that which is below the theoretical valley level.
t_{on} is the on time for the power switch.
t_{off} is the off time for the power switch.
V_{in} is the input voltage to the power circuit.
V_L is the voltage across the LED(s).
L is the value of the inductor in series with the LED(s).

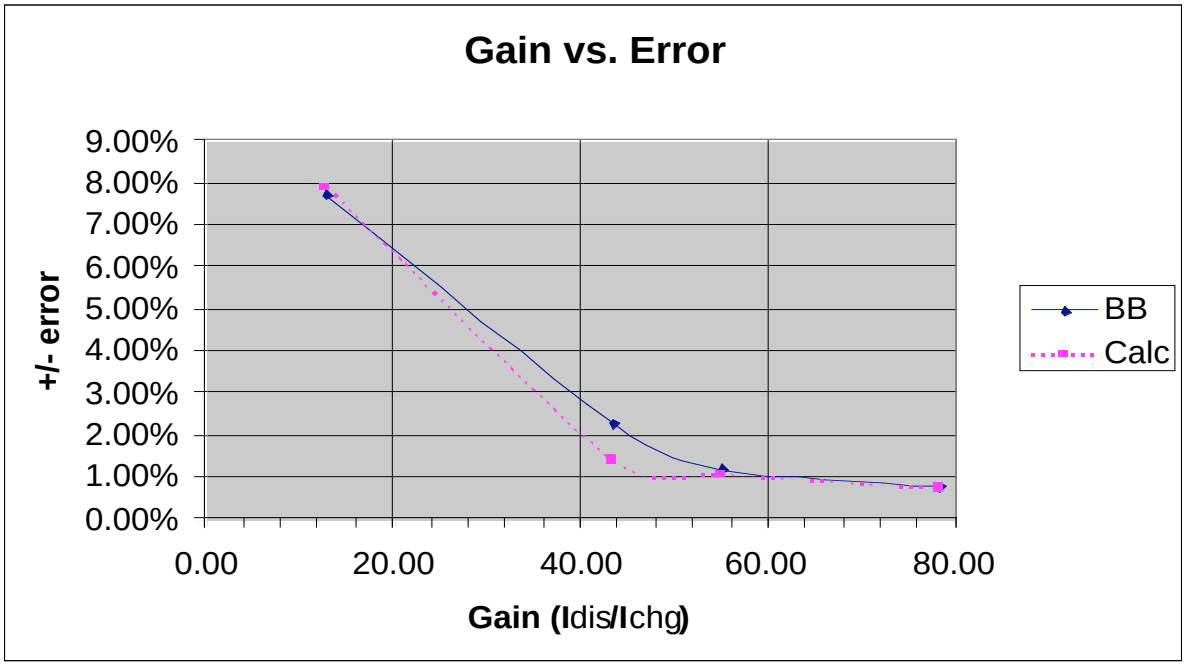

Figure 6. Gain vs. Regulation Error Data from Breadboard & Calculated. Input Voltage from 9 V to 18 V.

The calculated and breadboard data show good correlation other than a small amount of error at the gain of 43.

Transient Response

True hysteretic control has the fastest loop response of any control circuit. It operates to keep the controlled signal between two levels, an upper and lower level. If the controlled variable exceeds either level, the switch will either turn on or off until the variable reaches the opposite level. This is a nice feature of this type of controller.

In this implementation, the control is not pure hysteretic. When the current is increasing, it functions as a normal hysteretic control loop would, with a comparator which will turn off the switch as soon as the current reaches its maximum level.

In the other direction, the loop is not as simple. Since the off time is controlled by the timing circuit, the off time will be essentially the same as in the previous cycle, if the previous cycle was correct. As soon as one cycle occurs with a significant amount of error, the timing circuit will begin to correct. If the off time needs to be reduced, it will correct faster since the downward slope of the reference signal is very fast as compared to the upward slope. If the off time needs to increase, the reference signal can only move as fast as the upward slope with no reset pulse.

Even with the slow rising charging slope, the transient response has been shown to be quite good for line and load changes. The gain of the circuit and value of the reference capacitor have direct influences on the speed of recovery. The following waveforms were taken from a breadboard of this circuit. It has an I_{chg}/I_{dis} ratio of 43.

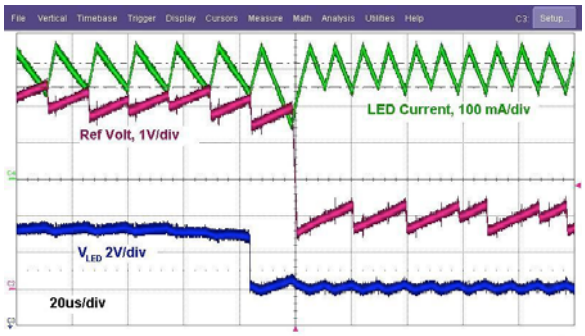

Figure 7. 1 LED to 2, Load Transient

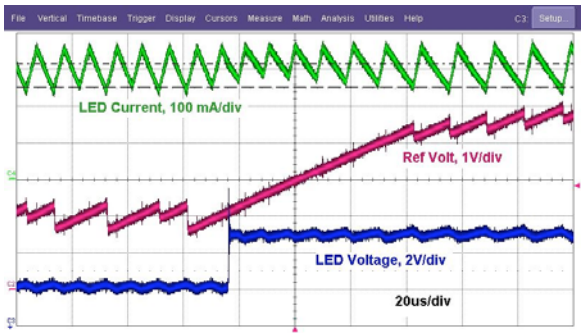

Figure 8. 2 LEDs to 1, Load Transient

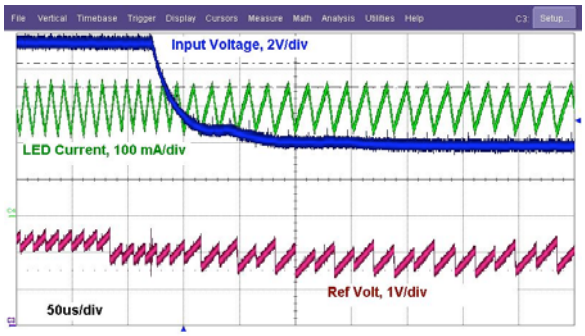

Figure 9. 16 to 9 V, Line Transient

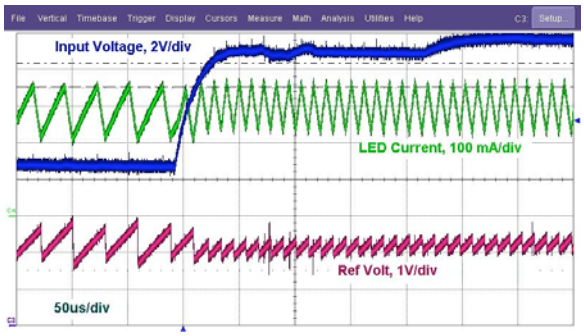

Figure 10. 9 to 16 V, Line Transient

It can be seen from the above photos that the transient response time varies from 1 to several cycles. In all cases there is only a minimal change in the average current and there was no perceptible difference in the light intensity of the LEDs during the transient event.

Stability

Similar to a standard analog loop, this loop can also become unstable. This phenomenon has been seen in various models and in the early chips that were designed. It has become apparent that the charging rate of the reference capacitor is a fundamental parameter that determines the stability of this circuit. A larger capacitor slows the charge rate and reduces any error that may occur in a given cycle, therefore making the circuit more stable. At the same time, it slows down the speed of response when the off time needs to increase. This is as would be expected – a slower loop is more stable.

At this time there are no equations available to define the parameters for a stable loop. This control circuit has been modeled in several versions of SPICE; a model exists in Excel and a physical breadboard has been made. There is some agreement will all of these sources of data, but none function exactly alike. The plots in figures 11 through 13 show the voltage on the reference capacitor (upper trace) and the LED current (lower trace) for both stable and unstable combinations of bias components.

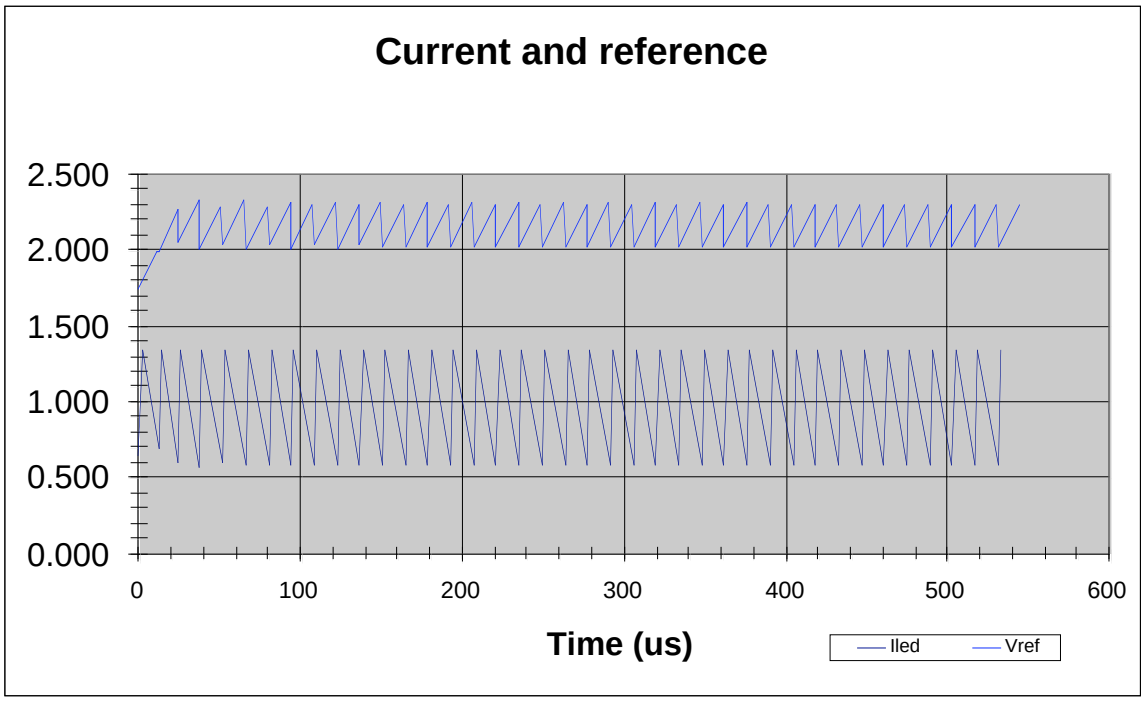

Figure 11. Stable Operation.

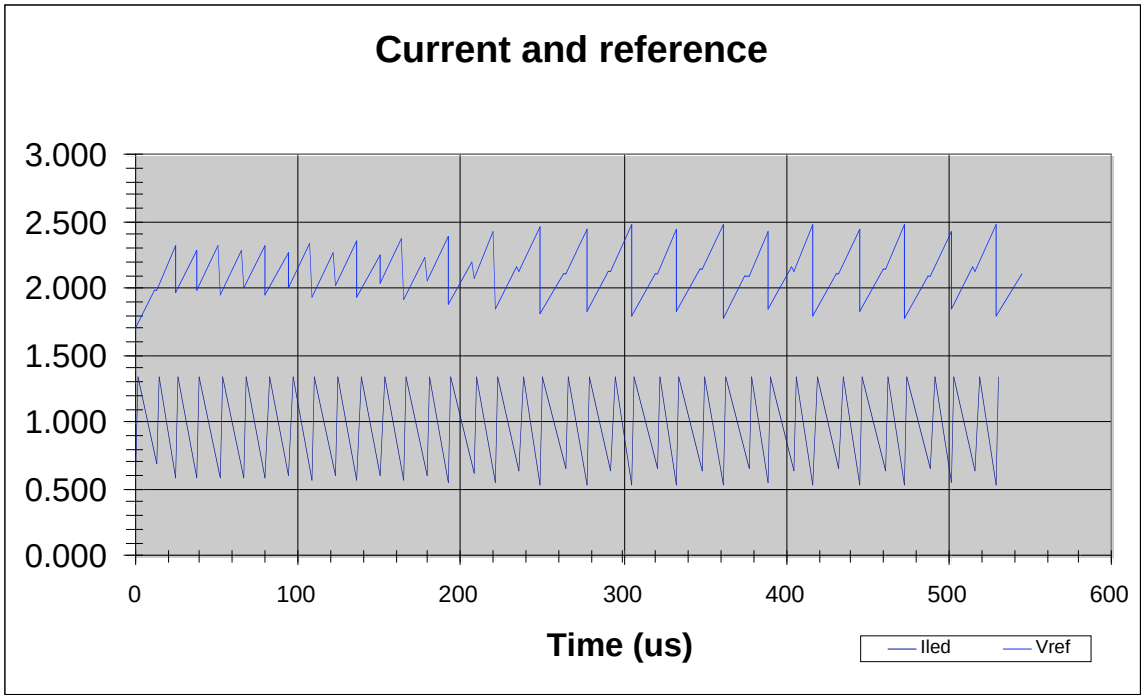

Figure 12. Marginally Stable Operation.

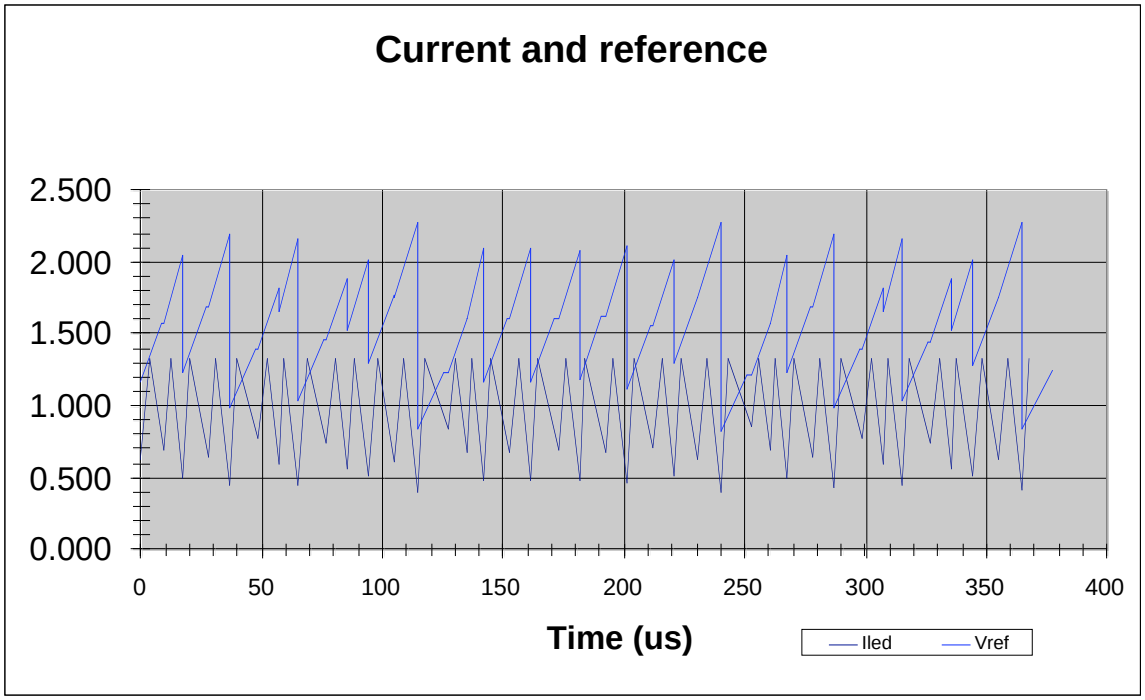

Figure 11. Unstable Operation.

All of the parameters for the above plots are the same except for the size of the reference capacitor. As that capacitor value is increased the circuit becomes more stable.

Conclusion:

It has been shown that this circuit has some of the features of a conventional hysteretic control loop but with some of the issues of a linear loop. There are many similarities to a closed loop feedback system. The gain of the device is dependent on the ratio of the charge and discharge current of the reference capacitor. As the gain increases, the regulation improves, however; the circuit becomes more difficult to stabilize. Increasing the size of the reference capacitor makes the loop more stable but increases the response time to transients.

This circuit offers a very simple implementation for constant current loads such as LED drivers. It uses a minimum of external components and does not require external loop compensation.