Physically Robust Interconnect Design in CUP Bond Pads

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Abstract

Economic challenges for small size IC design and manufacturing require: reduced die size without adding layers or other costs, bonding with Cu wire instead of Au wire, and maintained or improved reliability. Die size shrinking involves extensive use of circuit under pad (CUP) or bond over active circuitry (BOAC) on IC's having at least two levels of metal. CUP however, introduces more potential failure modes just as increased probe touchdowns at wafer probe and Cu wire bonding are harsher to the pad and underlying structures. Dielectric cracks under the pad may be more hazardous with circuitry present in the pad sub-layers. In short, bond pad cracks must be prevented while still lowering product cost by routing interconnect circuitry in all pad sub-layer metallization layers. Recommendations for improvement in both CUP and Cu wire bonding in published literature are inadequate for many products. This paper summarizes extensive experimental work and demonstrates practical solutions for improving product yield and reliability issues of bond pads consisting of two or more layers of Al interconnect metallization in SiO_2 dielectric. Qualitative CUP layout guidelines are developed for successful crack prevention, using the layout of the CUP circuitry itself to strengthen the pad. Al deformation and SiO_2 bending and cracking that would ordinarily be caused by harsh wafer probe or harsh wire bond are prevented, facilitating Cu wire bonding on CUP designs in current and future products. (This work presented previously [1]).

Key words: wafer probe, bond pad, wirebond, cracking, circuit under pad, bond over active circuitry

Introduction

The increasing need to reduce integrated circuit (IC) die size and manufacturing cost while increasing reliability presents challenges for bond pad design and manufacturing. Circuit under pad (CUP) is required (also called bond over active circuitry (BOAC)). Copper (Cu) wirebond needs to replace gold (Au) wirebond for lower cost. Pad cracks are a primary concern in this development because cracks mechanically weaken the bond and may cause leakage or shorts between CUP electrical nodes. But some new products may require up to 6 wafer probings, increasing the likelihood of pad cracks. And Cu wirebond requires more ultrasonic energy to bond to the aluminum (Al) alloy pad, further increasing stress to pad sub-layers and greatly increasing the likelihood of cracking. A further challenge is that the pad Al must remain thin for smallest die size and lowest manufacturing cost, so that no process changes, additional steps or materials costs are required.

Previous work by our group reported on the cracking weakness of "traditional" bond pad structures in Al based metallization and silicon dioxide (SiO_2) dielectric, with full sheets of metal in each level connected electrically by tungsten (W) vias. The top SiO_2 dielectric was found to crack easily at wafer probe. Top vias in the probe region enhance the top SiO_2 cracks, which tend to propagate from via to via, and promote "lifting barrier" issues. Pad cracking from harsh probing can be reduced by increasing the pad Al thickness [2,3]. Figure 1 illustrates a traditional pad structure.

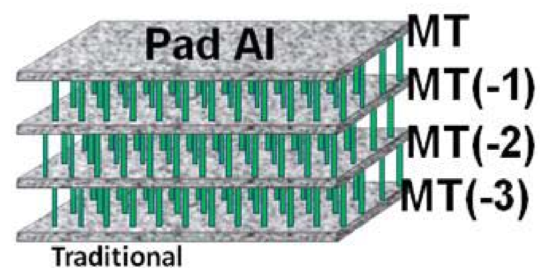

Figure 1. Illustration in concept of a traditional bond pad structure, 4 levels of Al-based metallization in this example. W vias electrically connect the full sheets of metal through SiO_2 dielectric that encases everything except the Pad Al surface at the top.

Traditional pads also crack easily at wirebond. Various pad structures simulating potential CUP designs were evaluated using both harsh probing and harsh bonding techniques and results compared to those of traditional pads [4,5].

Issues with pad cracks: Pad cracks can initiate in wafer probe, in wirebond, and in packaging processes. A crack that began in wafer probe may expand and propagate in wirebond, and may further worsen during packaging and potentially during product use. Al migration into the crack leading from electrical leakage to a short is a further issue in CUP pads. Crack initiation must be prevented in probe, wirebond, and packaging operations for high reliability products.

The typical method for observing pad cracks is the "cratering test", a destructive test that may be done periodically as a process monitor on a few product die samples, where the pad Al (and wirebond) is removed to inspect for damage to the pad structure. This test is not good at detecting cracks initiated at the bottom of the top SiO_2 film unless they become large enough to break the top surface. Inspecting for cracks by cratering test after wirebond can help to identify probe cracks as well as bond cracks. Probe cracks initiate at the location of the probe mark and tend to be shorter in length and tighter radius than bonding cracks. A probe crack that has gone through harsh bonding may have grown significantly, now a long crack across the pad center, perpendicular to the ultrasonic motion. Some probe cracks may also become like a starburst with propagation in many directions, recognizable as having initiated in probe because of the location in the pad. Ball bonding cracks from the ultrasonic energy have a characteristic arc shape of similar radius and location to the bond contact edge, roughly perpendicular to the ultrasonic motion. Bond cracks are often in pairs on opposite sides of the pad. Bond pad "ripple" is easy to spot at low magnification in the cratering test. High ripple is expected to have cracks associated with it [6].

CUP Pad Requirements: This work focuses on finding the best methods for design of CUP pads in existing manufacturing processes, having Al-based metallization in SiO_2 in the technologies of interest. Summarizing the situation and various requirements and engineering tradeoffs, we have:

1.) Traditional *pads crack easily* in standard wafer probe
2.) Traditional *pads crack easily* in Au wirebond
3.) *Pads cracks are NOT acceptable* in CUP / BOAC
4.) Circuits may have *two to 7 layers of metal*
5.) *All metal sub-layers* below the pad Al must be available for CUP interconnects through the pad window
6.) At least *some top vias* must be allowed in the pad window
7.) *Pad Al thickness may range from 0.55µm to 3µm*
8.) Some products allow up to *6 touchdowns at wafer probe*, increasing stress to pad
9.) Must be able to bond with *Au, Au alloy or Cu wire*, (Cu wirebond increases stress to pad)
10.) Product *reliability must increase*, not decrease
11.) *Deformation or bending in CUP metallization* layers is not acceptable in high reliability designs
12.) Product *cost must decrease* (smaller die size, no additional process steps, no wafer fab process changes, no additional materials costs, Cu wirebond option, …)

Available Pad Improvement Methods: We refer to George Harmon's reference book "Wirebonding in Microelectronics" as the general reference for understanding and optimizing wirebonding, and as a guide to some pertinent literature [7]. We categorize the available methods in the literature into 3 rough groups, based on well known industry practices, published literature and patents: 1.) Reduce the mechanical stress to the bond pad Al, 2.) Modify the top of the bond pad to reduce the stress reaching the pad sub-layers, 3.) Modify pad structure features for a specific purpose. We elaborate on each of these below.

1.) Reduce the mechanical stress to the bond pad Al

It is already industry practice to reduce stress to the bond pad in every way possible. This includes minimizing wafer probe force and touchdowns, and minimizing stress at wirebond. There is a growing list of options available at wafer probe to reduce stress to the bond pads, though increased expense will be required to accomplish increasingly gentler probing. On the other hand, Cu wirebond always imparts more stress to the bond pad than Au wirebond because more energy is required for creating the Cu – Al bond. Regardless of improvements to reduce pad stress at wafer probe, the pad structure must still be made more robust against cracks for Cu wirebond.

2.) Modify the top of the bond pad to reduce the stress reaching the pad sub-layers

Among the available methods to modify the bond pad upper layers, pad Al may be thickened or the barrier layer beneath pad Al may be improved and thickened, to reduce the stress reaching the top SiO_2 layer. Films may be added to the top of the existing pad metal as well. Thickening the pad Al or adding Al on the top are the simplest and lowest cost methods, however these don't meet our requirements of "no additional cost". For the pad metal thickness increase or other modification must be significant enough to prevent the additional stress of Cu wirebond from reaching the top SiO_2, the thickness increase may need to be large as compared with current pad Al. Doubling or tripling the pad Al thickness may be sufficient to prevent top SiO_2 cracking, but it still may not eliminate the undesirable sub-layer Al deformation. Thickening top metal generally requires further design tradeoffs as well, because the metal width and spacing rules must expand, counteracting the benefits of CUP pads for die size reduction.

Thicker barrier films below pad Al are an option to reduce stress from reaching the top SiO_2. Increasing barrier film thicknesses or substituting or adding new materials can be engineered to reduce pad cracking, but the change adds costs in re-engineering and qualification, with potential engineering tradeoffs such as wider line and space rules. Additional films after the current pad processing such as redistribution layers (RDL) can protect the pad CUP circuitry well, but all require extra process steps and cost. In our case, we will not consider these options. Examples of added layers are in references [8-10].

3.) Modify pad structure features for a specific purpose

There are numerous reported methods for modification of pad structure, each having a specific purpose, and many do not require process changes or additions. Essentially all recent bond pad literature deals with Cu – lowK bond pads, having an Al sheet on the top, where Cu provides the structural strength, unlike our case where the SiO_2 is stiffer than the Al metal. Most methods reported for Cu – lowK are instructive but cannot be directly applied to our Al – SiO_2 structures of interest, so we will generally not refer to them. Examples of pad structure design methods that could potentially be applied to the Al – SiO_2 pad structures of interest are:

- Eliminate top vias from the pad window to reduce cracking
- Change the pad metal topology to improve wirebond adhesion [11-14]
- Employ the two or more topmost metal layers as "the pad", which may include special metal patterning, then allow circuitry or devices beneath [15-18]
- Modify the top via pattern or use "via trenches" or "giant vias" in or around the pad window to prevent cracks or to contain cracks from propagating laterally outside the pad [19,20]
- Use top vias and lower vias in combination with specific sub-layer metal patterns to "strengthen" the structure [21]
- Remove sub-layer metal features to reduce stress to devices beneath, but place sub-layer dummy metal or specific metal features for damping of bonding stress to protect underlying devices [22,23]
- Place certain metal sub-layer patterns to achieve specific capacitance performance [24,25]
- Place specifically designed connected metal bus structures suitable for CUP in the pad window sub-layers [26]

Most of these methods don't make our short list because they don't permit free-form CUP design in the MT(-1) layer. Removal of top vias helps significantly to prevent top SiO_2 cracking, however, at least some top vias must be permitted in the CUP designs we require. The available methods don't help in this case. Methods that might still appear to be potentially usable are too

restrictive in what can be done below the pad window, or they add cost and still fall short of achieving all the requirements. Some of the claimed methods simply won't work in preventing metal deformation and cracks when applied to the technologies of interest, including 2-level metal.

We conclude that none of the surveyed methods or a combination of them will adequately improve an Al – SiO_2 pad structure's robustness to deformation and cracking in Cu wirebond for high reliability CUP designs at no additional cost. We must develop our own method.

Basic Pad Mechanical Issues – Al deformation, SiO_2 Cracking: Our previous experimental work highlights the key mechanisms of Al deformation and SiO_2 cracking in bond pads. We begin by discussing traditional pad structures, as shown in figure 1, above. Figure 2 shows another illustration of the traditional pad stack, this time illustrating a tiny section, zoomed in to see the approximate films thicknesses in relation to each other. The silicon (Si) layer at the bottom represents the wafer surface.

Figure 2. Thin films stack illustration of a traditional Al – SiO_2 bond pad within the pad window. Barrier and other layers are omitted for simplicity.

Pad Al on the top is the film that receives the stress from probing and bonding. Pad Al deforms easily into a probe mark, or compresses under the bond and splashes out, absorbing and dissipating much of the stress locally. An advantage with thicker pad Al is that it is able to absorb and dissipate more stress, reducing the stress reaching the brittle top SiO_2 film. Pad stress that couples into the top SiO_2 can result in cracking.

Wirebond Scenario: Figure 3 is an illustration of these concepts, showing deformation and bending that may occur under the edge of the bond contact area in harsh bonding such as Cu ball bond.

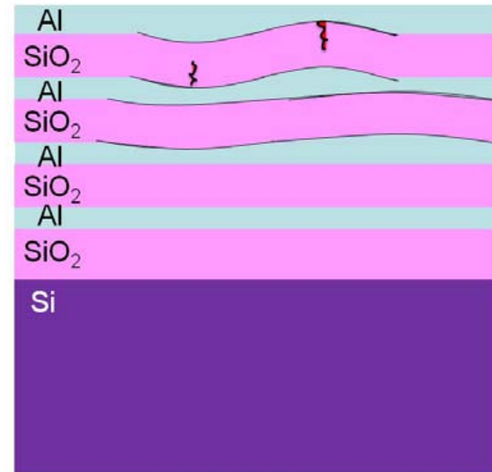

Figure 3. Thin films stack illustration of a traditional Al – SiO_2 bond pad, within the pad window, after ball bonding stress. Barrier and other layers are omitted for simplicity, and deformations are exaggerated for clarity. Cracks are shown at points of highest tensile stress in the top SiO_2.

Figure 3 is intended to show how the Al in pad sub-layers deforms plastically, while the SiO_2 films only bend. This makes it conceptually clear how the cracks initiate in the brittle SiO_2 film. Such films deformation and bending can be observed in focused ion beam (FIB) cross sections after crater test from harsh bonding on traditional pads with thin pad Al.

The harsh bonding stress scenario of figure 3 has the down force stress, generally applied more towards the outside of the ball contact area by the bonding capillary, with much additional stress from the lateral ultrasonic movement of the capillary. On the order of one thousand ultrasonic "shakes" are expected in a typical ball bonding process. At first the ultrasonic energy will shake the ball back and forth across the pad Al surface, but as the weld begins the ball becomes physically connected to the pad, so ultrasonic energy from the capillary eventually connects directly into the pad Al. The pad Al deforms greatly in the process, absorbing and dissipating stress, so that the stress that reaches

into the top SiO_2 has hopefully been dampened sufficiently to prevent deformation and cracking. This is often the case for thick pad Al, but if the pad Al is thin, high stress couples into the top SiO_2 and damage may be caused.

The lateral shaking of the top two or more SiO_2 layers in addition to the downforce will cause hill and valley deformation in the highest stress points in both MT(-1) and MT(-2). In a traditional pad, the MT(-1) is a full sheet across the pad window, and it is relatively easy for some Al material to migrate laterally away from the highest stress region, leaving a local valley and building up into a hill nearby. Figure 3 also illustrates the concept of the more subtle Al deformation in MT(-2), with the SiO_2 above it bending in conformance. The top SiO_2 bends in conformance to the total MT(-1) deformation, including any bending caused from the SiO_2 below. Tensile stress in the top SiO_2 due to the bending may be substantial, potentially causing crack initiation at the bottom of the valley and at the top of the hill. Pad ripple as seen in the cratering test will highlight the locations of greatest stress, being the most visible hills and valleys. Cracks visible in the cratering test are generally those at the "hill" locations.

Wafer Probe Scenario: The pad Al film deforms plastically in wafer probe due to a substantially downward force, forming the familiar probe mark. The downward stress that is not dissipated elsewhere into the pad Al can reach the top SiO_2 layer, which compresses, causing stress in the MT(-1) Al, which compresses against the stiffer SiO_2 below it. If there is sufficient stress in the MT(-1) it will plastically deform creating a local "valley" in the upper surface. The top SiO_2 bends into this MT(-1), causing tensile stress which may initiate a crack. Similar deformation and bending can occur in the layers below if there is sufficient stress, and the bending in lower layers will cause extra bending in the upper layers, being physically attached, compounding the tensile stress in the top SiO_2 and making the formation of cracks more likely. This mechanism for cracking at wafer probe is verified by the visible ripple seen in cratering tests, though ripple from probe is typically much smaller in area and more subtle than ripple from bonding.

Cracking occurs more easily when top vias are present in the top SiO_2. The W vias are much stiffer and won't compress or bend like the surrounding SiO_2 during local stress such as the force from a probe tip. If a probe tip exerts stress directly to the top SiO_2 and W vias together, as in our harsh probing experiments, the SiO_2 will compress while the W will not, relatively speaking. This mismatch will produce high stress in the SiO_2 and liner films surrounding the vias, enhancing the likelihood of crack initiation or propagation in that locality. Similarly, in bonding, the ultrasonic stress can more easily initiate cracks at via locations due to the stress mismatch through the alternating compression – tension cycles of the ultrasonic force.

Experimental pad designs: Harsh probing and harsh bonding experiments include experimental pads with various widths of slots or arrays of holes of various sizes in the pad window, in MT(-1), MT(-2) and MT(-3) layers. Also, full sheets of metal, absence of metal in certain layers, and dummy metal fill. Fifty-eight pad variations were actually tested, but we report here only on the few significant findings.

Traditional pad designs with full sheets of metal in MT(-1), MT(-2), and MT(-3) were consistently the weakest in regards to deformation of Al in sub-layers, with the most cracking in top SiO_2. Top vias enhance the top SiO_2 cracking, with cracks tending to propagate from via to via. Thickening pad Al reduces the tendency for sub-layer Al deformation, reducing cracking of the top SiO_2. All experimental pad structures were found to be more robust to cracking as compared with traditional pads.

Findings from harsh probing: Cracks initiate in top SiO_2 above metal features, especially MT(-1) which is nearest the pad Al. A dramatic decrease in cracking is seen as the pattern density in MT(-1) decreases in the pad window. Once the pattern density is lowered to about 50%, in a roughly uniform pattern, there is little cracking in the top SiO_2 for pad Al of 0.55μm to 0.8μm thickness. MT(-2) pattern density must also be lowered to further prevent cracking, but not as much as MT(-1). Vias between MT(-2) and MT(-1) tend to improve crack prevention slightly. Even MT(-3) can deform and cause top SiO_2 cracking and should not be a full sheet across the pad window.

Further analysis of the interaction of cracks from harsh probing with the sub-layer metal patterns

reveals that top SiO_2 cracks initiate in two basic situations. Most common is for a crack to form over a wide metal feature, similar to when the sub-layer is a full sheet. If the probe scrubs directly over a metal feature, that's where the crack will form. Cracks tend not to form when the probe scrubs over a "space", in other words a region of thicker SiO_2 which cannot bend easily. The other mechanism for cracks to form over patterned metal sub-layers is when the probe scrubs across a transition from space to metal, going from thick SiO_2 to a region of thin SiO_2 over metal or visa versa. The SiO_2 over metal bends downward while the thick SiO_2 in the space holds more constant. This creates high tensile stress at the transition, potentially initiating a crack in the top surface of the top SiO_2, easily visible in a cratering test.

Best crack prevention in the top SiO_2 from harsh probing is for the MT(-1) to be missing completely from the pad window, with lowered metal pattern densities in MT(-2) and MT(-3). When circuitry is required in MT(-1), then the metal feature width between holes or slots must be kept small in the direction perpendicular to the probe scrub, in addition to the low overall pattern density. This width restriction reduces the chance of cracking at the space to metal transitions by preventing deformation of the Al and subsequent bending of the top SiO_2. The presence of vias below sub-layer metal features is beneficial in preventing probe cracks.

Cracking results are most easily seen when pad Al is thinner and probing conditions are harsher. In summary, successful crack prevention in harsh probing is accomplished by preventing the probe downforce from being able to deform sub-layer Al and bend the top SiO_2.

Findings from harsh bonding: Compared to the harsh probing results, a similar trend of reduced cracking for reduced MT(-1) pattern density is seen. Also the reduction of metal width in the MT(-1) pattern is beneficial. Bonding cracks don't appear to interact with the MT(-1) pattern directly as they do in harsh probing. The absence of MT(-1) beneath highest stress regions of bonding prevents cracking similarly to the case for harsh probing.

Unlike the harsh probing case, prevention of cracks in the top SiO_2 improves slightly with the presence of some MT(-1) features, and vias below connecting to MT(-2) features, as long as the MT(-1) has sufficiently low pattern density and relatively small metal width. Harsh bonding, with the ultrasonic energy being an additional harsh stress component, benefits from both metal and via features in the sub-layers. If the pad sub-layer metal widths are small enough to prevent Al hill and valley formation, bonding cracks are prevented.

Combined summary, probing and bonding: Prevention of cracking can be acomplished, even for thin pad Al, by keeping the sub-layer Al from being able to deform. SiO_2 is the stronger material in compression, so use it to advantage in the pad structure, but never provide a situation where the thin top SiO_2 is able to bend significantly. High tensile stress during bending can cause initiation of a crack in the SiO_2. Knowing these principles and making use of specific data from experimentation in each technology and pad Al thickness of interest, one can design metal interconnect circuitry through the pad window while preventing cracking. CUP circuitry can thus be used to improve the robustness of the pad without any process changes, facilitating much harsher probing and bonding than is possible on traditional bond pads, reducing the need for thicker pad Al.

CUP Pad Design Guidelines: taking note of the differences between the harsh probing and harsh bonding results, we favor the creation of design guidelines catering to harsh bonding because we have more methods available to reduce cracking at wafer probe, if this were to become necessary. We have confidence that by robust CUP layouts for harsh bonding, pad cracking likelihood will already be reduced by at least 2 orders of magnitude from the cracking of traditional pads without top vias, and the chance of encountering a probing situation in production as harsh as the probing experiments is nil.

Table 1 shows general CUP pad metallization layout guidelines based on the extensive experimentation. Once a pad Al thickness is chosen, we refer to specific ranges for MT(-1) and MT(-2) pattern density in the pad window, and qualitative recommendations for limits on the maximum metal width in each sub-layer.

MT	Very thin	nominal	THICK
VT	Very sparse	Sparse	Sparse
MT(-1) density *MT(-1) width*	0 to half density, *very narrow*	0 to 3/4 density, *narrow*	0 to "not full density" *not as narrow*
VT(-1)	Dense vias encouraged		
MT(-2) density *MT(-2) width*	¼ to 3/4 density, *wide*	¼ to "not full density" *wider*	¼ to "not full density" *widest*
VT(-2)	Dense vias encouraged		
MT(-3)	¼ to "not full density"		

Table 1. Recommended Al – SiO_2 bond pad design guidelines based on the combined outcomes of previous harsh probing and harsh bonding experiments.

Actual numbers for pad Al thickness and maximum metal width will be more dependent upon film details in an individual technology (actual cladding or barrier layer thicknesses and materials, Al alloy and thickness and SiO_2 layer thicknesses). MT(-1) is allowed to be zero density, meaning that there is no MT(-1) at all within the pad window. As we saw, this may be best in case of harsh probing. But for harsh bonding, some density of MT(-1), with vias below are encouraged.

Sparse top vias may be allowed to connect the pad metal to circuitry in MT(-1) within the pad window, but are discouraged in the probing region as well as the bonding high stress region because of their tendency to enhance cracking. For ball bond pads, it may be preferable to chamfer the inside corners of the pad window to include dense vias as desired just outside the pad window where high stress will be avoided.

MT(-2) and MT(-3) should definitely have some pattern density within the pad window, and are allowed to be much more dense, with larger metal widths between spaces, but they may not be full sheets. Larger metal width in lower metal levels is allowed because the thick SiO_2 above does not bend so easily. Vias between MT(-3) and MT(-2) in the pad window are encouraged. Lower vias significantly help to reduce pad cracking.

CUP Pad Design Solution Examples

Robust Pad Design Example 1: 3LM CUP Pad. A design was needed for a CUP pad in an older 3-level metal CMOS technology having very thin MT. Only about 5% circuit density is required in MT(-1), with top vias to the MT(-1). MT(-2) and below is designed for ESD protection under the pad. CUP pads in this technology have been troublesome in the past due to cracking.

MT(-2) (which is the metal 1 layer in this case) ended up being over 90% dense in the pad window after routine layout procedures for the ESD protection structures. It was left as is, though the density was higher than desired according to the table. Top vias and the required MT(-1) features were moved near the pad window edge as much as possible, to avoid interaction with probing and ball bonding stresses.

The product was fabricated and qualified for production in standard probing and Au wire bonding. Then much extra testing was done to look at potential effects of harsh probing and harsh bonding on the new pad structures. No cracking was found after harsh probing. A small percent of pads were found with craters after harsh bonding, thought to be due to the harsh recipe being too extreme for such thin pad metal. (The same harsh bonding recipe cracked nearly 100% of traditional pads in this technology). This performance was acceptable for the product, which has been successful in production with Au wirebond.

Robust Design Example 2 3LM Power Device. A power device having 3-level metal designed with a "pad anywhere" layout concept, failed its reliability qualification due to cracks shorting the pad metal to the circuitry beneath. The particular pads with cracking were the ones where MT(-1) had very large busses within the pad window.

Based on the concepts learned from experiments with various pad structures, it was clear that the MT(-1) density must be lowered within the pad window. Various designs for this product were tried out designed experiment, including placement of holes or slots in MT(-1) and MT(-2) within the

pad window, and alternate placement or density of vias. The simplest solution worked best: place an array of holes in only the wide MT(-1) features within each pad window, lowering that feature's pattern density to about 80%. No modifications were required to other MT(-1) circuitry within the pad window or to any MT(-2) circuitry. Via position or density alterations made no difference in this case. The bus resistance increase due to the added holes was still well within the required tolerance, so this was an acceptable solution.

The revised product was then qualified and also passed harsher reliability stressing without issues. It has been successful in production without issues. Numerous other products have been designed (or redesigned) and introduced into production following the same guidelines, all successful with no cracking issues.

Robust Design Example 3 Robust Pad for Design Library. A robust pad design was needed for a design library. It needed to accommodate 4 or more levels of metal, with ESD protection circuitry beneath the pad, and CUP circuitry capability through the pad window. Designers need the options to decide whether or not to use the provided metal 1 design including the ESD protection under pad. Also, bus circuitry is provided, crossing the pad window in MT(-2). But similar bus circuitry in MT(-1) is to be optional, the default design being MT(-1) absent from the pad window to be best for harsh probing in case circuitry is not actually required in MT(-1) in a particular pad. This technology has nominal MT thickness.

A standardized CUP pad for 4 or more metal layers was designed having 3 versions: 1.) without MT(-1) in the pad window, busses through the pad window in MT(-2), and metal 1 design for the ESD protection circuitry to go under the pad; 2.) & 3.) same MT(-2) and ESD options, but two different bussing arrangements through the pad window in MT(-1), with arrays of holes in the MT(-1) busses, and some vias to MT(-2). All 3 designs were fabricated, assembled by ball bond and plastic package, some standard and some harsh wirebond (1mil Au, Au-Pd, and Cu wires were all used in the experiment). Three lots of assembled parts were reliability stressed for double the normal times and cycles. All parts passed the tests, and many were then subjected to wire pull testing followed by cratering test to look for cracks. Wire pull data was still fine. No cracks or other issues relating to the bond pad structure were found, either prior to or after the reliability stressing. No performance differences were found between the 3 designs in terms of sub-layer deformation.

The pad without MT(-1) in the pad window was chosen as the library standard, being the simplest robust pad whether CUP is employed or not. It is in use in the pad library and has the optional ESD structures under pad available. Appropriate design rule checks (DRC) are implemented to ensure that only robust pads are used. The other 2 pad versions are qualified as well, so when a design requires, either of them can be used without risk.

Further recommendations concerning the use of the pad design guidelines and more reliability considerations are given in another paper [27].

Conclusions

A number of pad design challenges must be overcome in producing lower cost higher reliability ICs having Al – SiO_2 pad structures. Available methods fall short of accomplishing the required objectives simultaneously. Extensive experimental results of our own work have been analyzed for both harsh probing and harsh wirebonding on test pads. There is sufficient information to show that robust pads may be designed using the CUP circuitry itself to prevent cracking and facilitate harsher bonding.

General pad design guidelines are presented based on the overall analyses. The guidelines are mainly qualitative, but can be refined based on the thin films details of a particular technology. Three examples of successful new pad introduction have been discussed.

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