ON Semiconductor®

Power Electronics System Thermal Design

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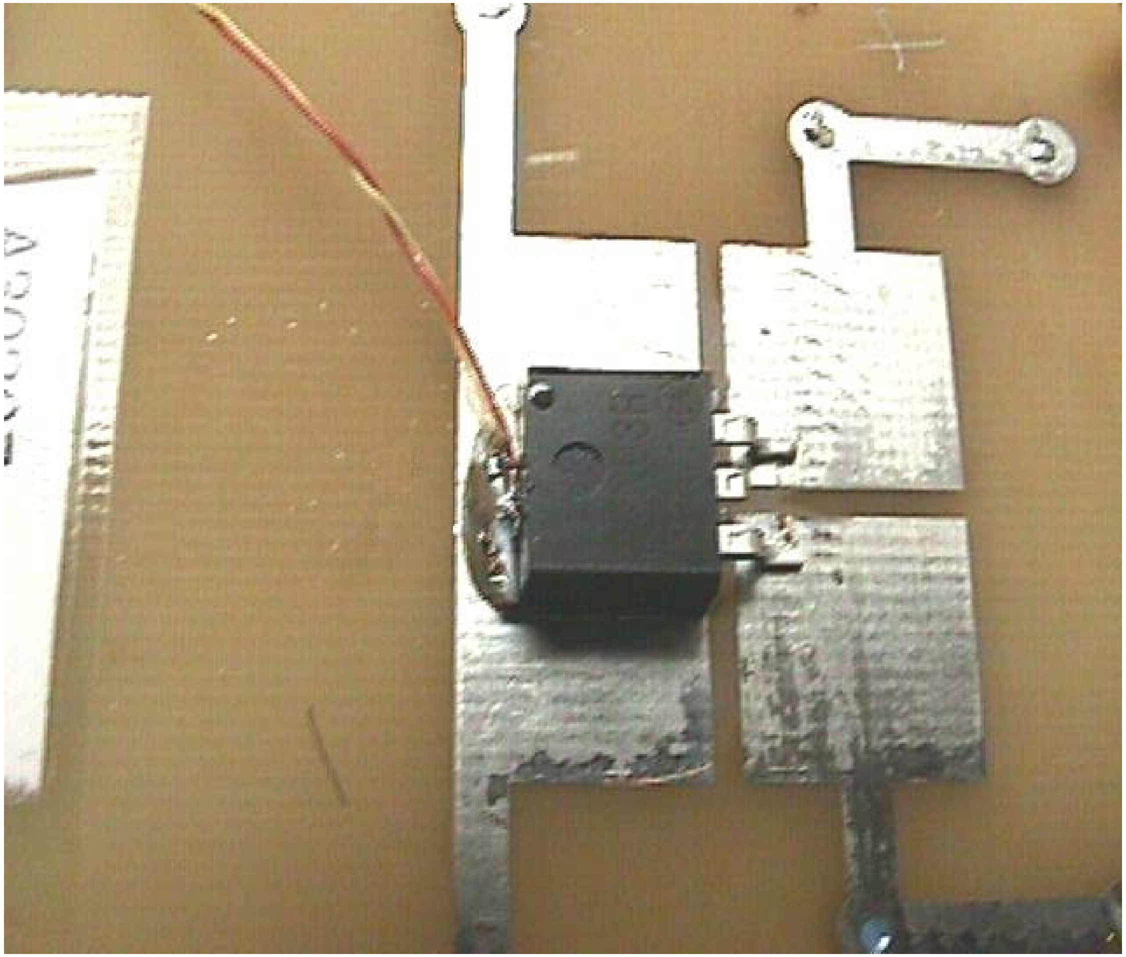
Course outline

- ***Part I: (90 minutes)***
  - Introduction (30 minutes)
  - Characterization Techniques (60 minutes)

>> 30 minute BREAK <<

- ***Part II: (45 minutes)***
  - Linear Superposition – Theory (7 minutes)
  - The Reciprocity Theorem (6 minutes)
  - A Detailed Example and its Implications (6 minutes)
  - Controlling the Matrix (6 minutes)
  - Building a System Model (20 minutes)
- ***Part III: (35 minutes)***
  - Thermal Runaway – Theory (15 minutes)
  - Thermal Runaway – Practice #1 (7 minutes)
  - Thermal Runaway – Practice #2 (13 minutes)
- ***Quick demos (10 minutes, time permitting)***

Can this device handle 2 W?



“Junction” temperature?

Historically, for discrete devices, the *junction* was literally the essential “pn” junction of the device. This is still true for basic rectifiers, bipolar transistors, and many other devices.

More generally, however, by “junction” these days we mean simply the hottest place in the device (which *will* be somewhere on the silicon).

As we move to complex devices where different parts of the silicon do different jobs at different times, the *exact* location gets to be somewhat tricky to identify. But we’re still interested in the hottest spot.

Thermal-electrical analogy

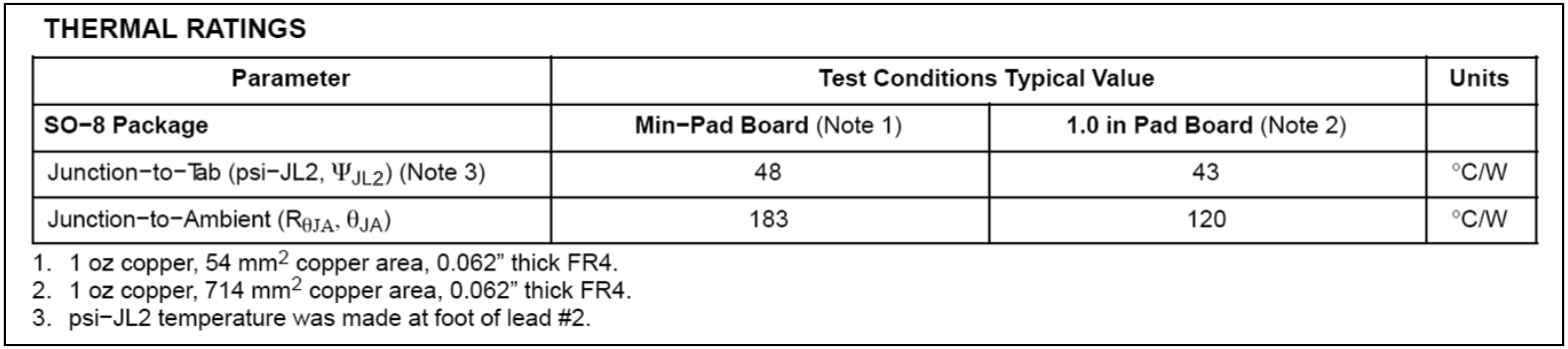
temperature <=> voltage

power <=> current

Δtemp/power <=> resistance

energy/degree <=> capacitance

What’s wrong with theta-JA?



THERMAL RATINGS

Parameter	**Test Conditions Typical Value**		**Units**
SO−8 Package	**Min−Pad Board** (Note 1)	**1.0 in Pad Board** (Note 2)	
Junction−to−Tab (psi−JL2, Ψ_{JL2}) (Note 3)	48	43	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	183	120	°C/W

1. 1 oz copper, 54 mm^2 copper area, 0.062” thick FR4.
2. 1 oz copper, 714 mm^2 copper area, 0.062” thick FR4.
3. psi−JL2 temperature was made at foot of lead #2.

$$\theta_{JA} = \frac{T_J - T_a}{P_d}$$

$$\Psi_{Jtab} = \frac{T_J - T_{tab}}{P_d}$$

$$T_J = \theta_{JA} \cdot P_d + T_a$$

$$T_J = \Psi_{Jtab} \cdot P_d + T_{tab}$$

Theta-JA vs. copper area

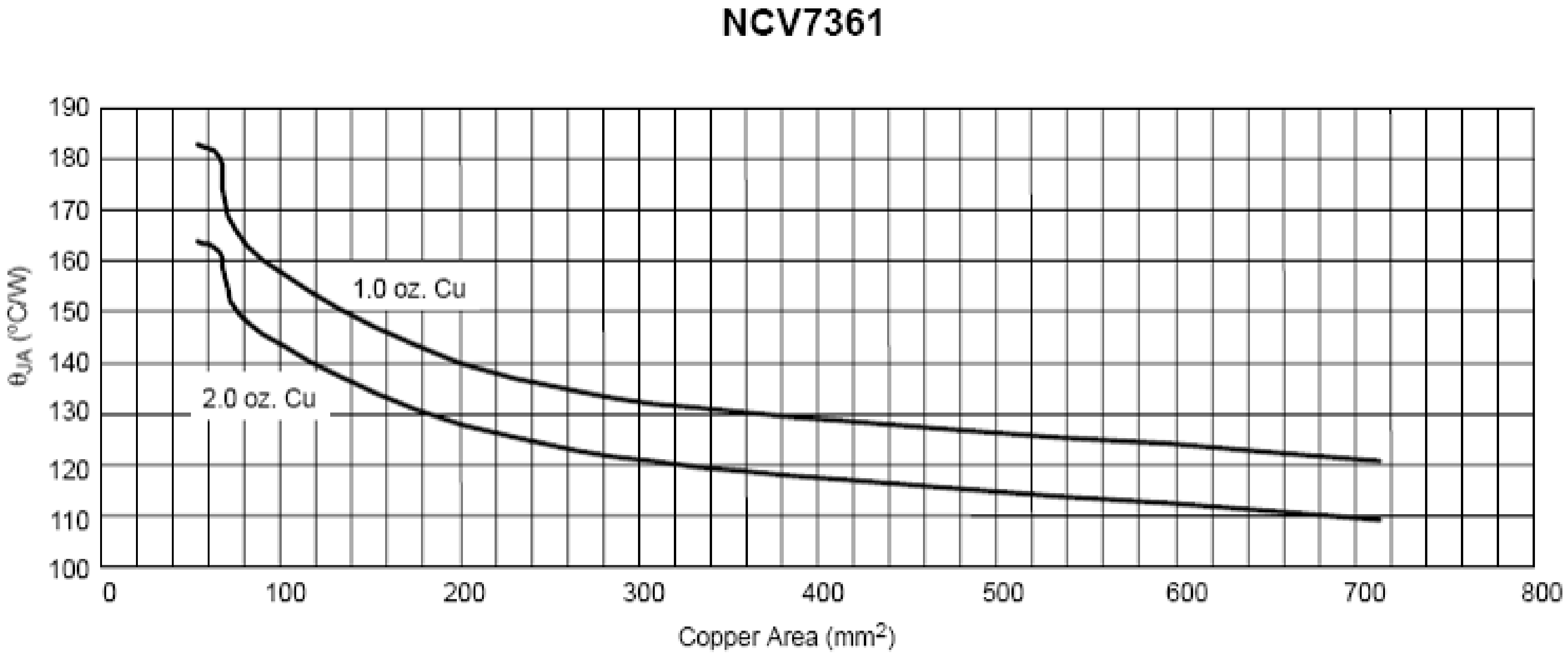


Figure 21. SO−8, θ_{JA} as a Function of the Pad Copper Area Including Traces, Board Material

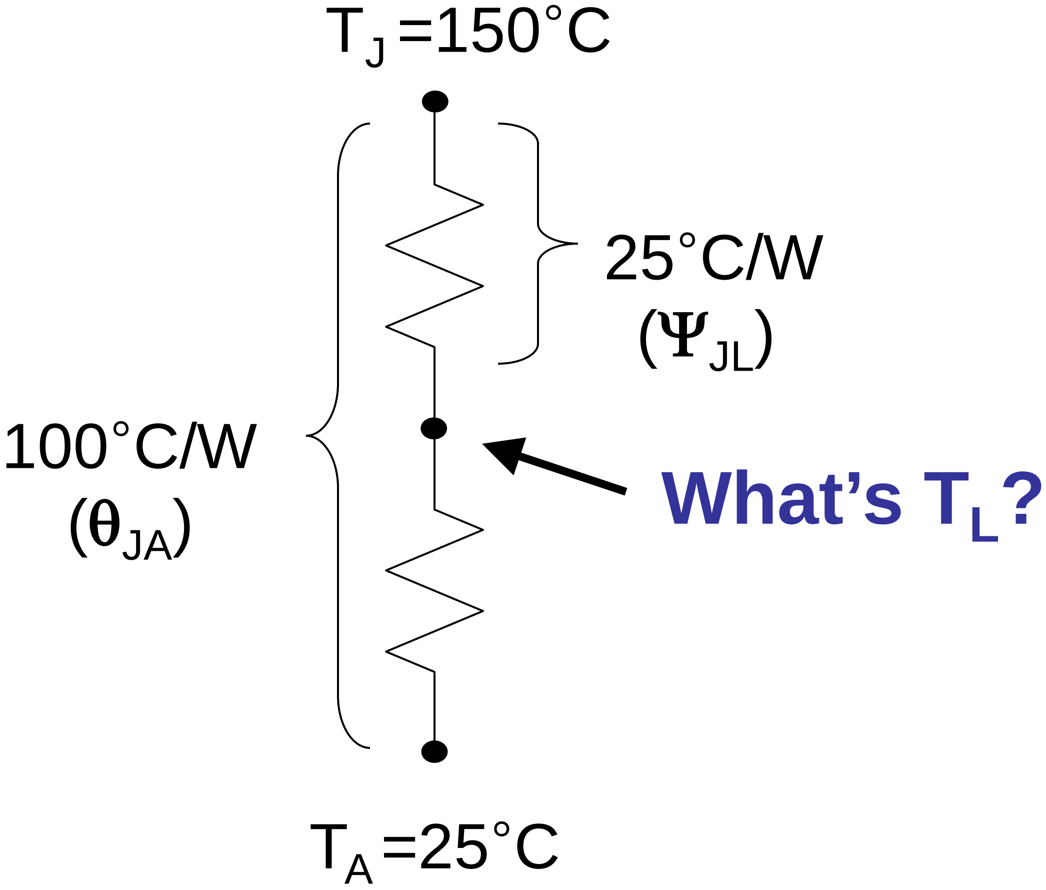
An example of a device with two *different* “Max Power” ratings

- **Suppose a datasheet says:**
  - $T_{jmax} = 150^\circ C$
  - $\theta_{JA} = 100^\circ C/W$
  - $P_d = 1.25W\ (T_{amb}=25^\circ C)$

- **But it also says:**
  - $\Psi_{JL} = 25^\circ C/W$
  - $P_d = 3.0W\ (T_L=75^\circ C)$

Where’s the “inconsistency”?

Where's the inconsistency?



T_J=150°C

25°C/W
(Ψ_{JL})

100°C/W
(θ_{JA})

What's T_L?

T_A=25°C

Why is ON’s SOT-23 thermal number so much worse than the other guy’s?

- ON
  - SOT-23 package
  - 60x60 die
  - Solder D/A
  - Copper leadframe
  - Min-pad board
  - Still air

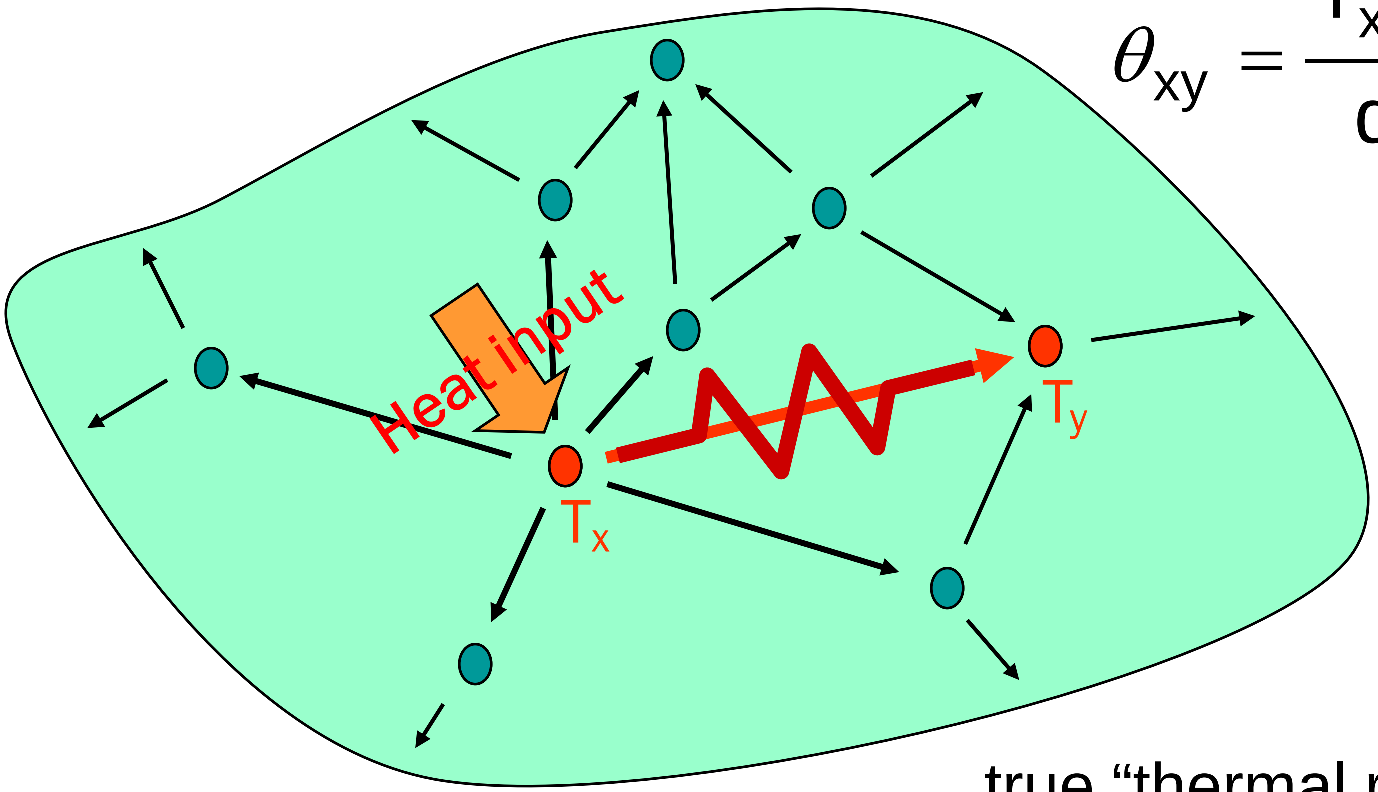
- some other guy
  - SOT-23 package
  - 20x20 die
  - Epoxy D/A
  - Alloy 42 leadframe
  - 1” x 2oz spreader
  - Big fan

Theta (θ) vs. Psi (Ψ)

- JEDEC <http://www.jedec.org/> terminology
  - $Z_{\theta JX}$, $R_{\theta JA}$ older terms ref JESD23-3, 23-4
  - θ_{JA} ref JESD 51, 51-1
  - θ_{JMA} ref JESD 51-6
  - Ψ_{JT}, Ψ_{TA} ref JESD 51-2
  - Ψ_{JB}, Ψ_{BA} ref JESD 51-6, 51-8
  - $R_{\theta JB}$ ref JESD 51-8
  - **Great overview, all terms: JESD 51-12**

“Theta” (Greek letter θ)

We know actual heat flowing along path of interest

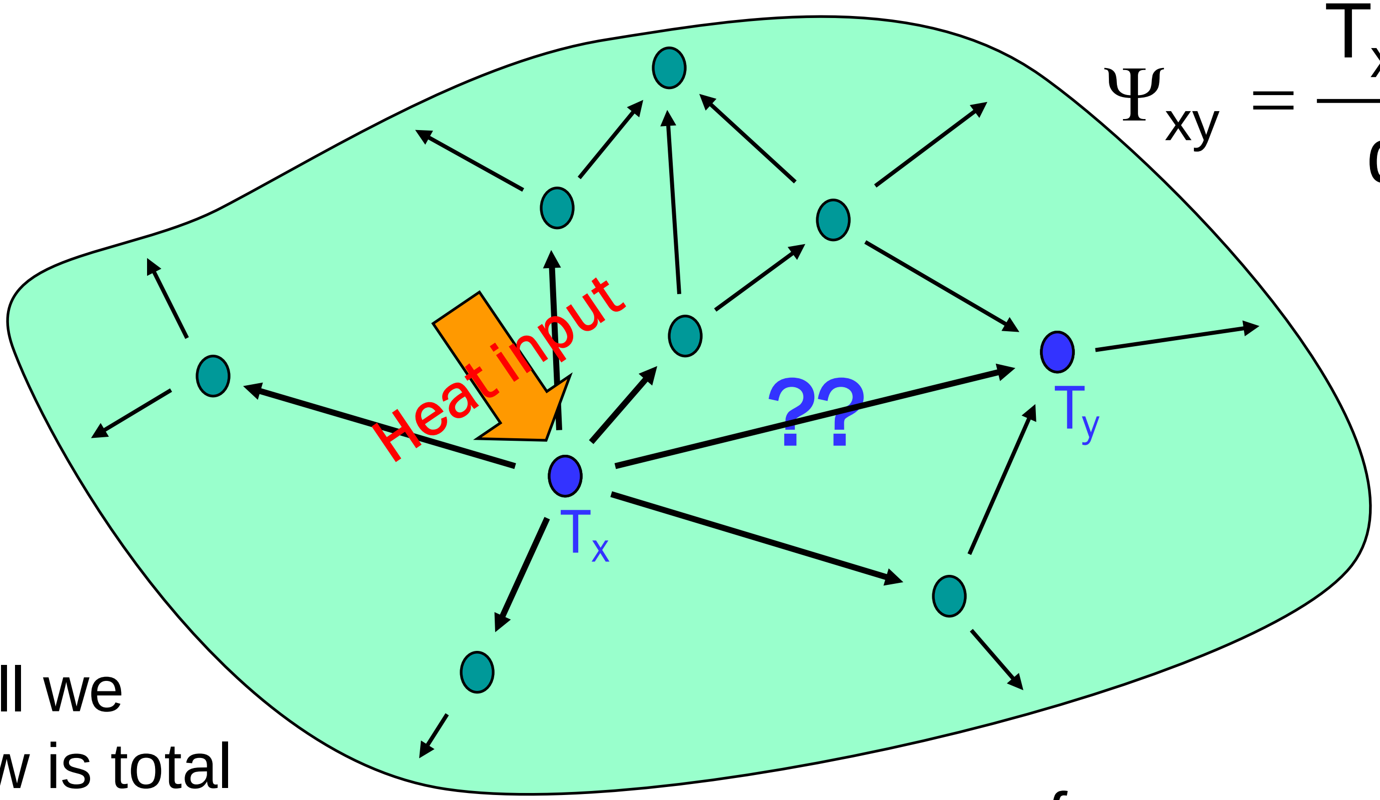


$$\theta_{xy} = \frac{T_x - T_y}{q_{path}}$$

true “thermal resistance”

“Psi” (Greek letter Ψ)

We *don’t know* actual heat flowing along path of interest



$$\Psi_{xy} = \frac{T_x - T_y}{q_{total}}$$

… all we know is total heat input

a reference number only

Fundamental ideas

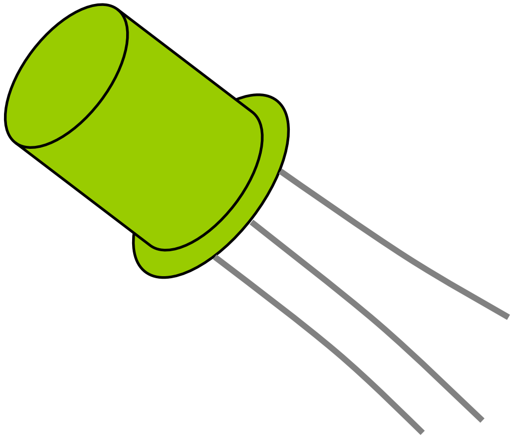
- Heat flows from higher temperature to lower temperature
- The bigger the temperature difference, the more heat that flows
- Three modes of heat transfer
  - Conduction (solids, fluids with no motion)
  - Convection (fluids in motion)
  - Radiation (it just happens)

Common fallacy

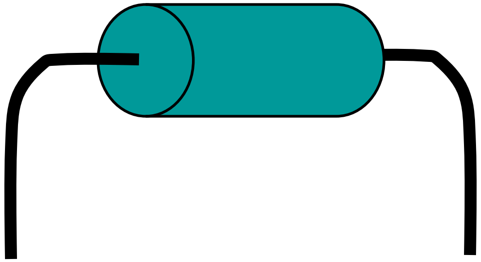
- Basic idea:
  - “thermal resistance” is an intrinsic property of a package
- Flaws in idea:
  - there is no isothermal “surface”, so you can’t define a “case” temperature
    - Plastic body (especially) has big gradients
  - different leads are at different temperatures
  - multiple, parallel thermal paths out of package

Back in the good old days ...

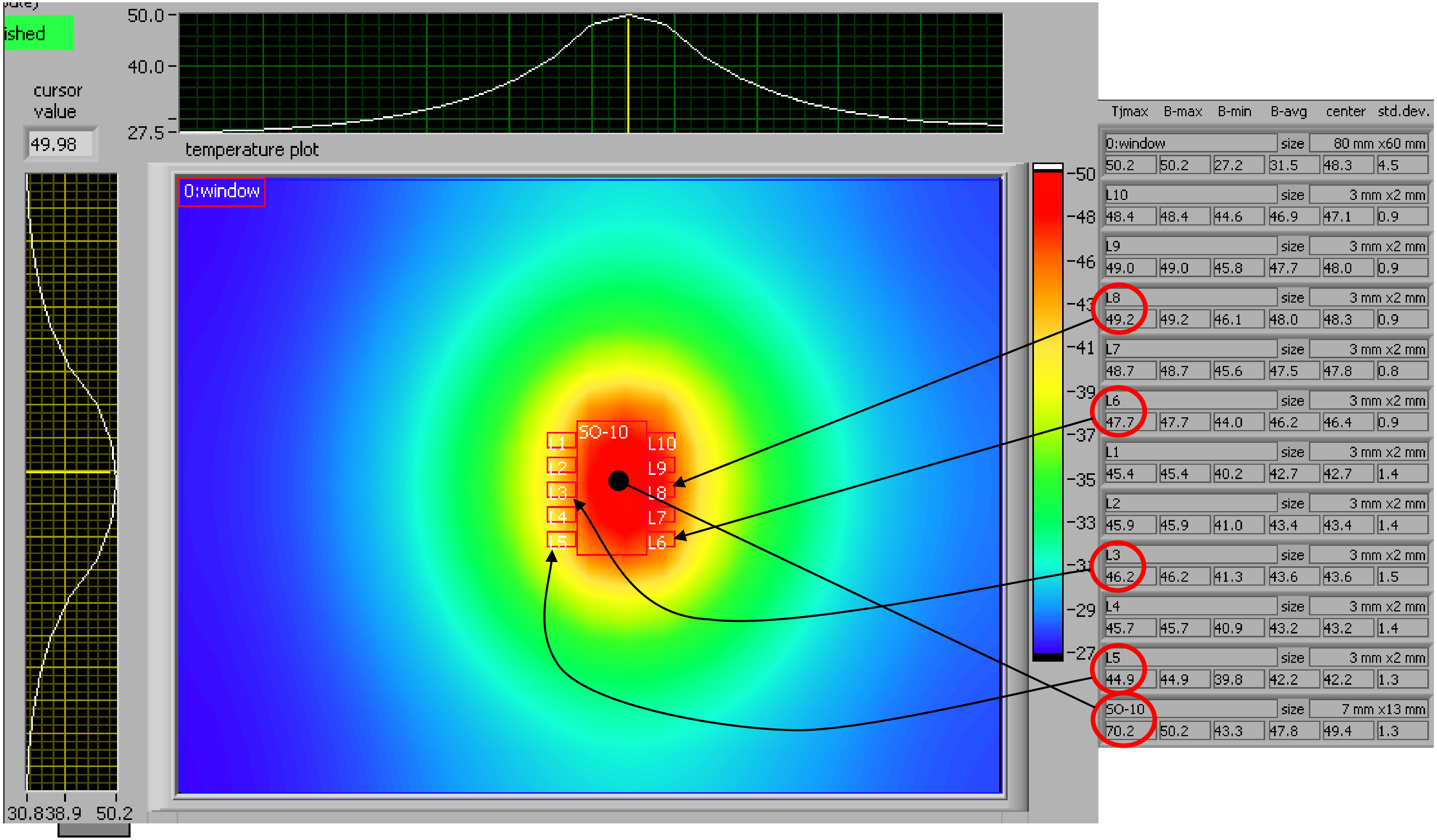
metal can – *might be* a fair approximation of an "isothermal" surface



axial leaded device - only two leads, at least the heat path is fairly well defined



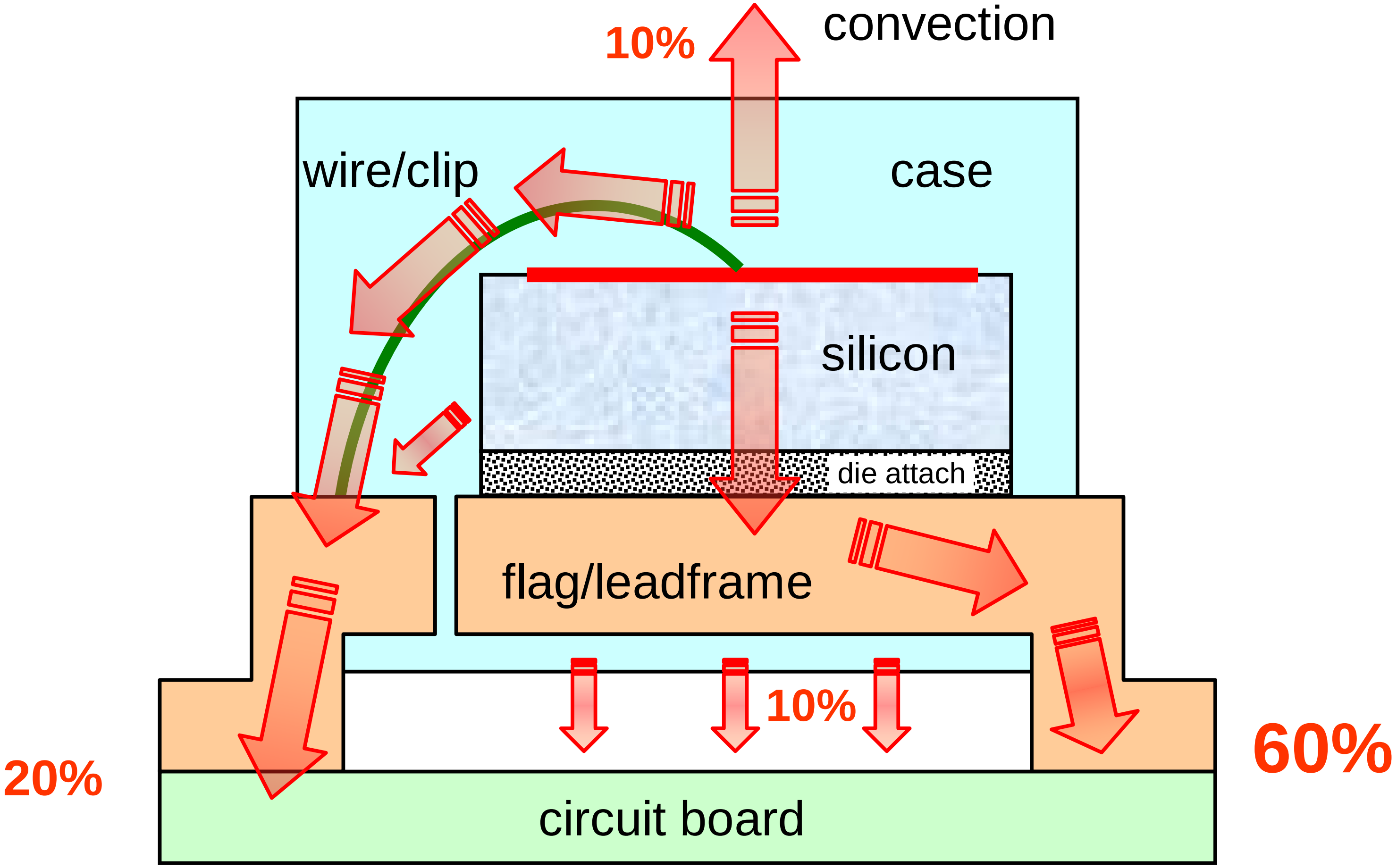
Which lead? Where on case?



cursor value 49.98

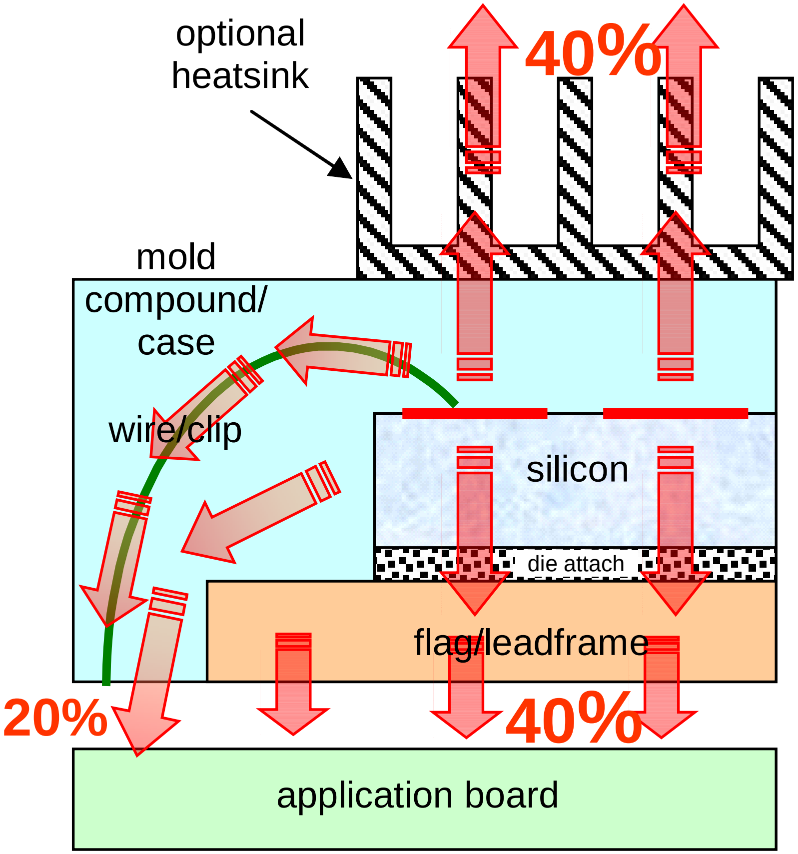
	size	Tjmax	B-max	B-min	B-avg	center	std.dev.
0:window	80 mm x60 mm	50.2	50.2	27.2	31.5	48.3	4.5
L10	3 mm x2 mm	48.4	48.4	44.6	46.9	47.1	0.9
L9	3 mm x2 mm	49.0	49.0	45.8	47.7	48.0	0.9
L8	3 mm x2 mm	49.2	49.2	46.1	48.0	48.3	0.9
L7	3 mm x2 mm	48.7	48.7	45.6	47.5	47.8	0.8
L6	3 mm x2 mm	47.7	47.7	44.0	46.2	46.4	0.9
L1	3 mm x2 mm	45.4	45.4	40.2	42.7	42.7	1.4
L2	3 mm x2 mm	45.9	45.9	41.0	43.4	43.4	1.4
L3	3 mm x2 mm	46.2	46.2	41.3	43.6	43.6	1.5
L4	3 mm x2 mm	45.7	45.7	40.9	43.2	43.2	1.4
L5	3 mm x2 mm	44.9	44.9	39.8	42.2	42.2	1.3
SO-10	7 mm x13 mm	70.2	50.2	43.3	47.8	49.4	1.3

“Archetypal” package

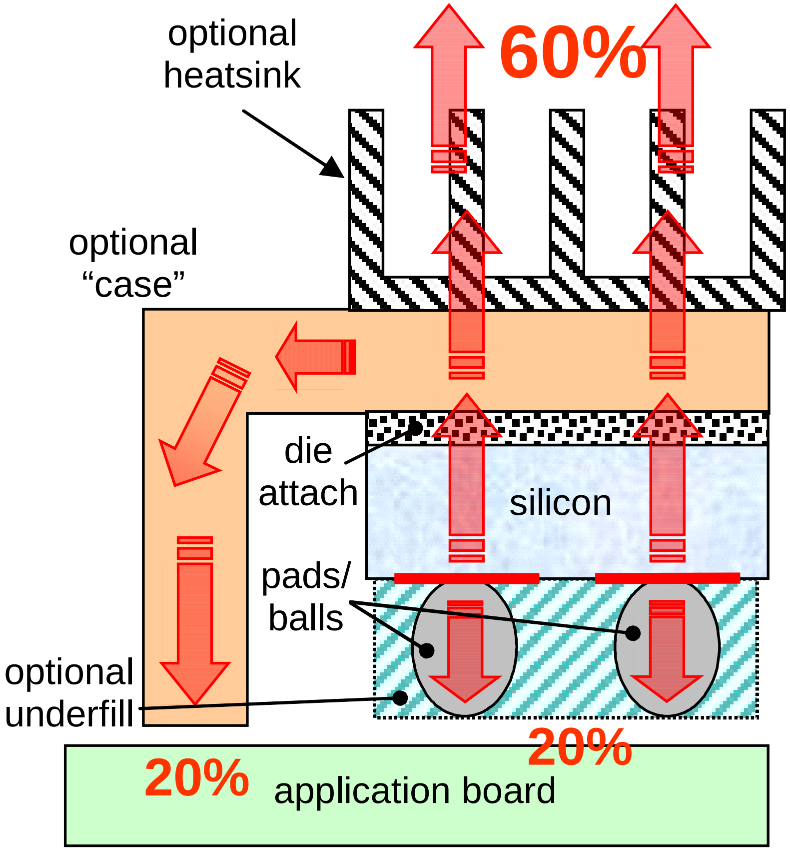


Basic variations on a theme …

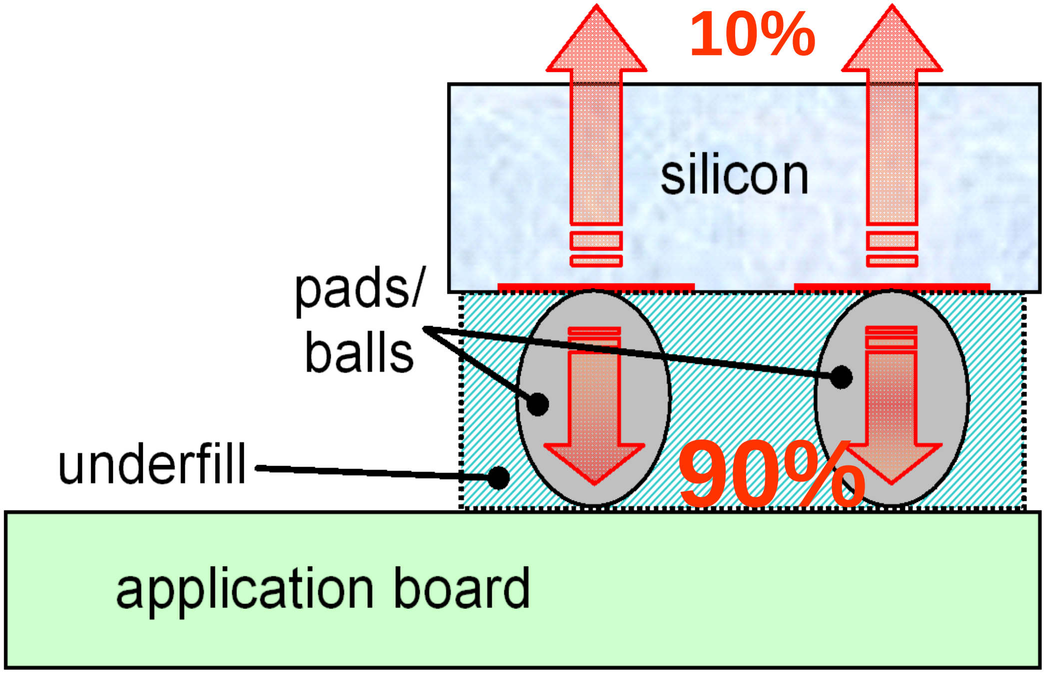
add an external heatsink …



flip the die over …



A bare "flip chip"



Same ref, different values

$\Psi_{J-tab} = 1.2\ °C/W$

$P_d = 50\ W$

$T_c = 25\ °C$

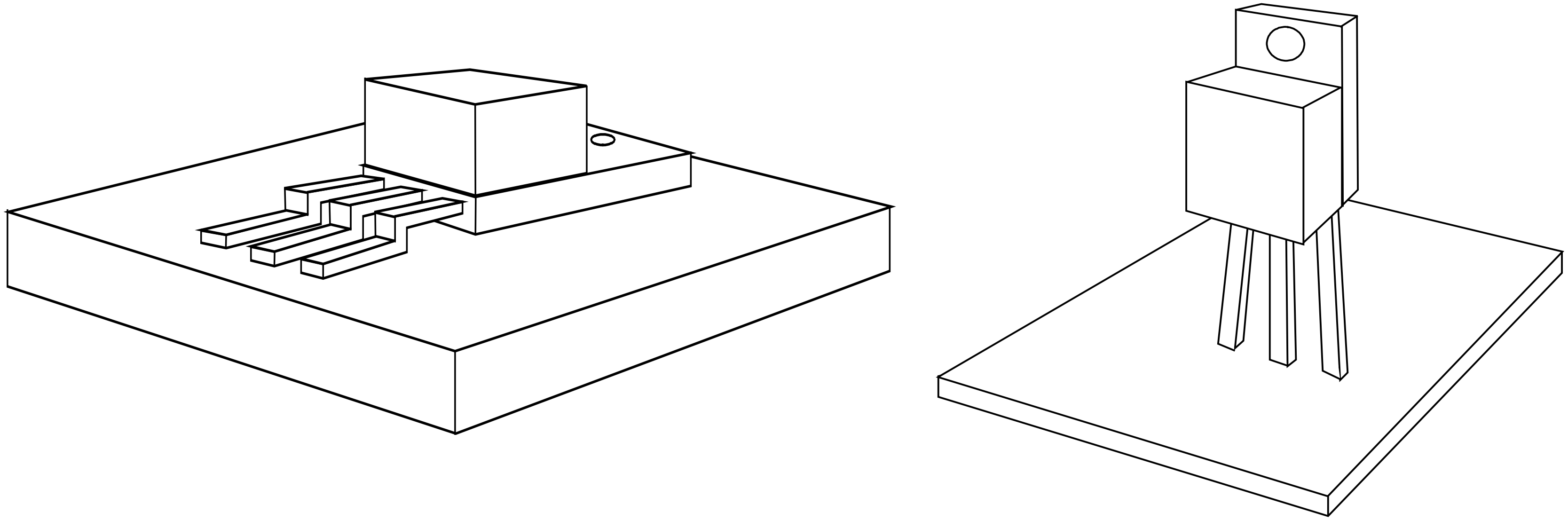
1 GPM of H_2O

$\Psi_{J-tab} = 0.8\ °C/W$

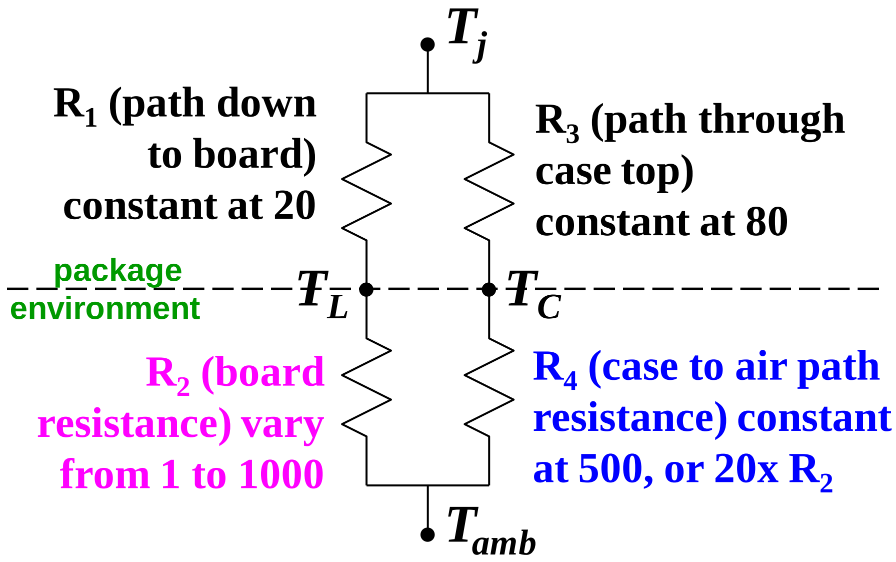
$P_d = 1.5\ W$

$T_c = 25\ °C$

still air



Even when it's constant, it's not!



T_j

R_1 (path down to board) constant at 20

R_3 (path through case top) constant at 80

package

environment

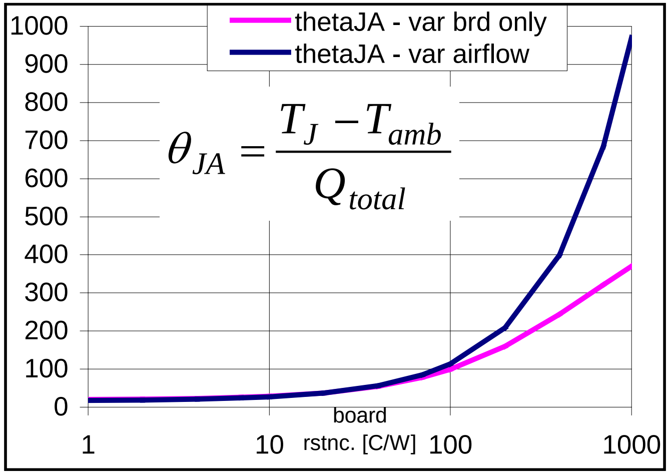
T_L

T_C

R_2 (board resistance) vary from 1 to 1000

R_4 (case to air path resistance) constant at 500, or 20x R_2

T_{amb}

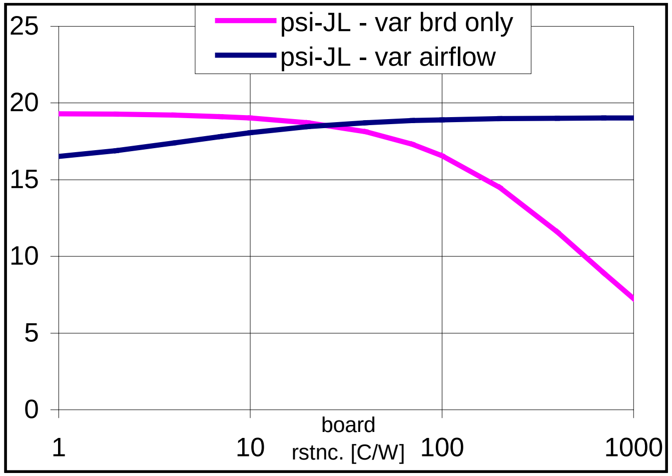


$$\theta_{JA} = \frac{T_J - T_{amb}}{Q_{total}}$$

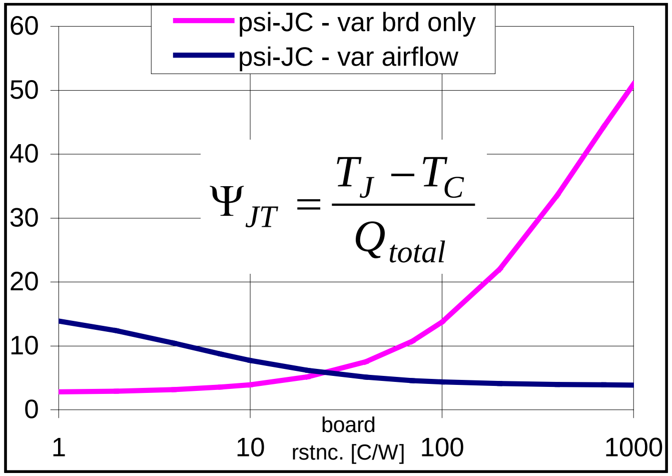
theta-JA

psi-JL

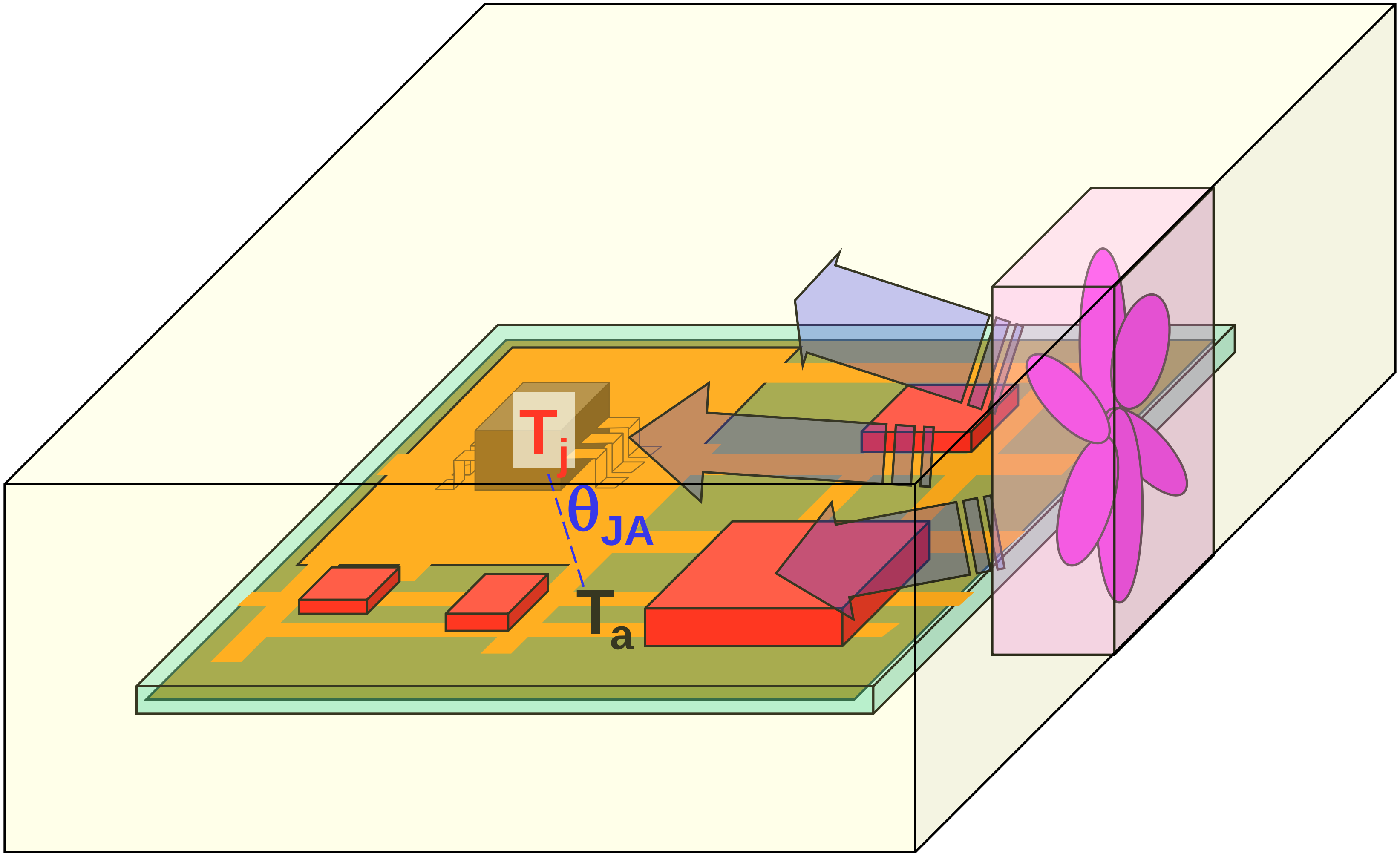
$$\Psi_{JL} = \frac{T_J - T_L}{Q_{total}}$$



psi-JT



$$\Psi_{JT} = \frac{T_J - T_C}{Q_{total}}$$


T_j
θ_{JA}
T_a

Fallacy recap:

"Package resistance" isn't fixed:

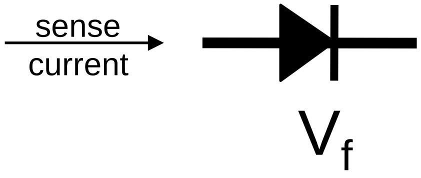
- At the package level itself …
  - – multiple heat paths exiting package
- External to the package …
  - – boundary conditions dictate heat flow
    - Heat sinks
    - Neighboring devices/power dissipation
    - Single vs. double-sided boards
    - Local convection vs. board-edge cooling
    - Multiple layers/power/ground planes

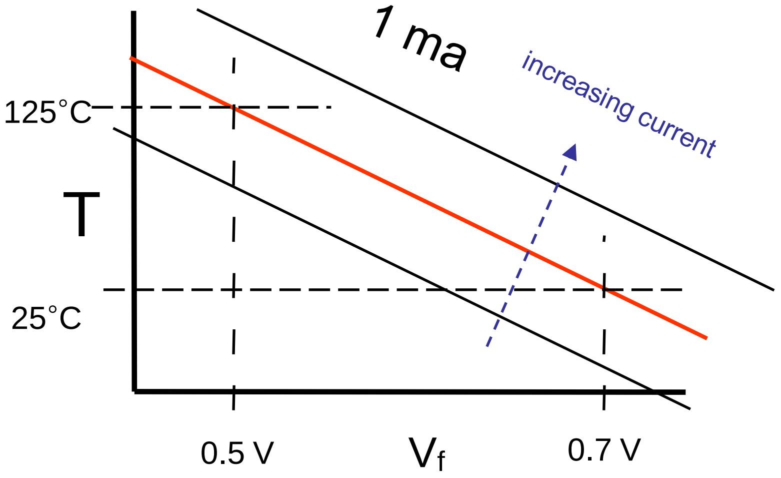
- Therefore, different application environments will see different "package resistance"

Characterization Techniques

Typical TSP behavior

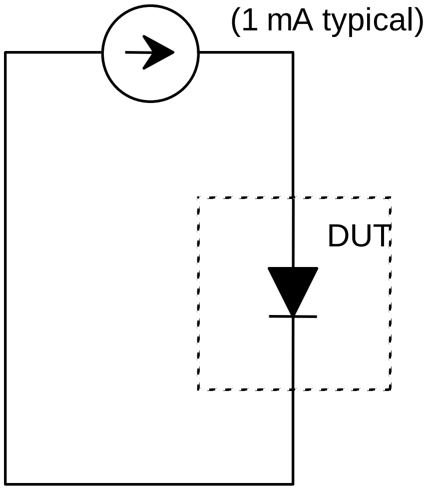
calibrate forward voltage at controlled, small (say 1mA) sense current





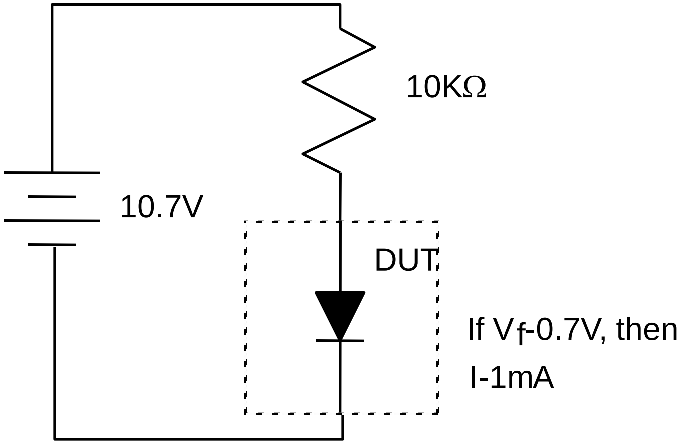
How to measure T_j

true const. current supply



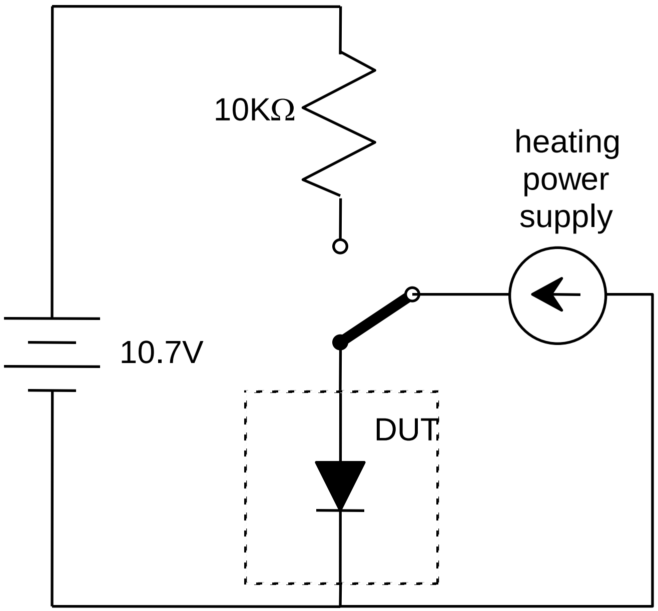
OR

approximate const. current supply



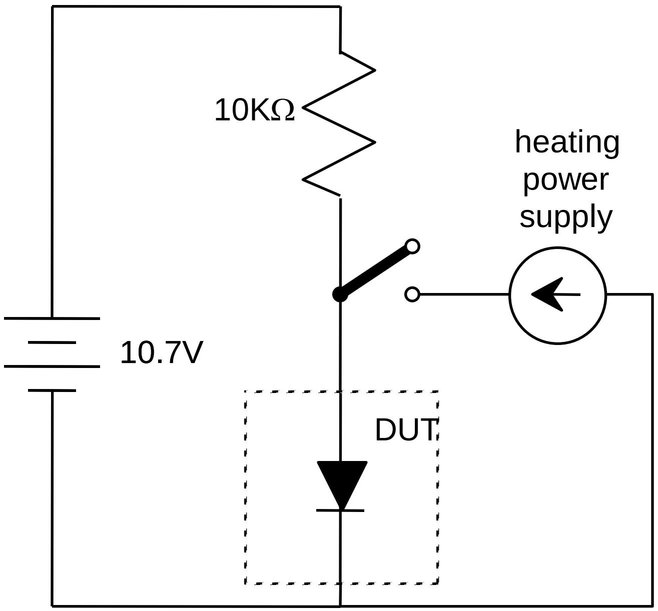
How to heat

sample current is off
while heating current on

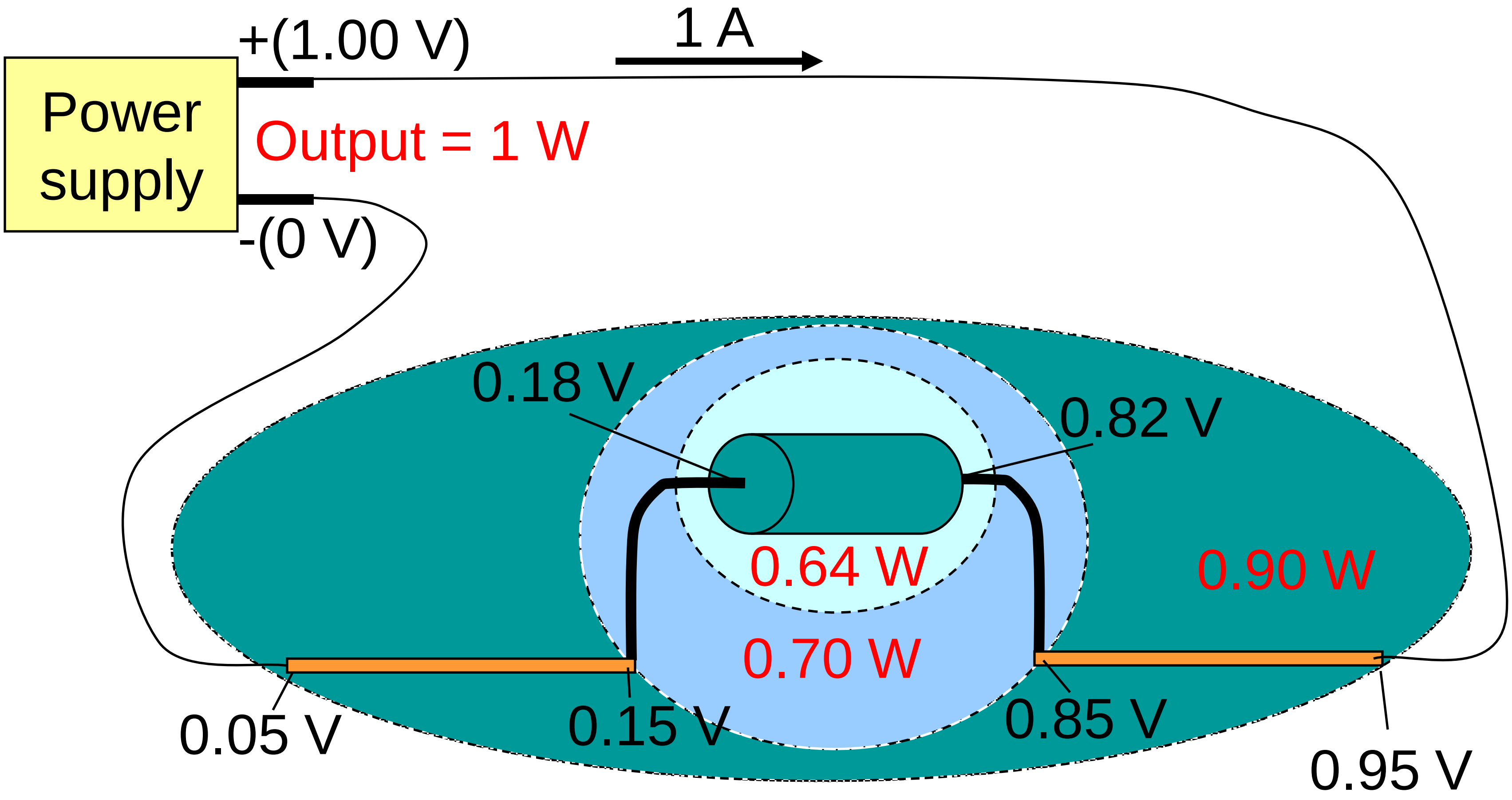


OR

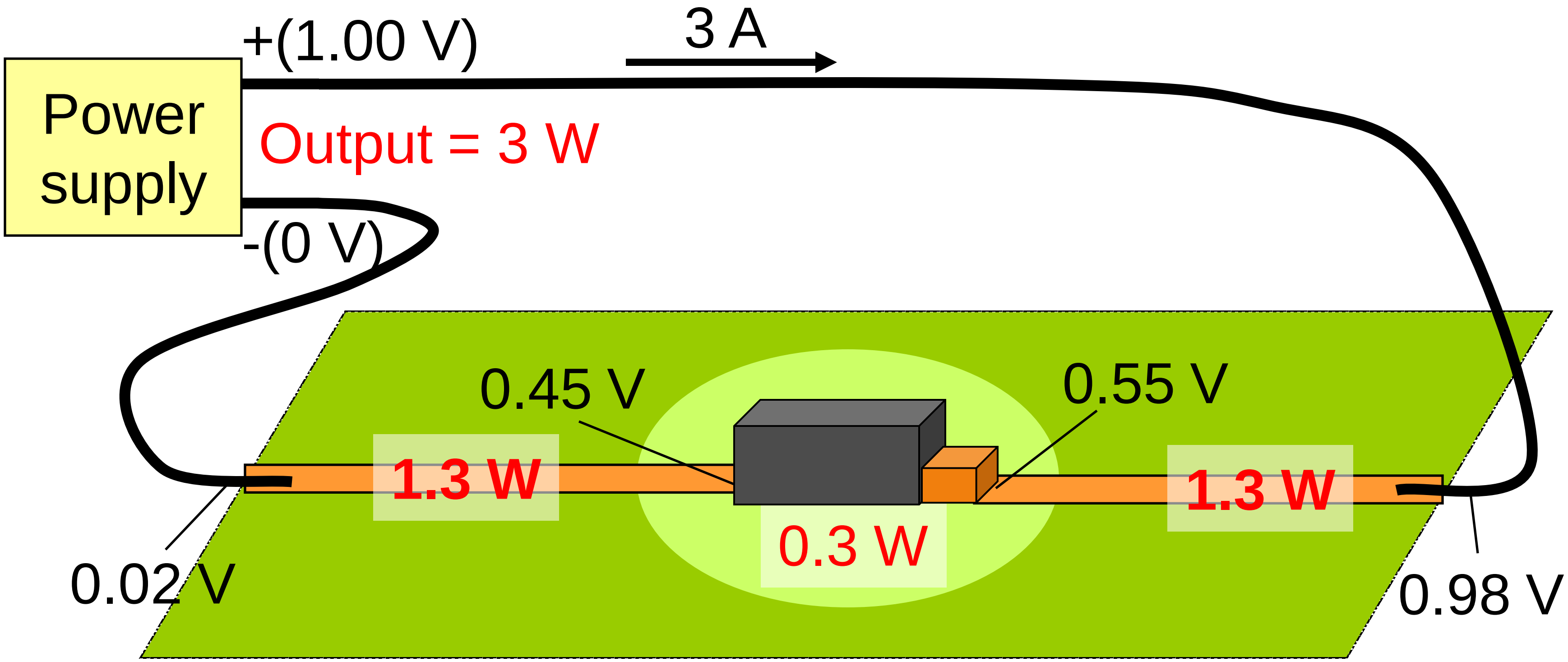
sample current is always on



The importance of 4-wire measurements



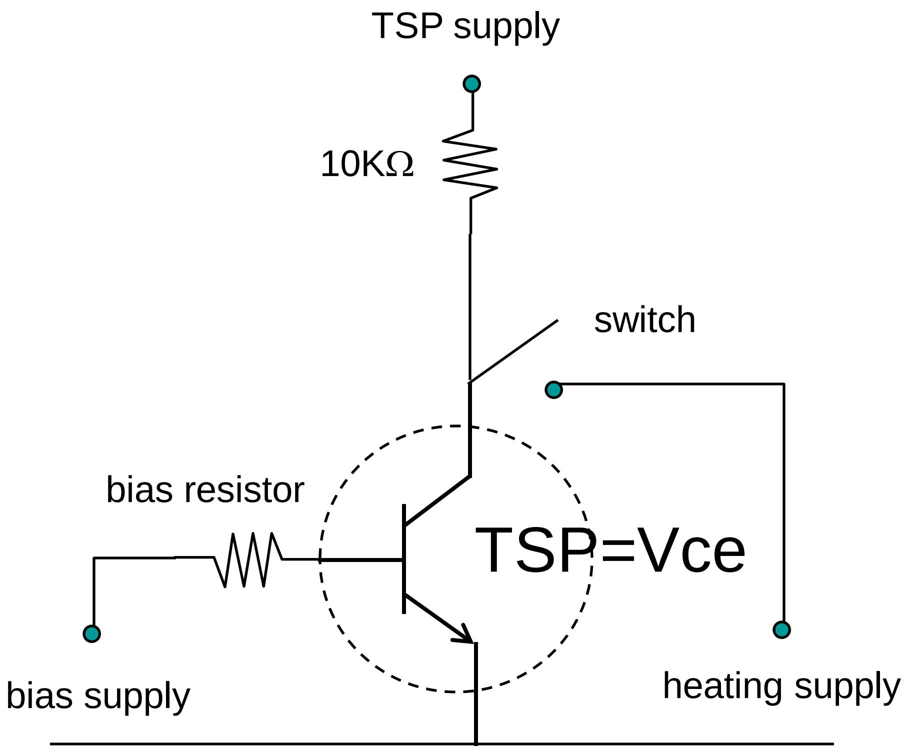
Which raises an interesting question:



Is this a fair characterization of a low-Rds-on device?

Bipolar transistor

- TSP is Vce at designated "constant" current
- Heating is through Vce
- Choose a base current that permits adequate heating

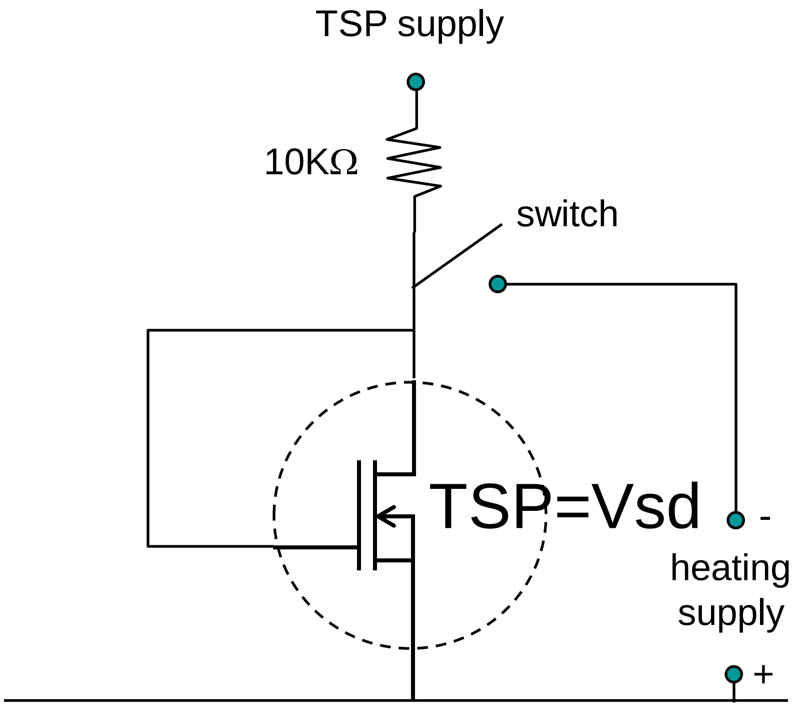


Schottky diode

- TSP is forward voltage at “low” current
- Voltages are typically very small (especially as temperature goes up)
- Highly non-linear, though maybe better as TSP current increases; because voltage is low, higher TSP current may be acceptable
- Heating current will be large

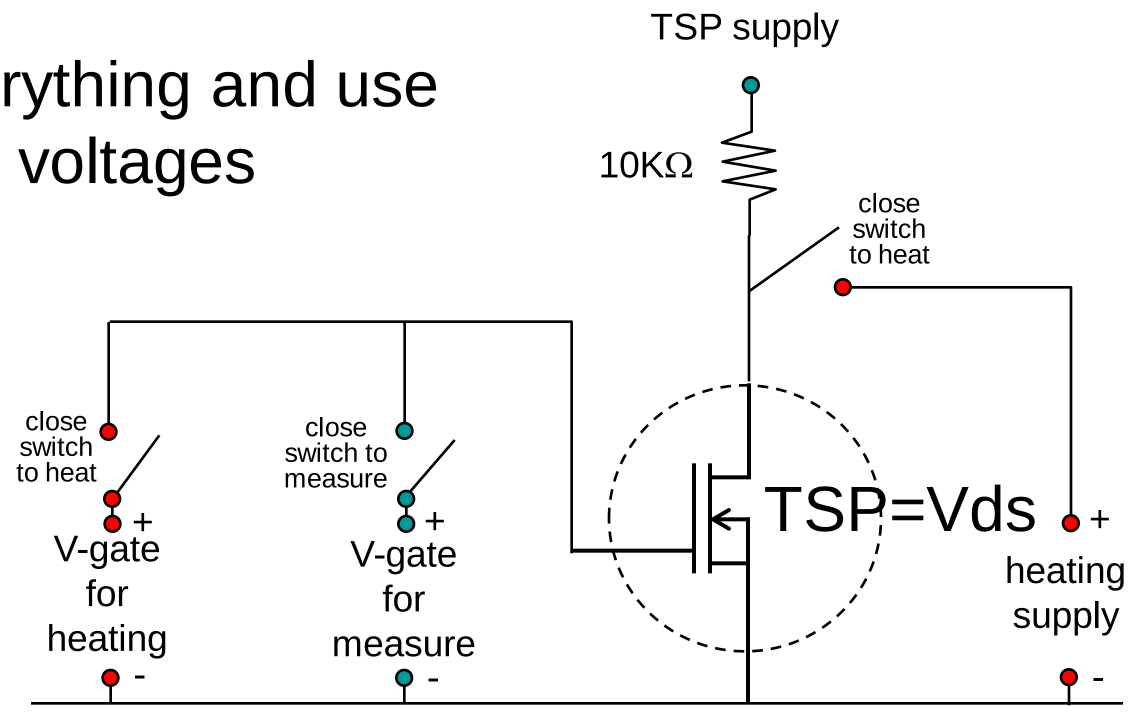
MOSFET / TMOS

- Typically, use reverse bias “back body diode” for both TSP and for heating
- May need to tie gate to source (or drain) for reliable TSP characteristic



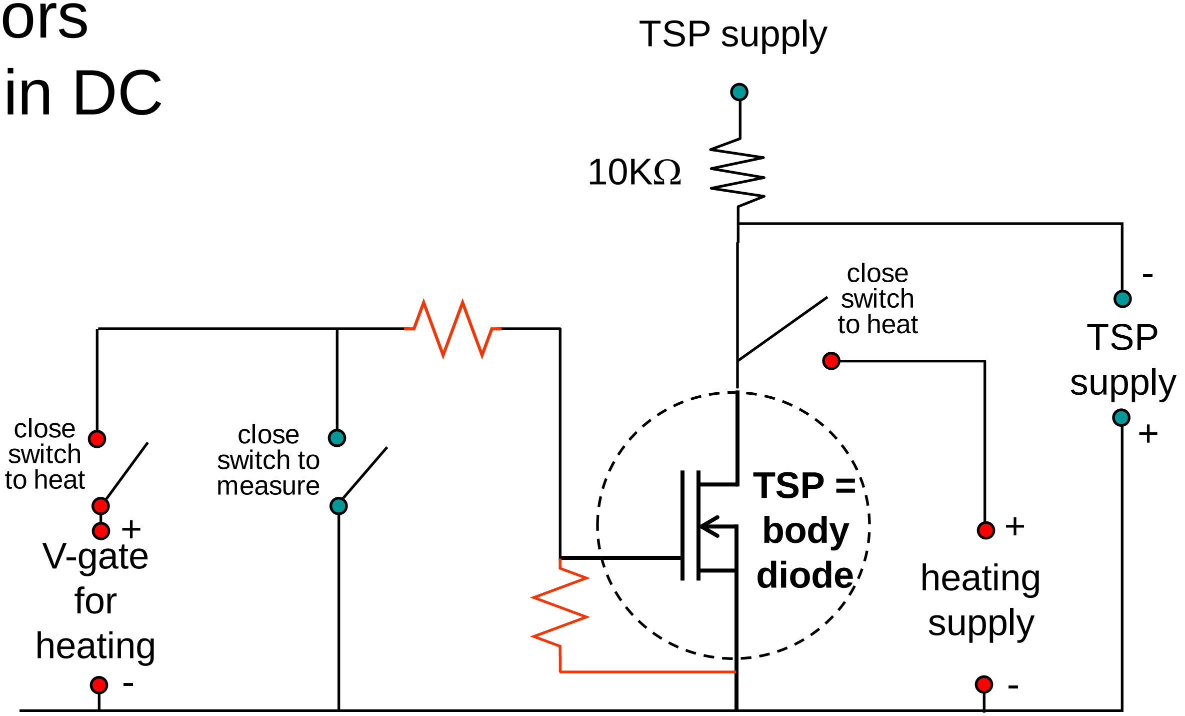
MOSFET / TMOS method 2

- If you have fast switches and stable supplies
- Forward bias everything and use two different gate voltages



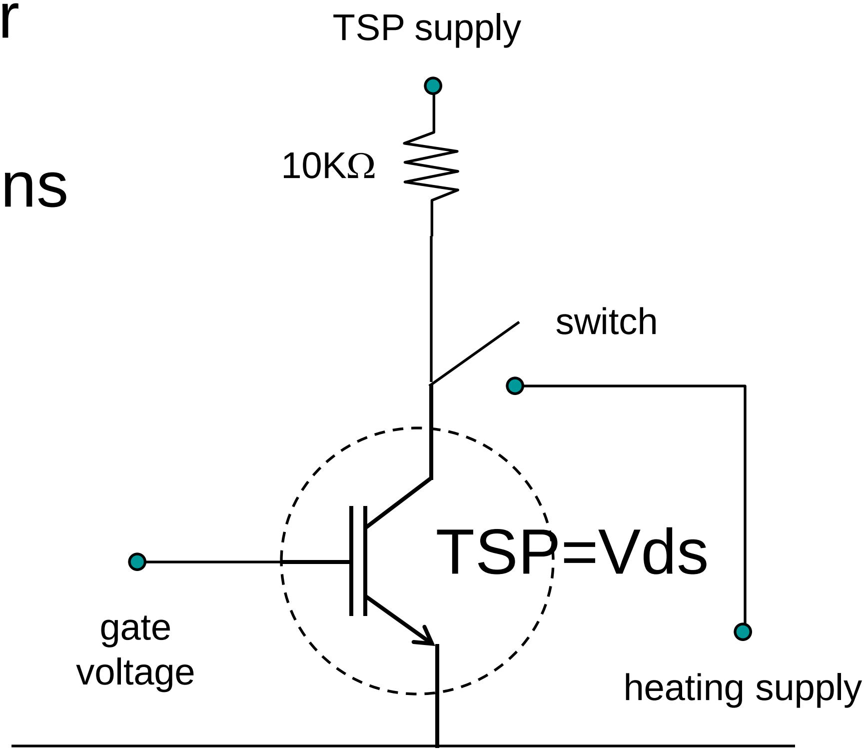
RF MOS

- They exist to amplify high frequencies (i.e. noise)!
- Feedback resistors may keep them in DC



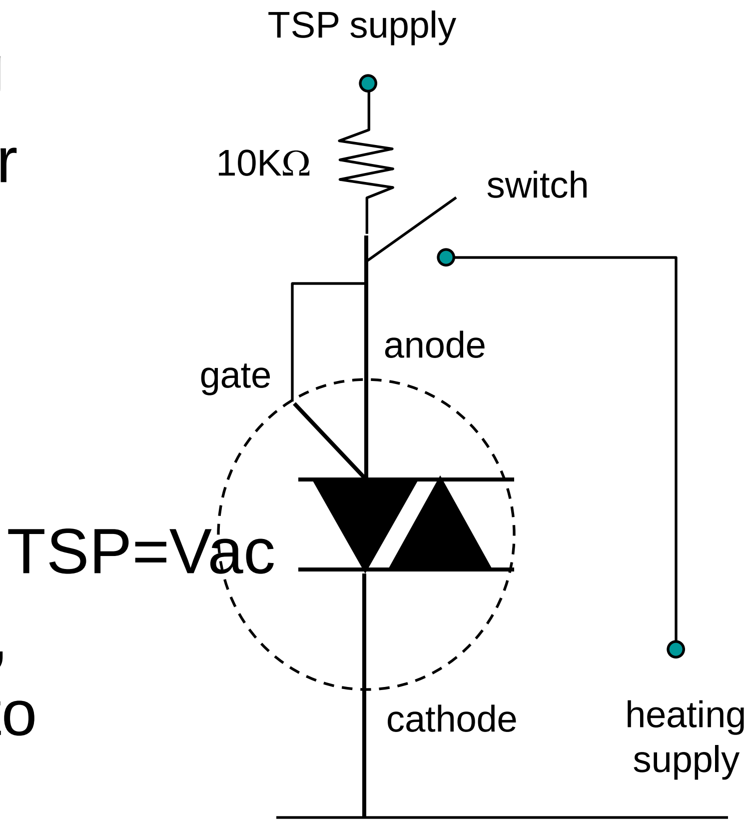
IGBT

- Drain-source channel used for both TSP and heating
- Find a gate voltage which “turns on” the drain-source channel enough for heating purposes
- Use same gate voltage, but typically low TSP current for temperature measurement



Thyristor

- Anode--to-cathode voltage path used both for TSP and for heating
- typical TSP current probably lower than “holding” current, so gate must be turned on for TSP readings; try tying it to the anode (even so, we used 20mA to test SCR2146)
- Hopefully, with anode tied to gate, enough power can be dissipated to heat device without exceeding gate voltage limit



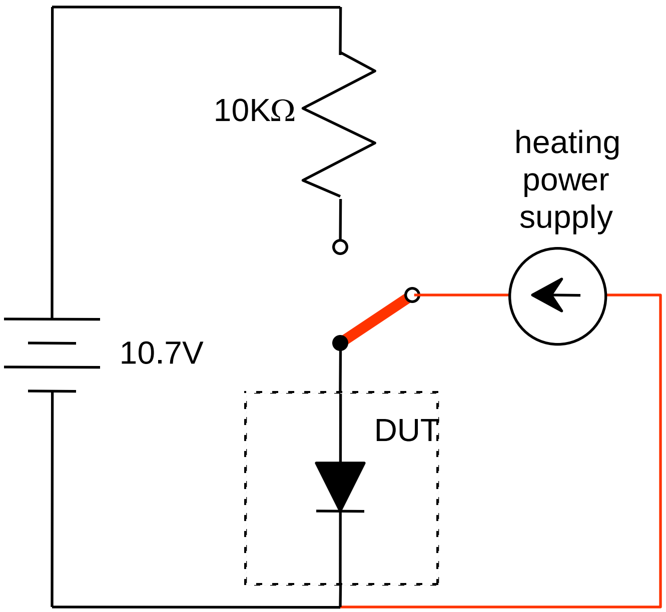
Logic and analog

- Find any TSP you can
  - – ESD diodes on inputs or outputs
  - – Body diodes somewhere
- Heat wherever you can
  - – High voltage limits on Vcc, Vee, whatever
  - – Body diodes or output drivers
  - – Live loads on outputs
    - (be very careful how you measure power!)

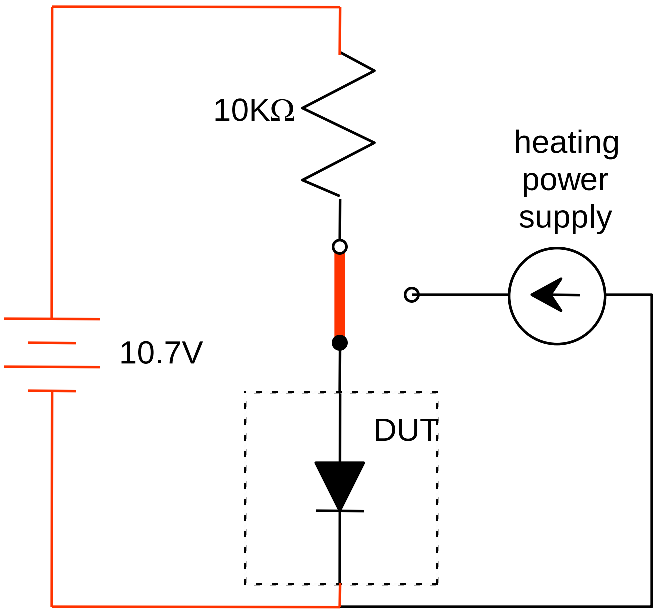
Heating curve method
vs.
cooling curve method

Quick review:
Basic T_j measurement

first we heat



then we measure



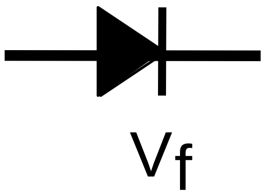
Question

- What happens when you switch from “heat” to “measure”?

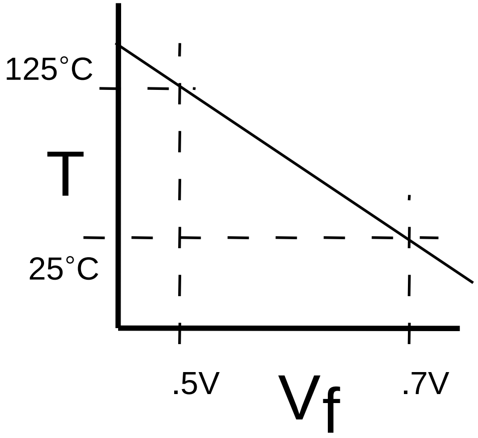
Answer: stuff changes

- More specifically, the junction starts to cool down

Basic
“heating curve”
transient method

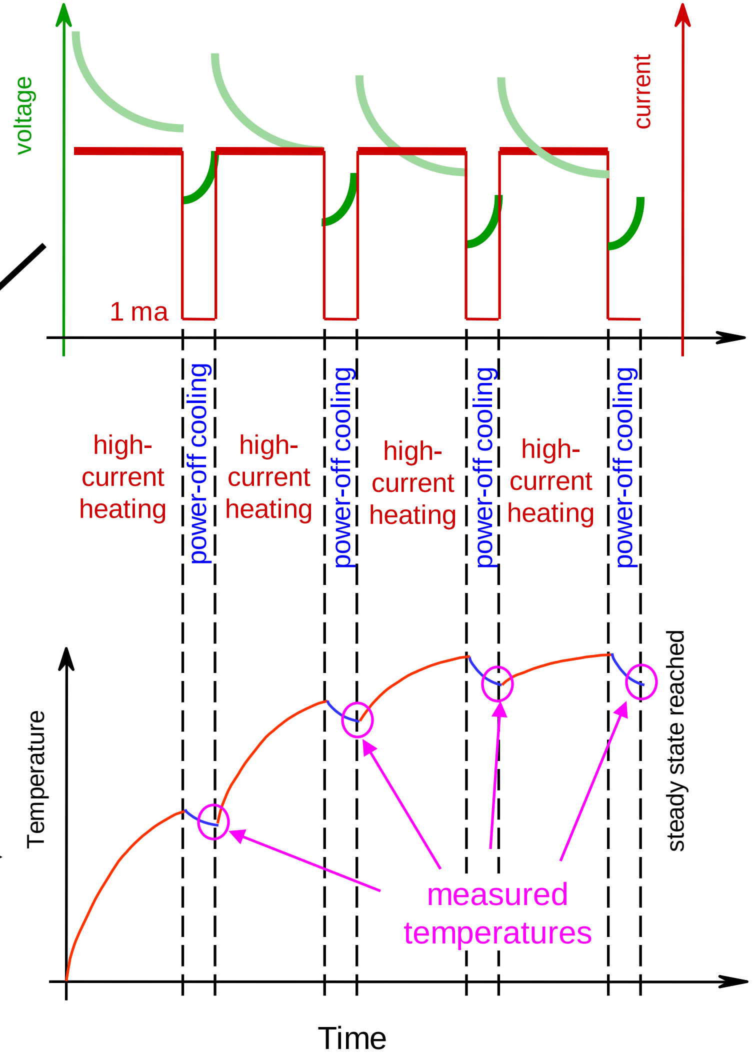


calibrate forward voltage
@ 1mA sense current

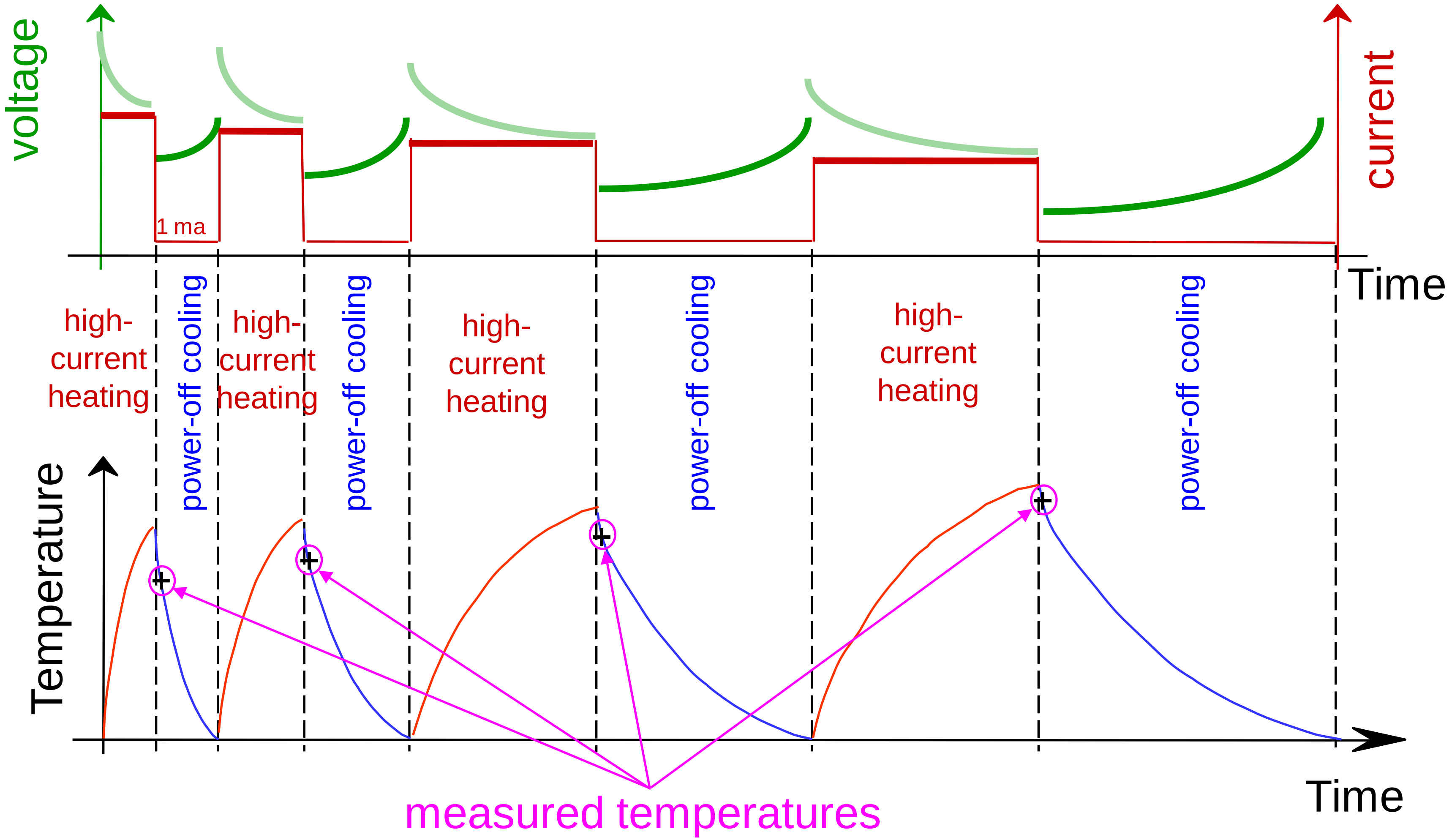


convert cooling
volts to
temperature

measurements

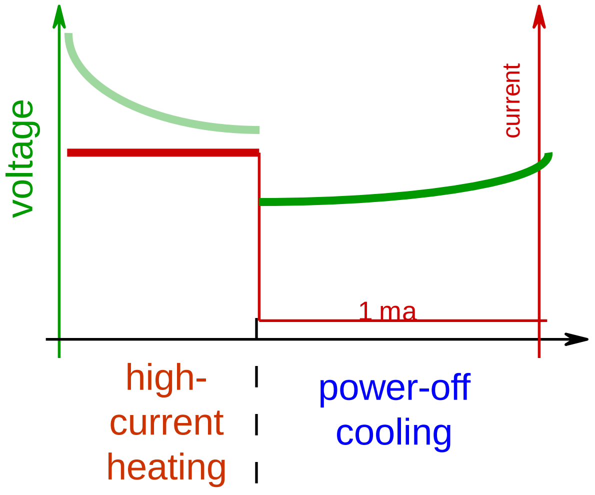


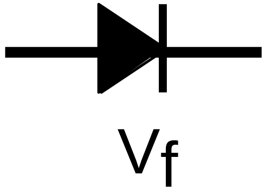
Heating curve method #2



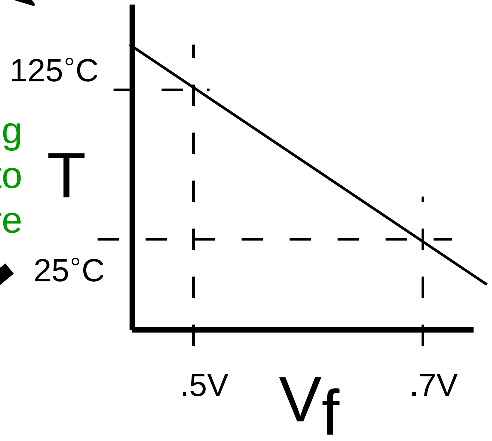
Basic “cooling curve” transient method

measurements

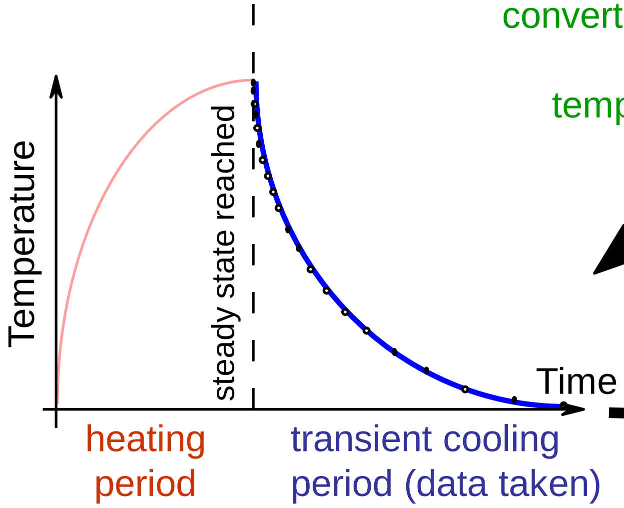




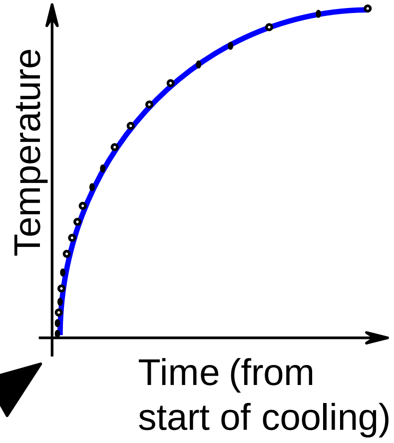
calibrate forward voltage @ 1mA sense current



convert cooling volts to temperature



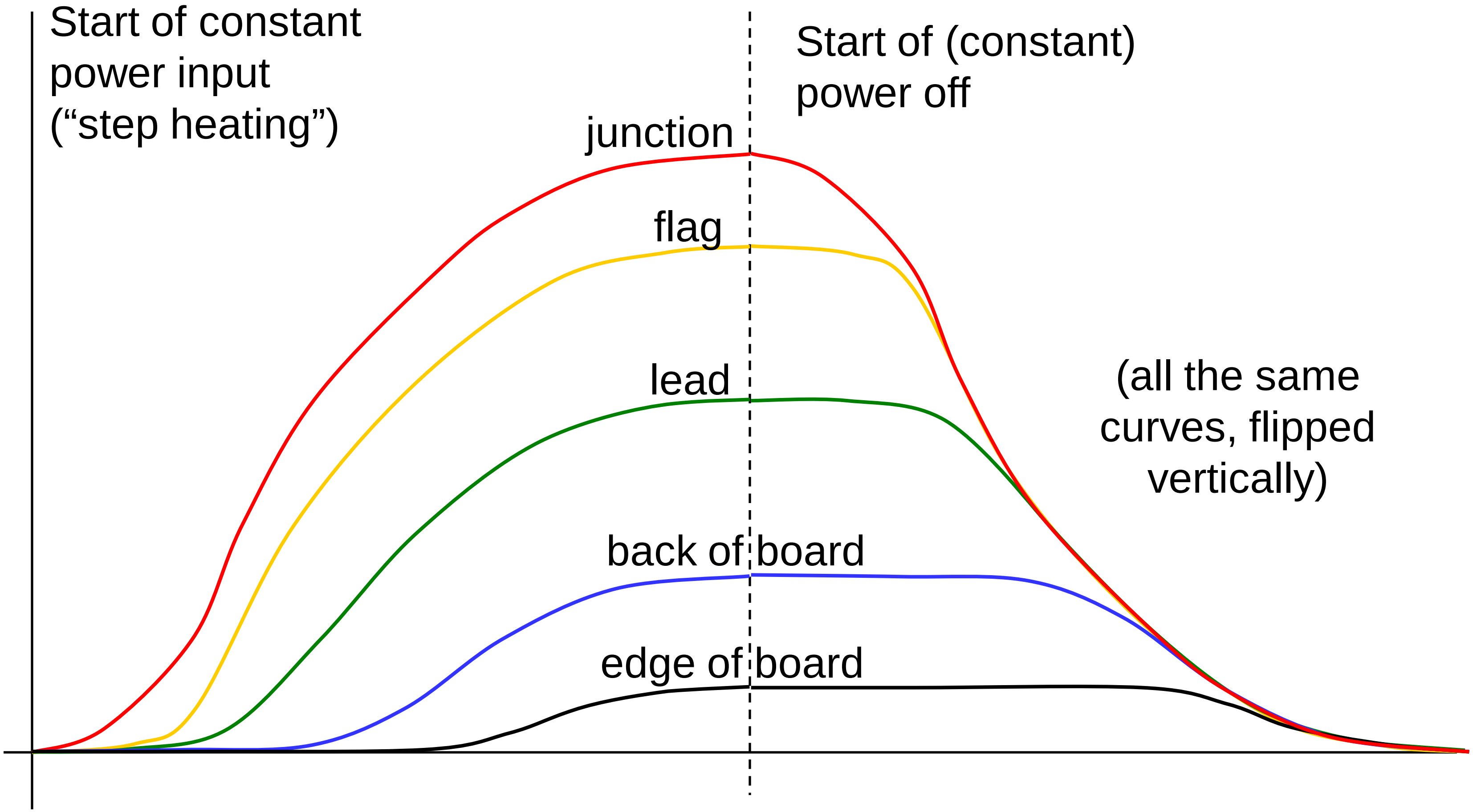
subtract cooling curve from peak temperature to obtain “heating” curve equivalent



Whoa!
… that last step there …

- Heating vs. cooling
  - Physics is symmetric, as long as the material and system properties are independent of temperature

Heating vs. cooling symmetry



A (perhaps) subtle point …

- For a theoretically valid cooling curve, you must begin at true thermal equilibrium (not uniform temperature, but steady state)
- So whatever your $\boldsymbol{\theta_{JA}}$, max power is limited to:

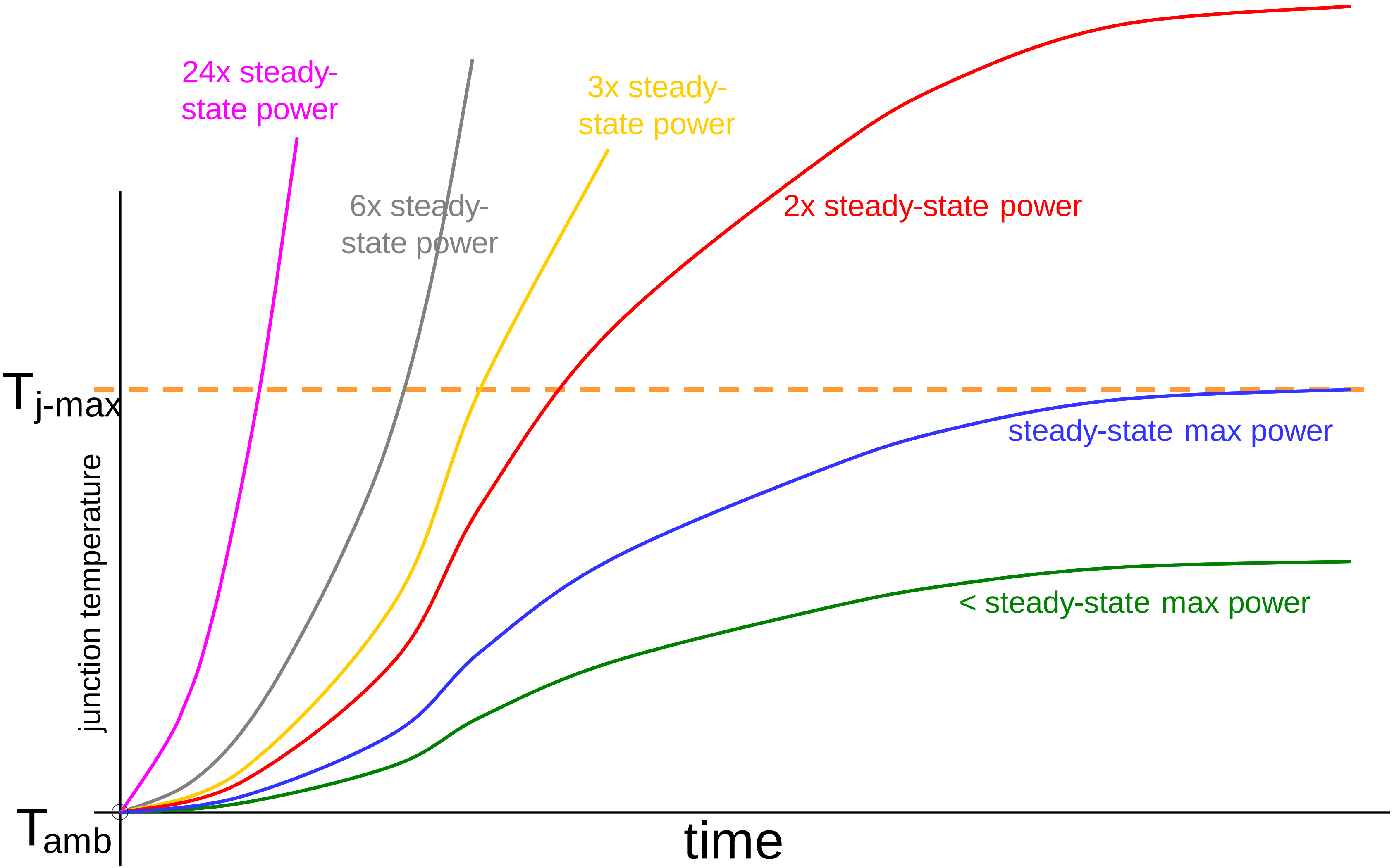
$$power = \frac{T_{j\max} - T_{\text{ambient}}}{\theta_{JA}}$$

By the way …
Steady-state vs. transient ?

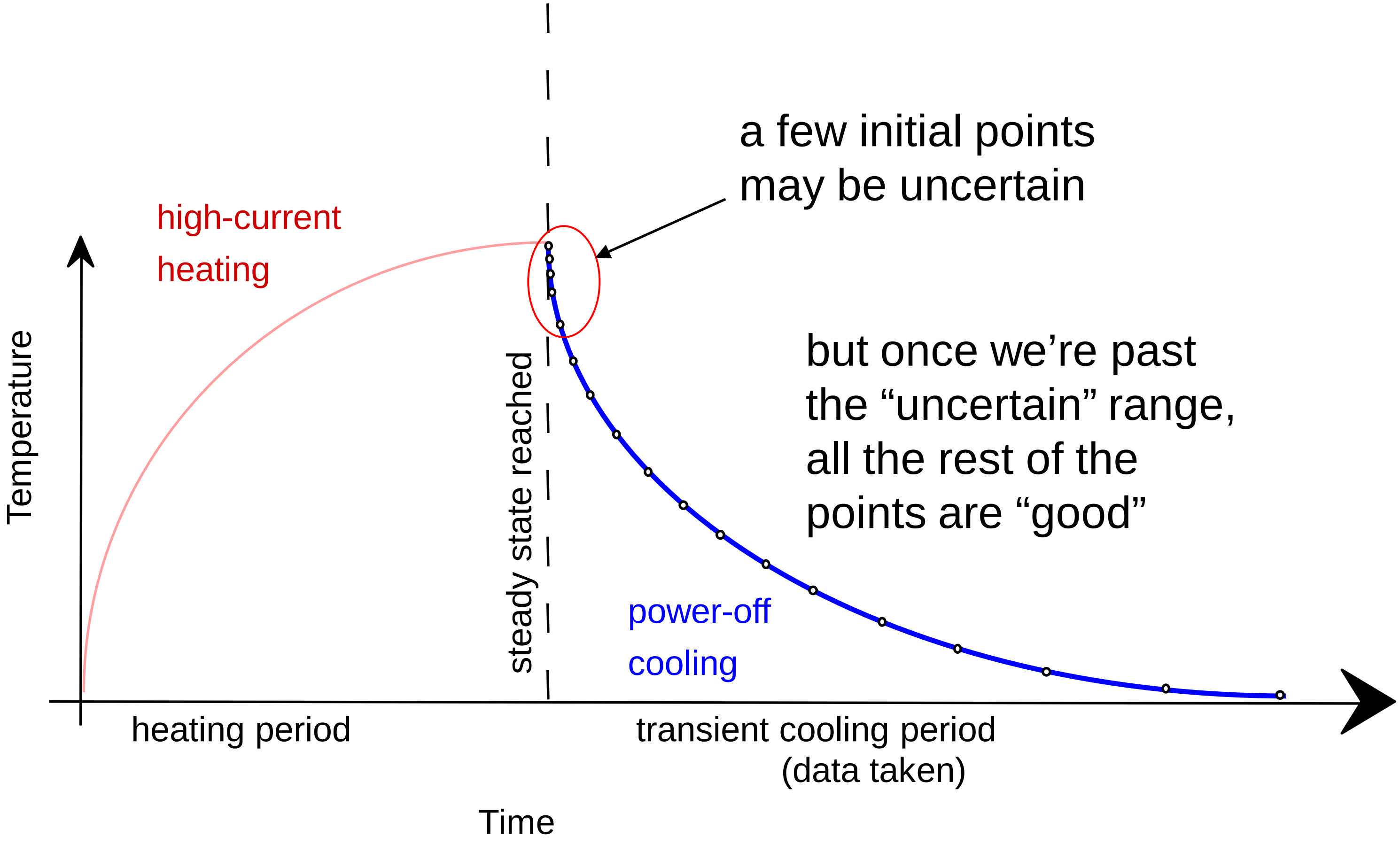
- Since you must have the device at steady state in order to make a full transient cooling-curve measurement, steady-state θ_{JA} is a freebie.

  (given that you account for the slight cooling which took place before your first good measurement occurred)

Effect of power on heating curve



Some initial uncertainty



a few initial points
may be uncertain

but once we’re past
the “uncertain” range,
all the rest of the
points are “good”

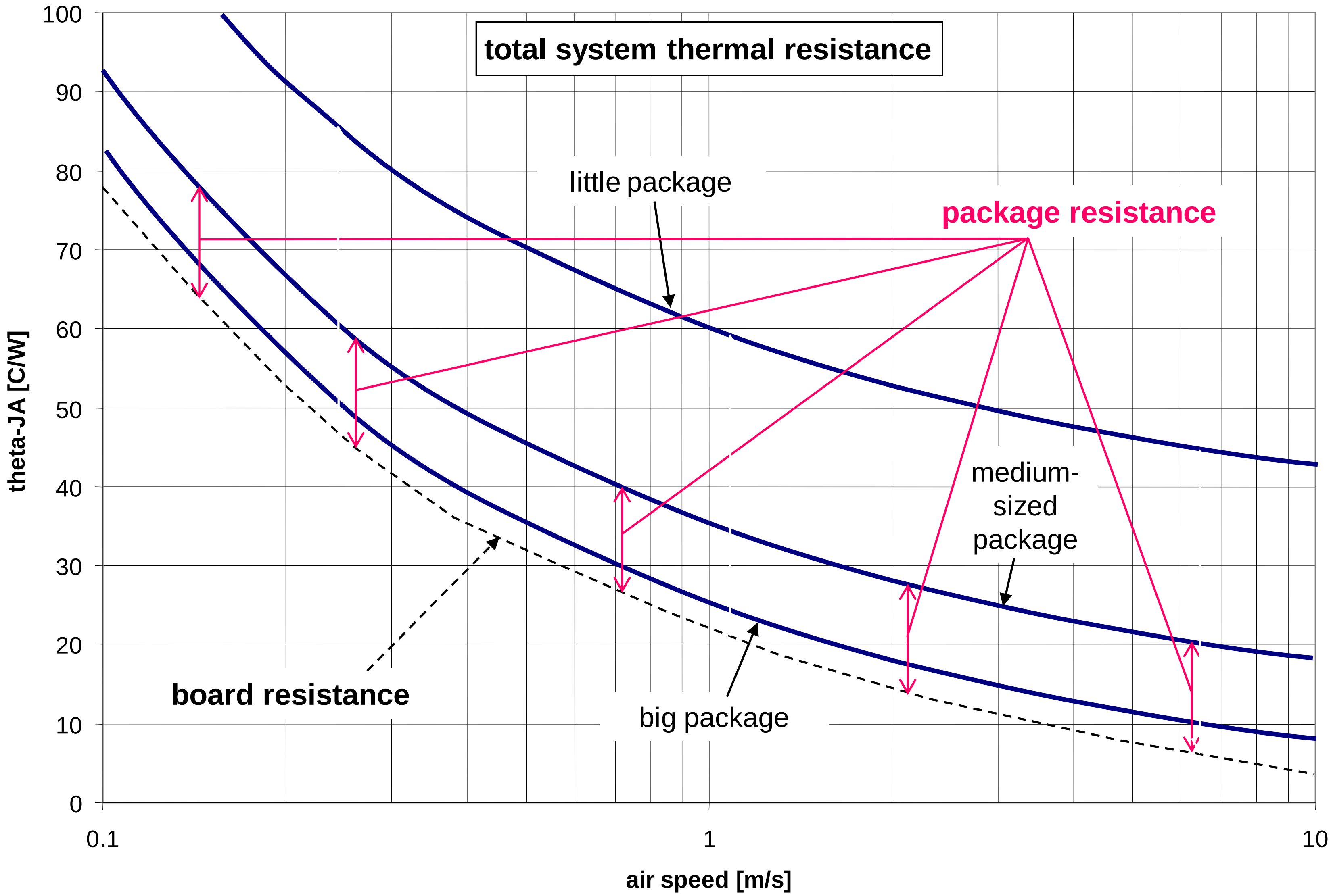
Heating vs. cooling tradeoffs

	HEATING	COOLING
starting temperature	ambient	?
heating power	limited by tester	limited to steady-state
temperature of fastest data	closer to ambient	closer to $T_{j\text{-max}}$
error control	all points similar error	error limited to first few points

Still air vs. moving air

- Varying the air speed is mainly varying the heat loss from the test board surface area, not from the package itself
- You just keep re-measuring your board’s characteristics

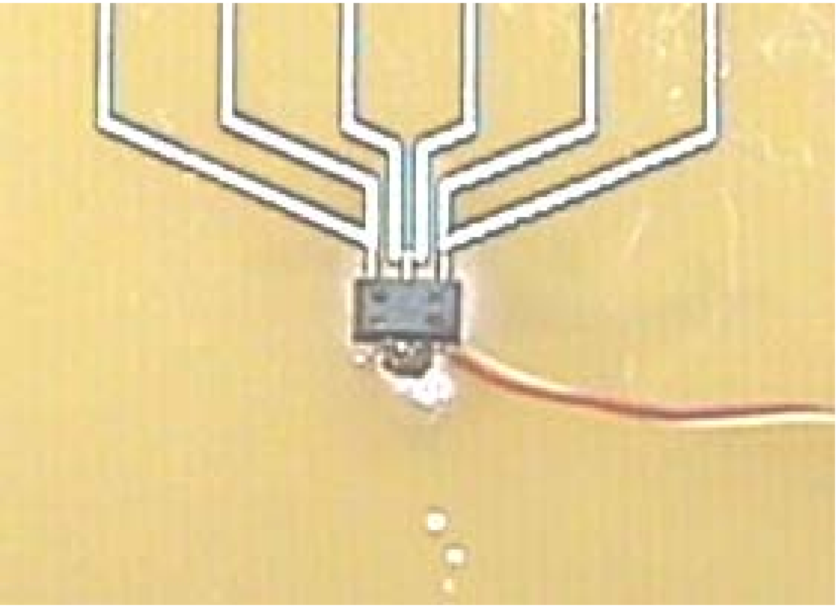
Typical theta-vs.-air speed chart

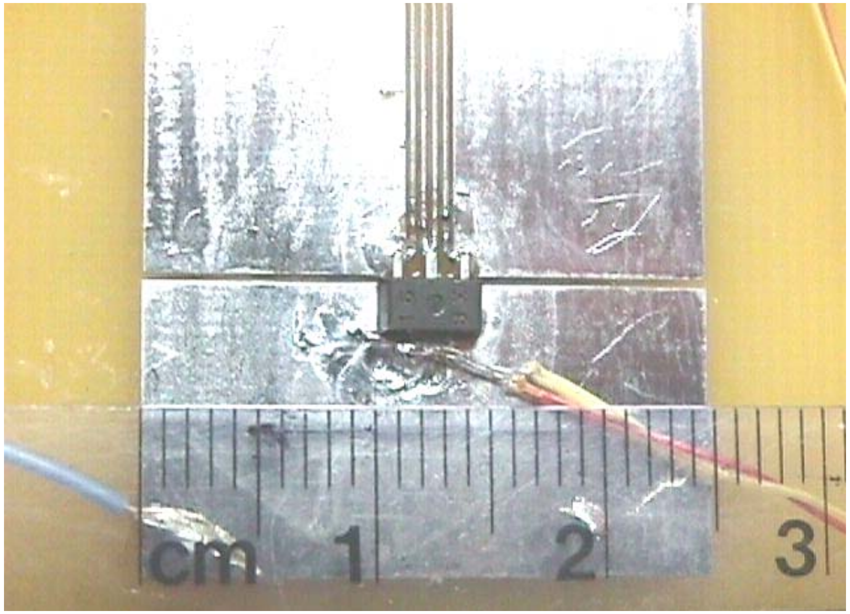


Different boards

- Min-pad board
- 1” heat spreader board
- You’re mainly characterizing how copper area affects *every* package and board, not how a *particular* package depends on copper area

Typical thermal test board types



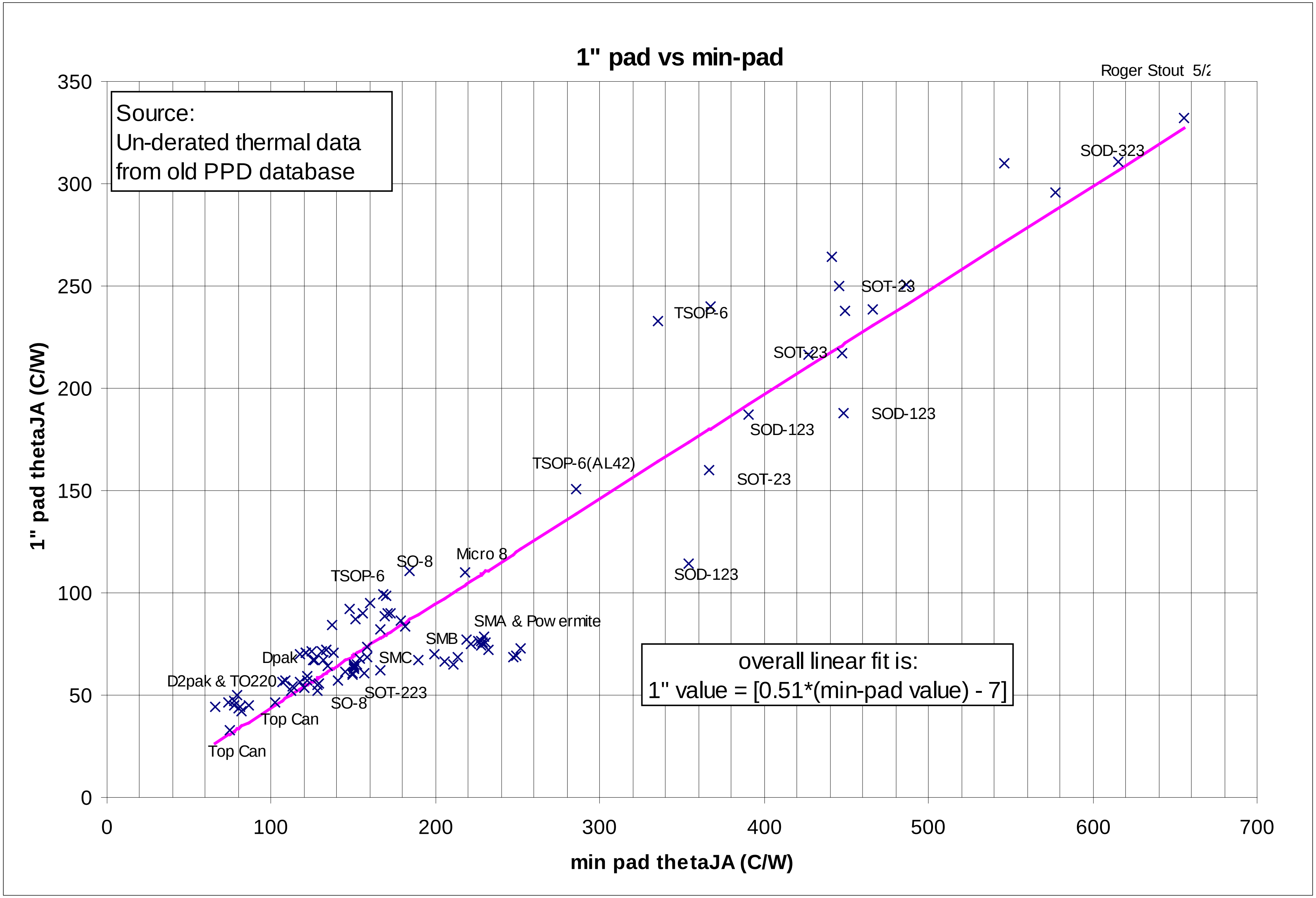


Min-pad board

Minimum metal area to attach device (plus traces to get signals and power in and out)

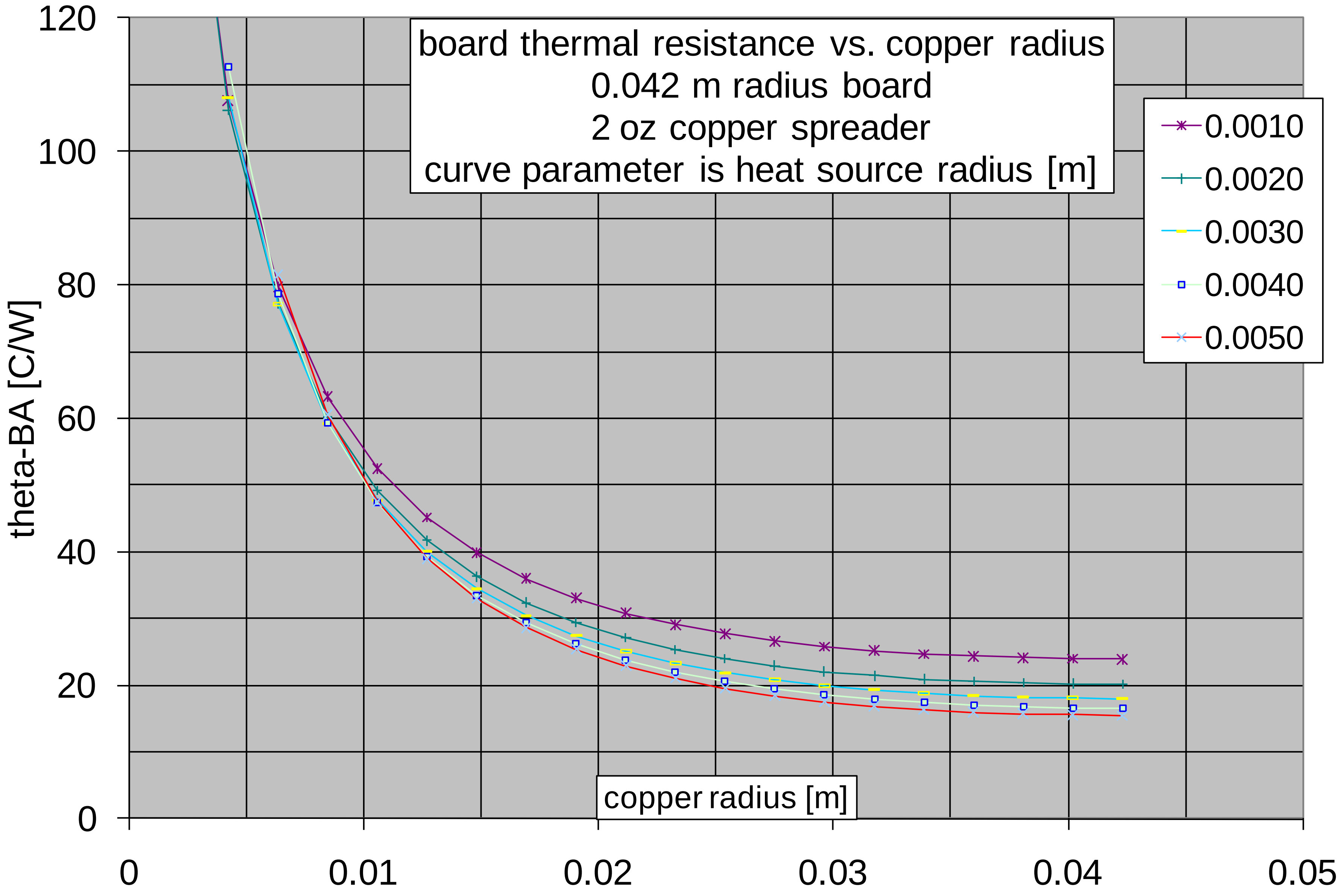
1-inch-pad board

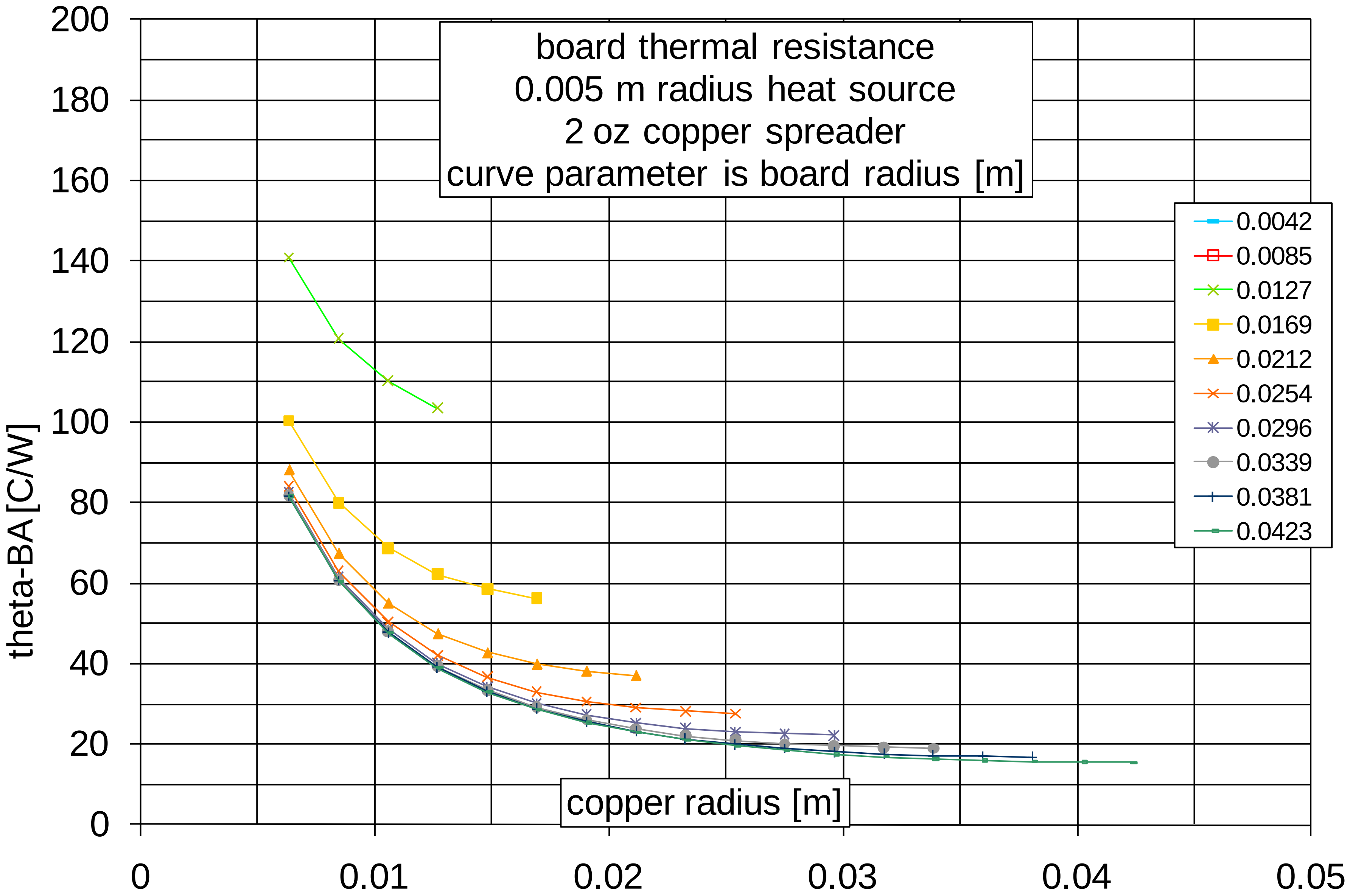
Device at center of 1”x1” metal area (typically 1-oz Cu); divided into sections based on lead count



Source:
Un-derated thermal data
from old PPD database

overall linear fit is:
1" value = [0.51*(min-pad value) - 7]


board thermal resistance vs. copper radius
0.042 m radius board
2 oz copper spreader
curve parameter is heat source radius [m]
theta-BA [C/W]
0
20
40
60
80
100
120
copper radius [m]
0
0.01
0.02
0.03
0.04
0.05
0.0010
0.0020
0.0030
0.0040
0.0050


board thermal resistance
0.005 m radius heat source
2 oz copper spreader
curve parameter is board radius [m]
theta-BA [C/W]
copper radius [m]
200
180
160
140
120
100
80
60
40
20
0
0
0.01
0.02
0.03
0.04
0.05
0.0042
0.0085
0.0127
0.0169
0.0212
0.0254
0.0296
0.0339
0.0381
0.0423

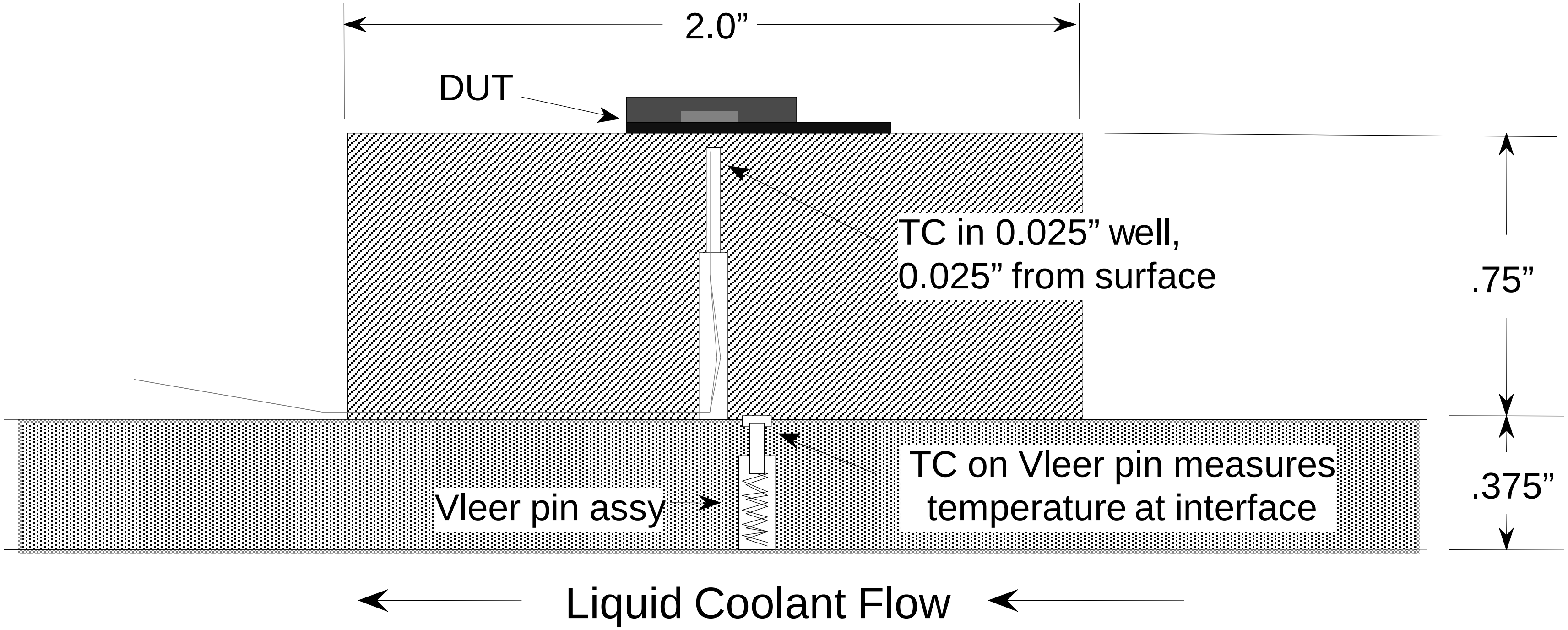
Standard coldplate testing

- “infinite” heatsink (that really isn’t) for measuring theta-JC on high-power devices

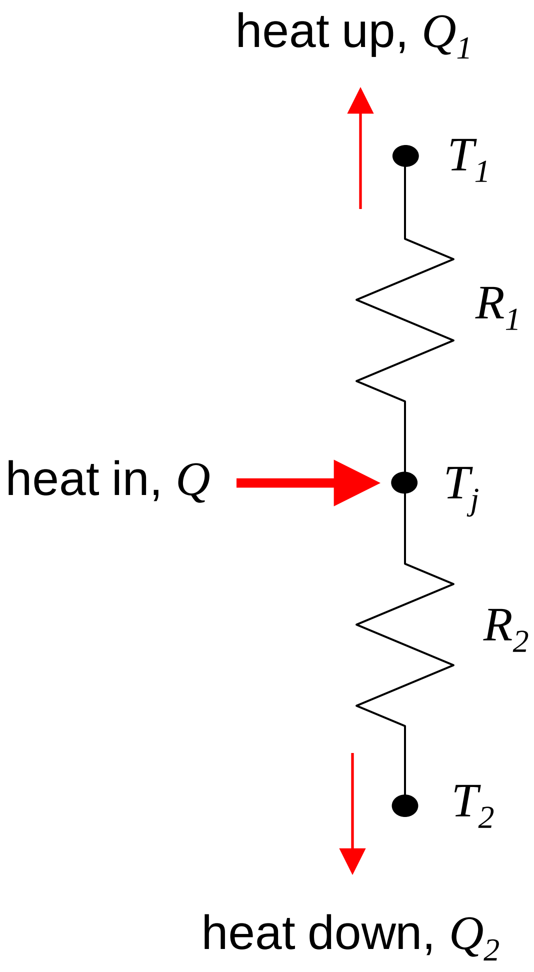
- If both power and coldplate temperature are independently controlled, “two parameter” compact models may be created

Standard coldplate testing

- Detailed design and placement of “case” TC can have *significant* effect on measured value



2-parameter data reduction



$$Q = Q_1 + Q_2$$

$$Q = \frac{1}{R_1}\left(T_j - T_1\right) + \frac{1}{R_2}\left(T_j - T_2\right)$$

This has the form of a two-variable linear equation:

$$y = m_1 x_1 + m_2 x_2 + b$$

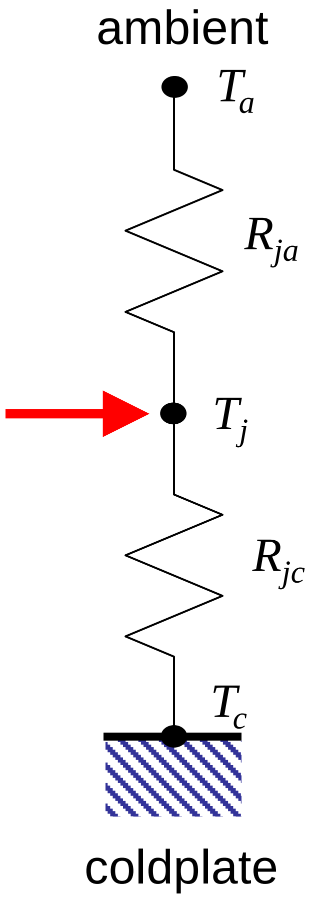
where:

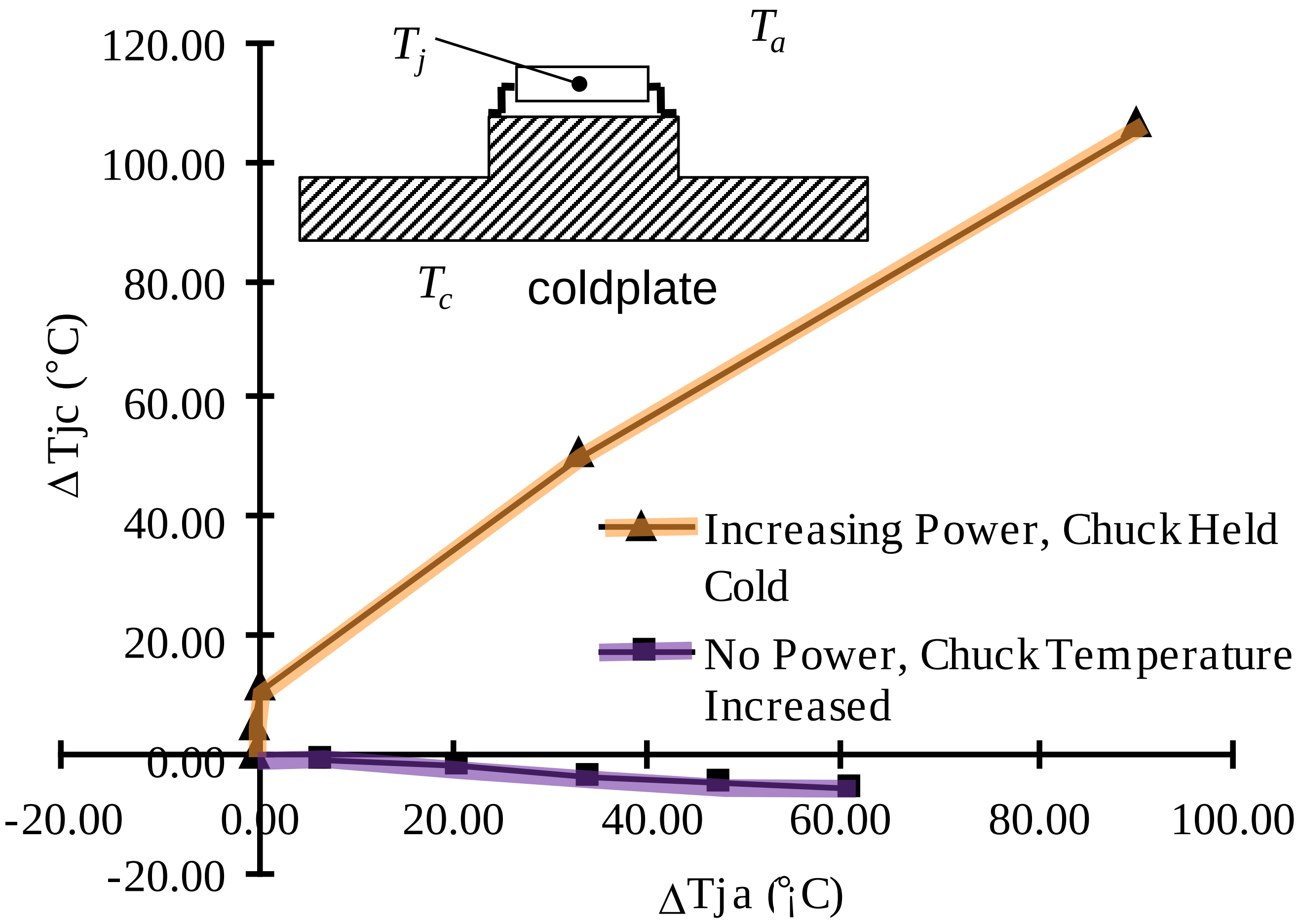
$$m_1 = \frac{1}{R_1} \qquad x_1 = \left(T_j - T_1\right)$$

$$m_2 = \frac{1}{R_2} \qquad x_2 = \left(T_j - T_2\right)$$

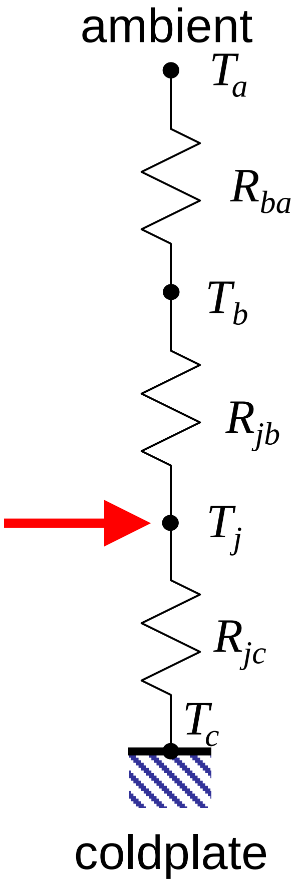
$$b \equiv 0$$

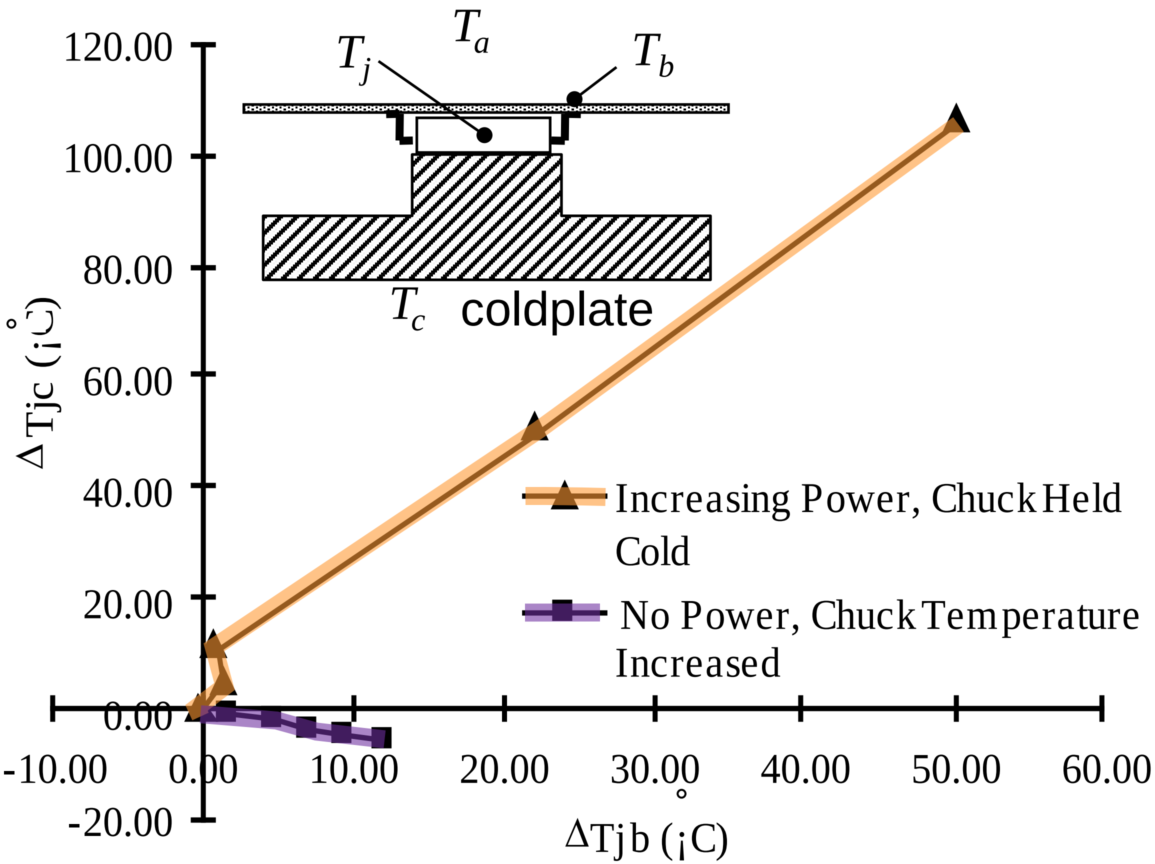
A “single coldplate” test





A “single coldplate” test, package down

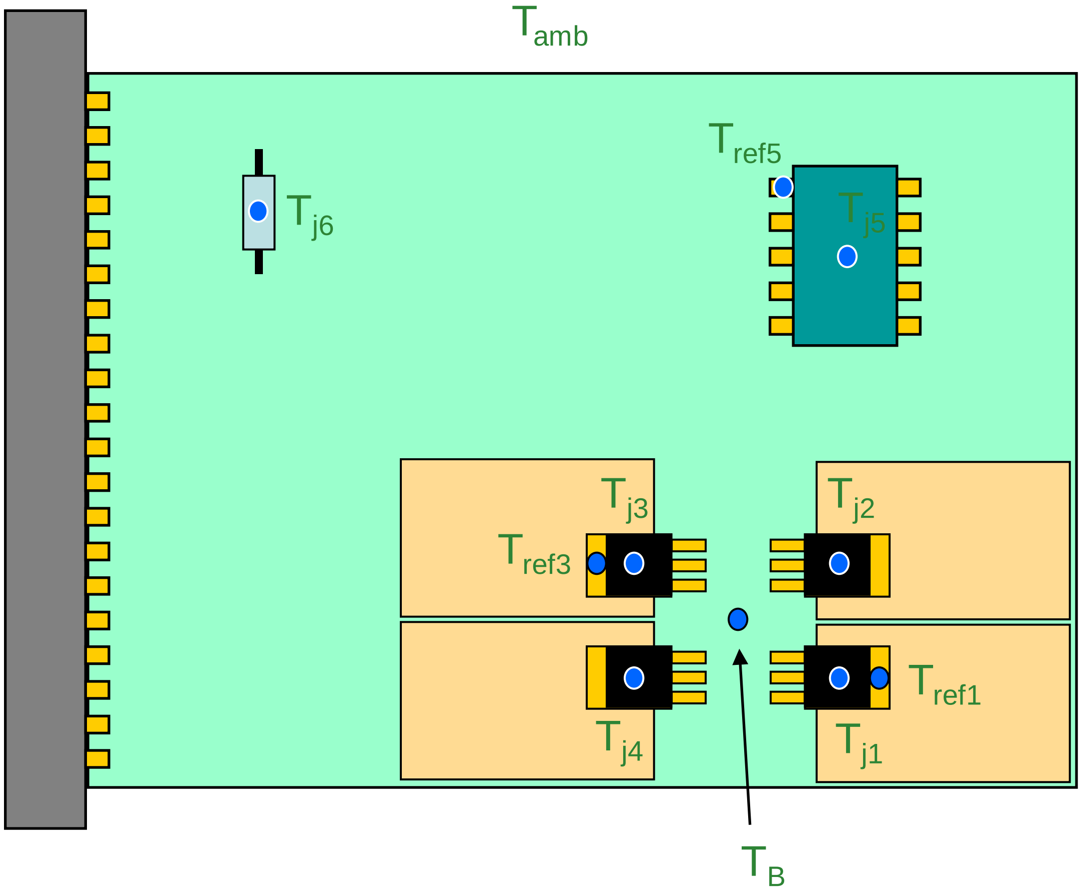




Linear superposition

- What is it?
  - The total response of a point within the system, to excitations at all points of the system, is the sum of the individual responses to each excitation taken independently.
- When does it apply?
  - The system must be “linear” – in brief, all responses must be proportional to all excitations.
- When would you use it?
  - When you have multiple heat sources (that is, all the time!)

Linear superposition – how do you use it?

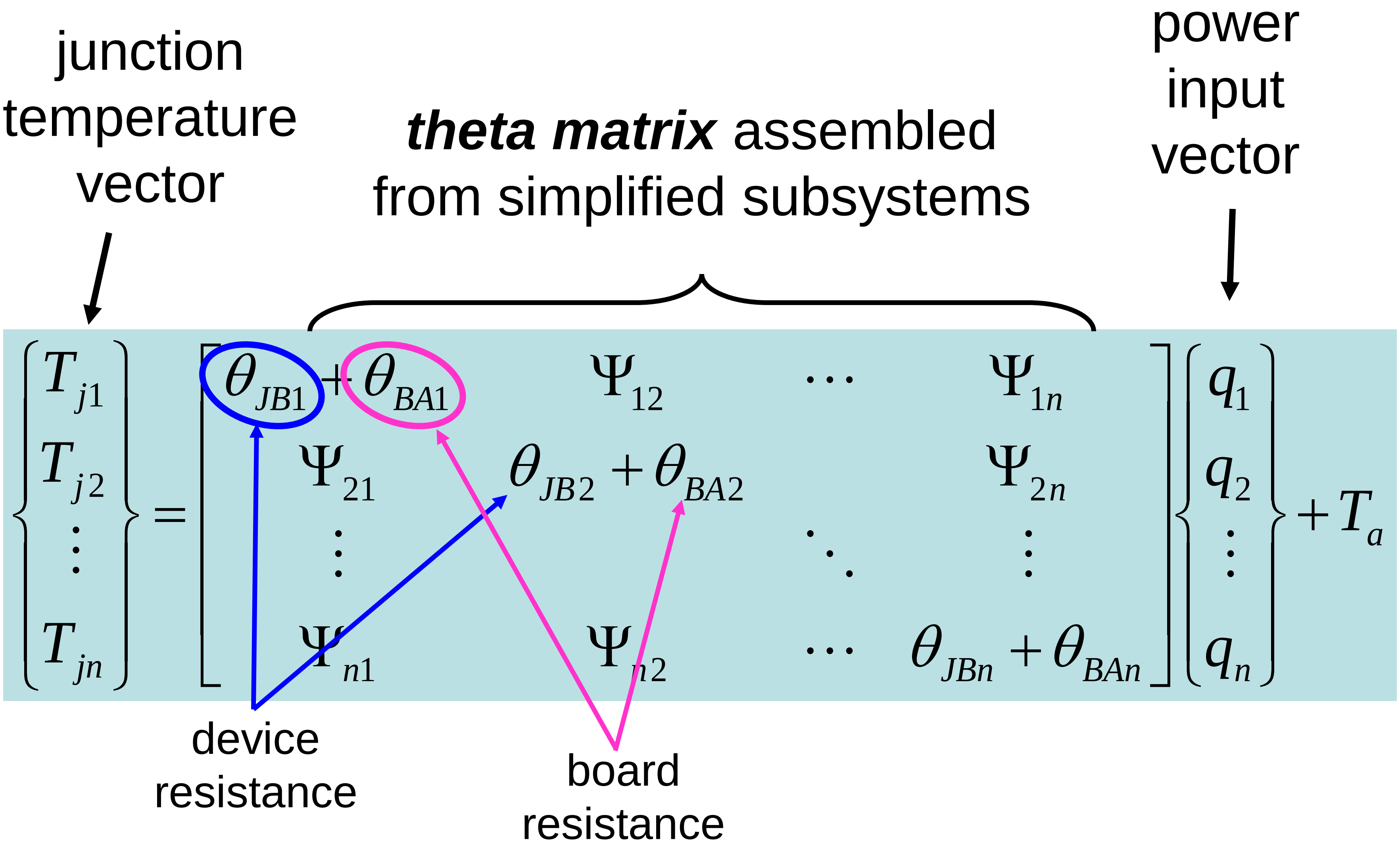


junction
temperature
vector

theta matrix assembled
from simplified subsystems

power
input
vector

$$\begin{Bmatrix} T_{j1} \\ T_{j2} \\ \vdots \\ T_{jn} \end{Bmatrix} = \overbrace{\begin{bmatrix} \theta_{J1A} & \Psi_{12} & \cdots & \Psi_{1n} \\ \Psi_{21} & \theta_{J2A} & & \Psi_{2n} \\ \vdots & & \ddots & \vdots \\ \Psi_{n1} & \Psi_{n2} & \cdots & \theta_{JnA} \end{bmatrix}} \begin{Bmatrix} q_1 \\ q_2 \\ \vdots \\ q_n \end{Bmatrix} + T_a$$



junction
temperature
vector

theta matrix assembled
from simplified subsystems

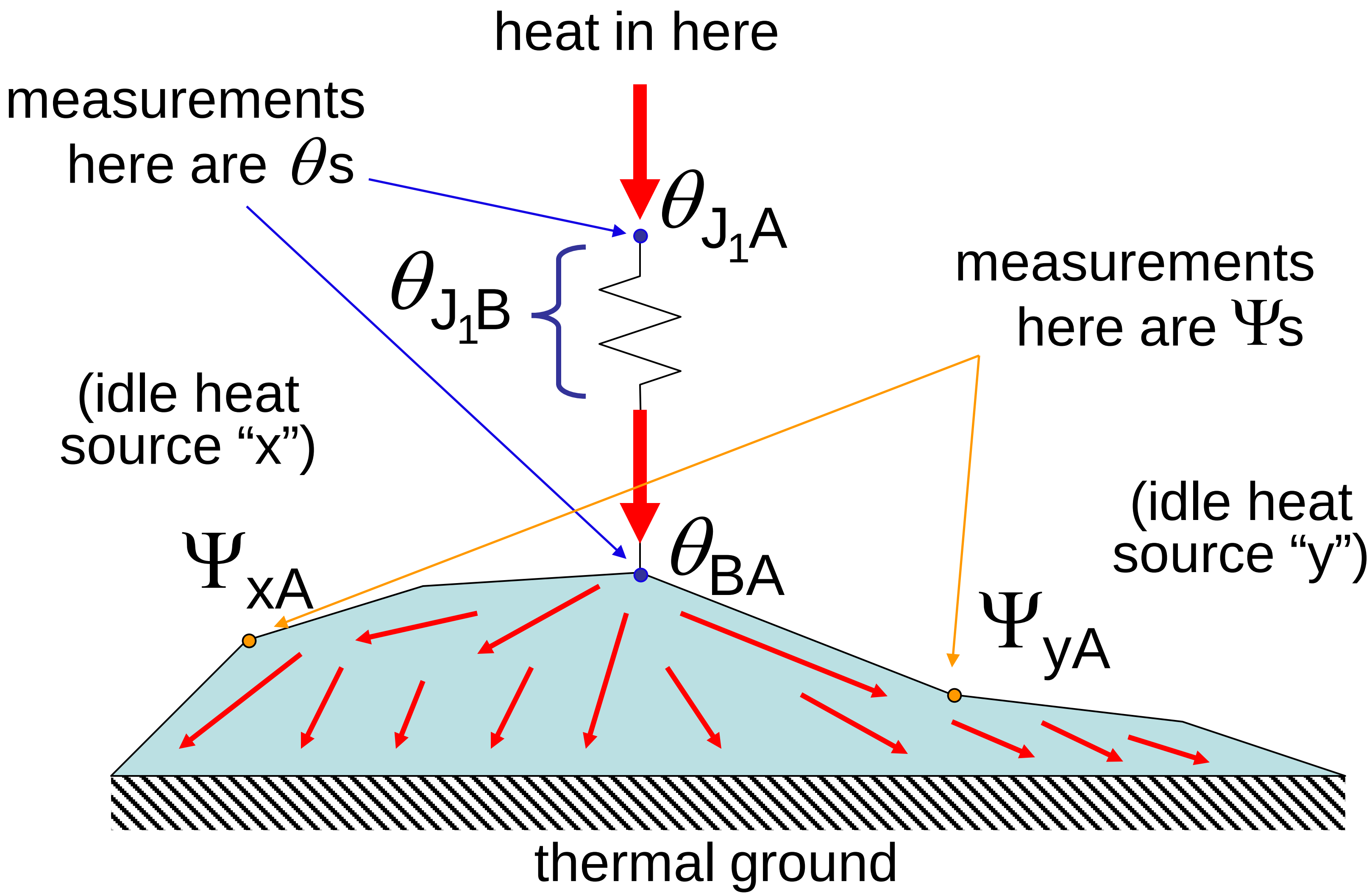
power
input
vector

$$\begin{Bmatrix} T_{j1}\\ T_{j2}\\ \vdots\\ T_{jn}\end{Bmatrix} = \begin{bmatrix} \theta_{JB1}+\theta_{BA1} & \Psi_{12} & \cdots & \Psi_{1n}\\ \Psi_{21} & \theta_{JB2}+\theta_{BA2} & & \Psi_{2n}\\ \vdots & & \ddots & \vdots\\ \Psi_{n1} & \Psi_{n2} & \cdots & \theta_{JBn}+\theta_{BAn}\end{bmatrix} \begin{Bmatrix} q_1\\ q_2\\ \vdots\\ q_n\end{Bmatrix} + T_a$$

device
resistance

board
resistance

visualizing theta and psi



theta matrix doesn't have to be square

junction temperature vector

one column for each heat source

power input vector

$$\begin{Bmatrix} \Delta T_{j1} \\ \Delta T_{j2} \\ \Delta T_{xA} \\ \Delta T_{L1A} \\ \Delta T_{BA} \end{Bmatrix} = \overbrace{\begin{pmatrix} \theta_{JA1} & \Psi_{12} & \Psi_{13} \\ \Psi_{12} & \theta_{JA2} & \Psi_{23} \\ \Psi_{x1} & \Psi_{x2} & \Psi_{x3} \\ \Psi_{L1\cdot 1} & \Psi_{L1\cdot 2} & \Psi_{L1\cdot 3} \\ \Psi_{B1} & \Psi_{B2} & \Psi_{B3} \end{pmatrix}} \begin{Bmatrix} q_1 \\ q_2 \\ q_3 \end{Bmatrix}$$

one row for each heat source

one row for each temperature location of interest

(why is this Ψ and not θ?)

The Reciprocity Theorem

"… the reciprocity theorem is not one with many obvious uses. Nevertheless, it is an elegant theorem and seems to be one that every educated man is expected to know."1[1]

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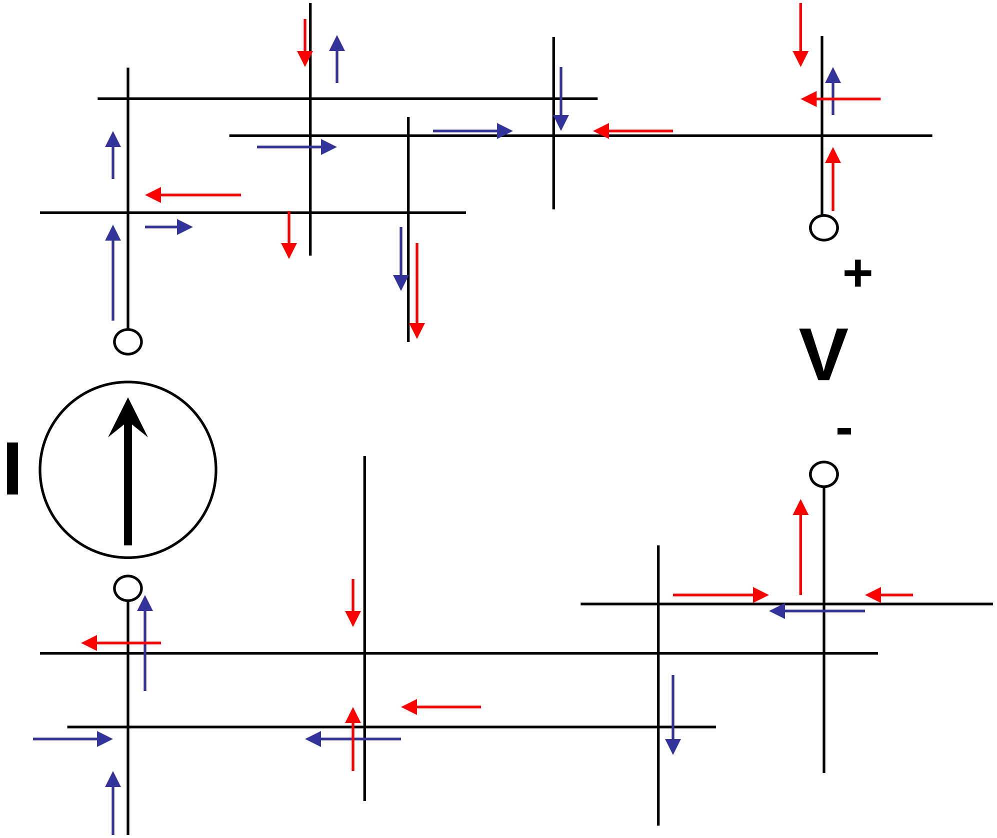
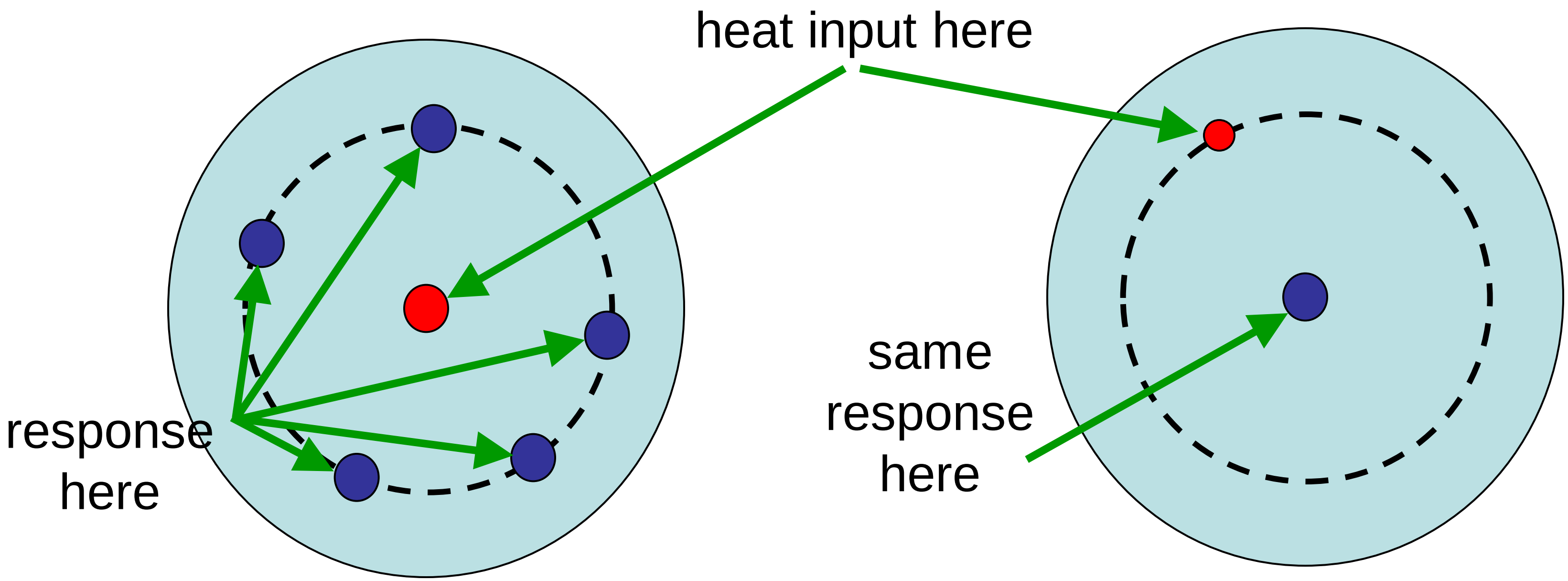
[1] H. Skilling, Electric Networks, pg. 249, John Wiley and Sons, 1974

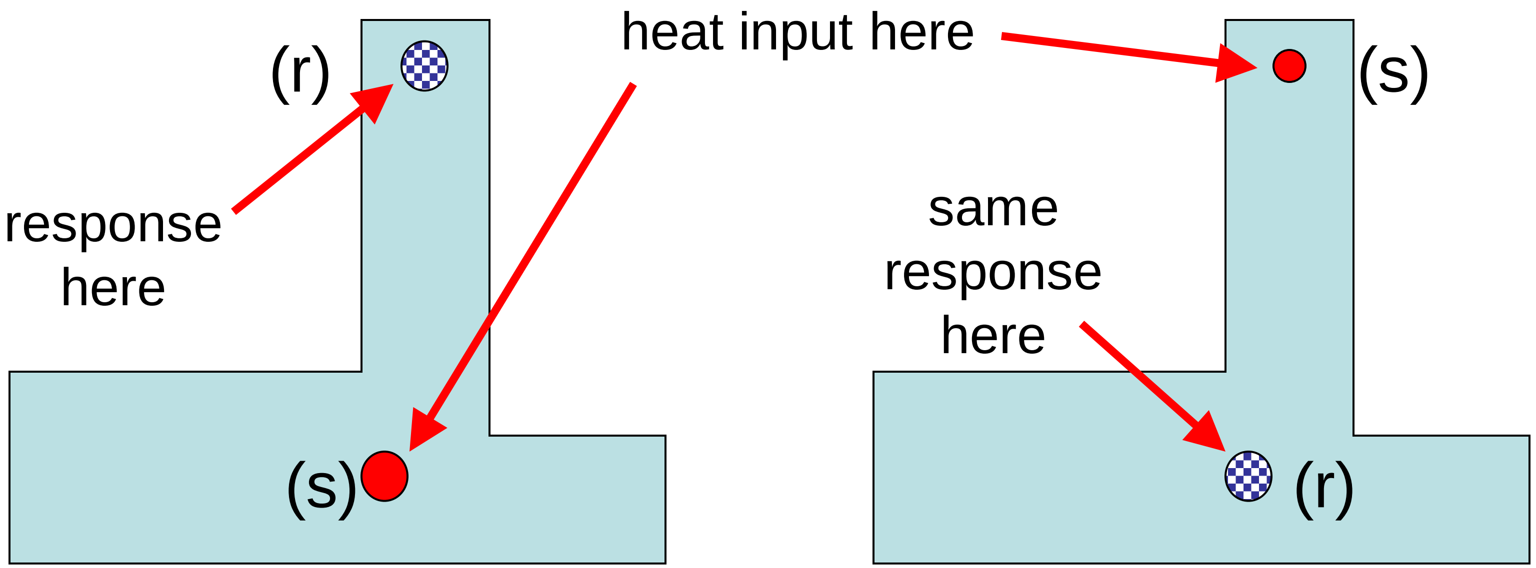
Electrical reciprocity



Thermal reciprocity

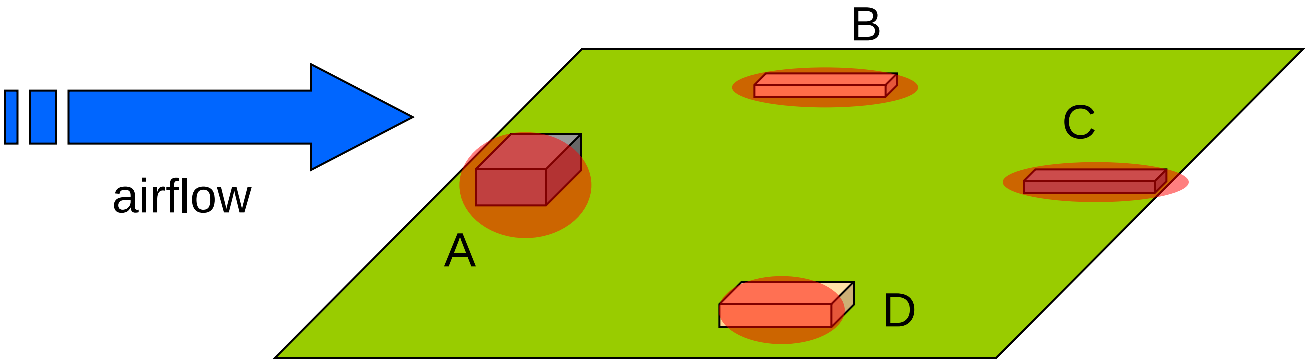


Another thermal reciprocity example



When does reciprocity *NOT* Apply?

- Upwind and downwind in forced-convection dominated applications



Heat in at “A” will raise temperature of “C” more than heat in at “C” will raise temperature of “A”

“B” and “D” may still be roughly reciprocal

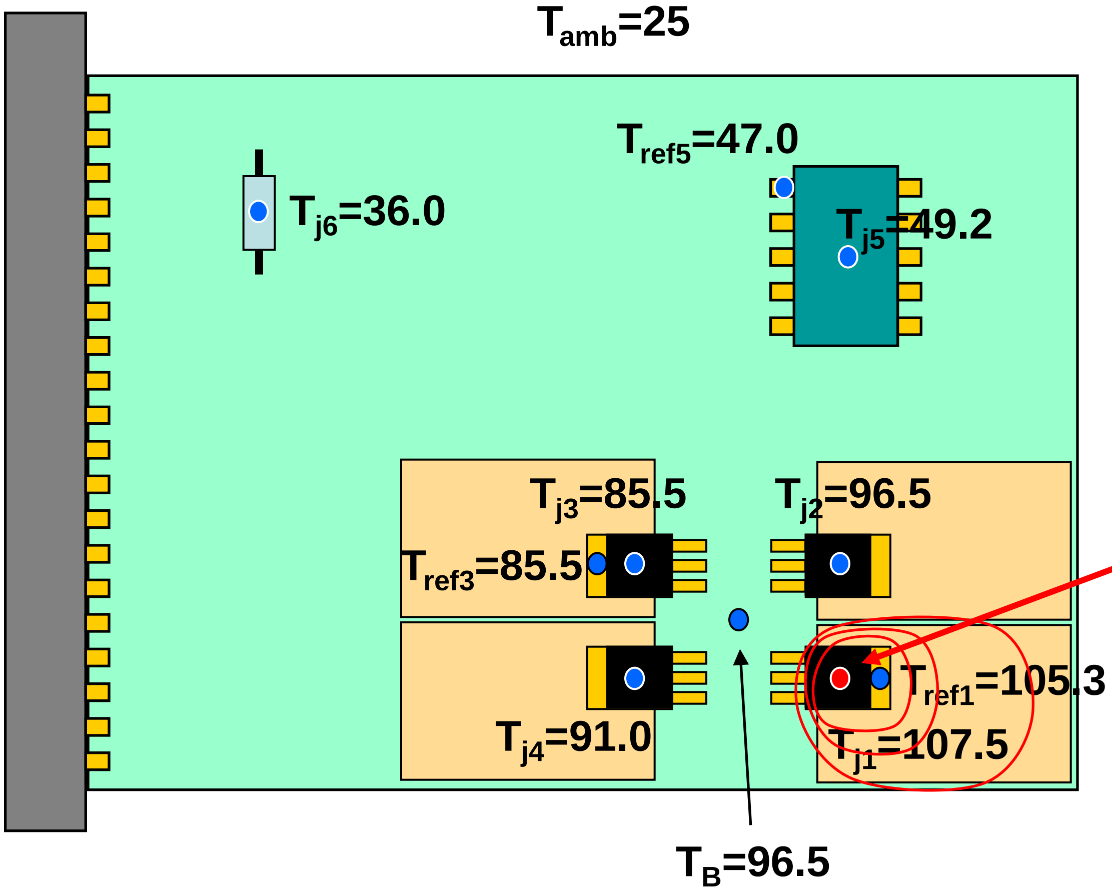
(square part of) matrix is symmetric

columns are the heat sources

rows are the response locations

J1	75	65	55	60	22	10
J2	65	71	60	55	25	11
J3	55	60	65	61	21	15
J4	60	55	61	73	18	11
J5	22	25	21	18	125	14
J6	10	11	15	11	14	180
R1	73	65	55	59	22	10
R3	55	60	63	61	21	15
R5	20	24	14	19	95	15
B	65	63	62	63	21	12

Superposition example



Device 1 heated, 1.1 W

Reduce the data

$$\theta_{j1A} = \frac{T_{j1} - T_{amb}}{q_1} = \frac{107.5 - 25}{1.1} = 75$$

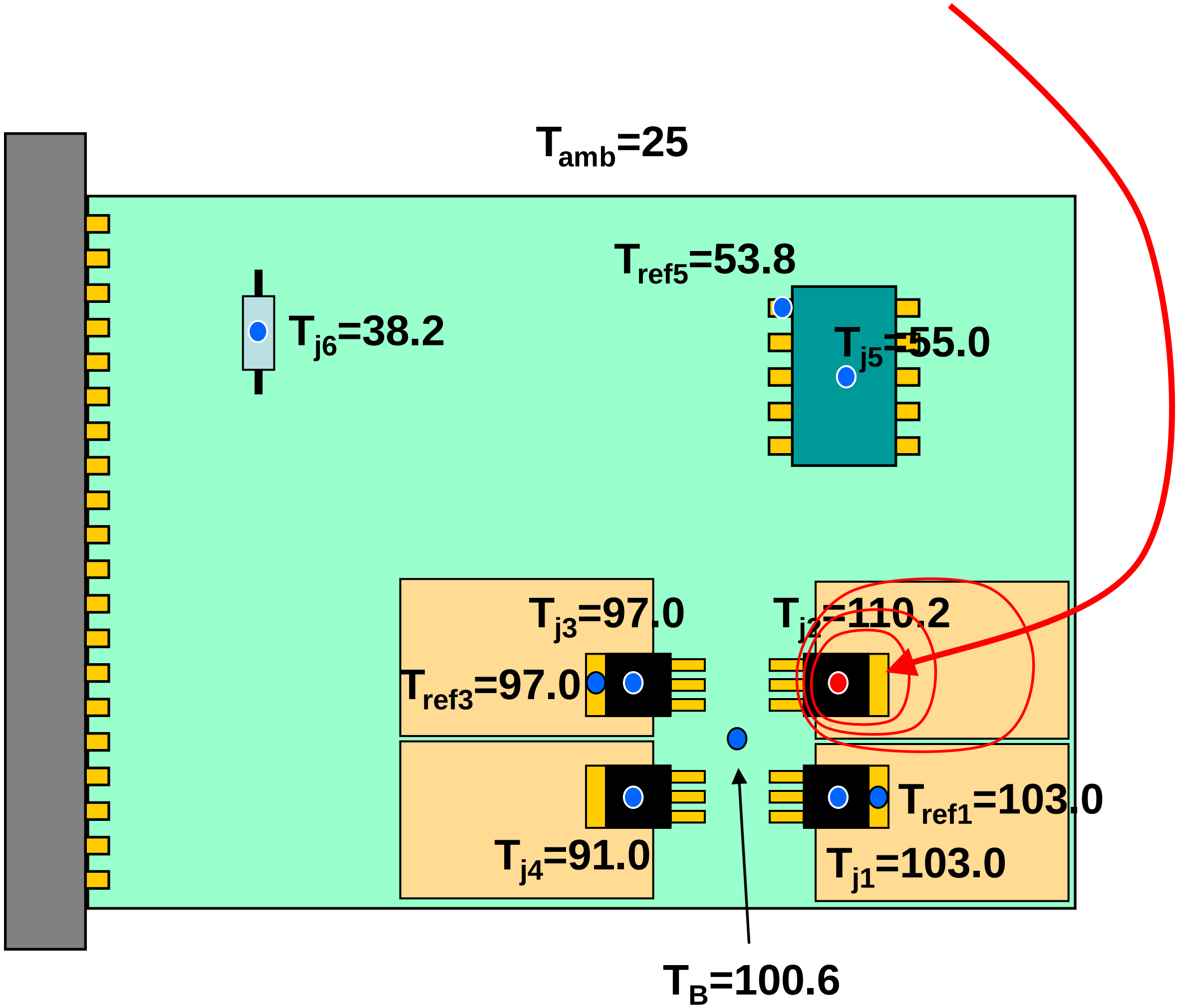
$$\Psi_{j2A} = \frac{T_{j2} - T_{amb}}{q_1} = \frac{96.5 - 25}{1.1} = 65$$

$$\vdots$$

$$\Psi_{BA} = \frac{T_{B} - T_{amb}}{q_1} = \frac{96.5 - 25}{1.1} = 65$$

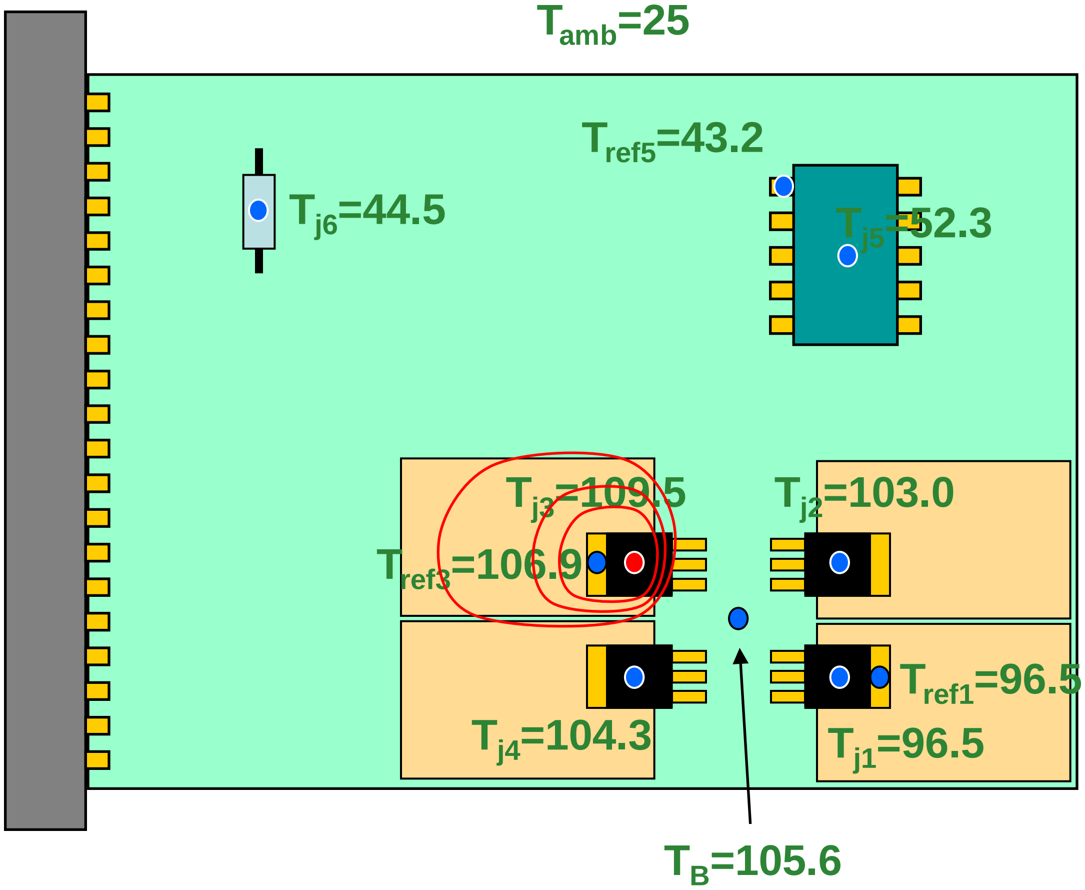
θ_{j1A}	75
Ψ_{j2A}	65
Ψ_{j3A}	55
Ψ_{j4A}	60
Ψ_{j5A}	22
Ψ_{j6A}	10
Ψ_{r1A}	73
Ψ_{r3A}	55
Ψ_{r5A}	20
Ψ_{BA}	65

Device 2 heated, 1.2 W



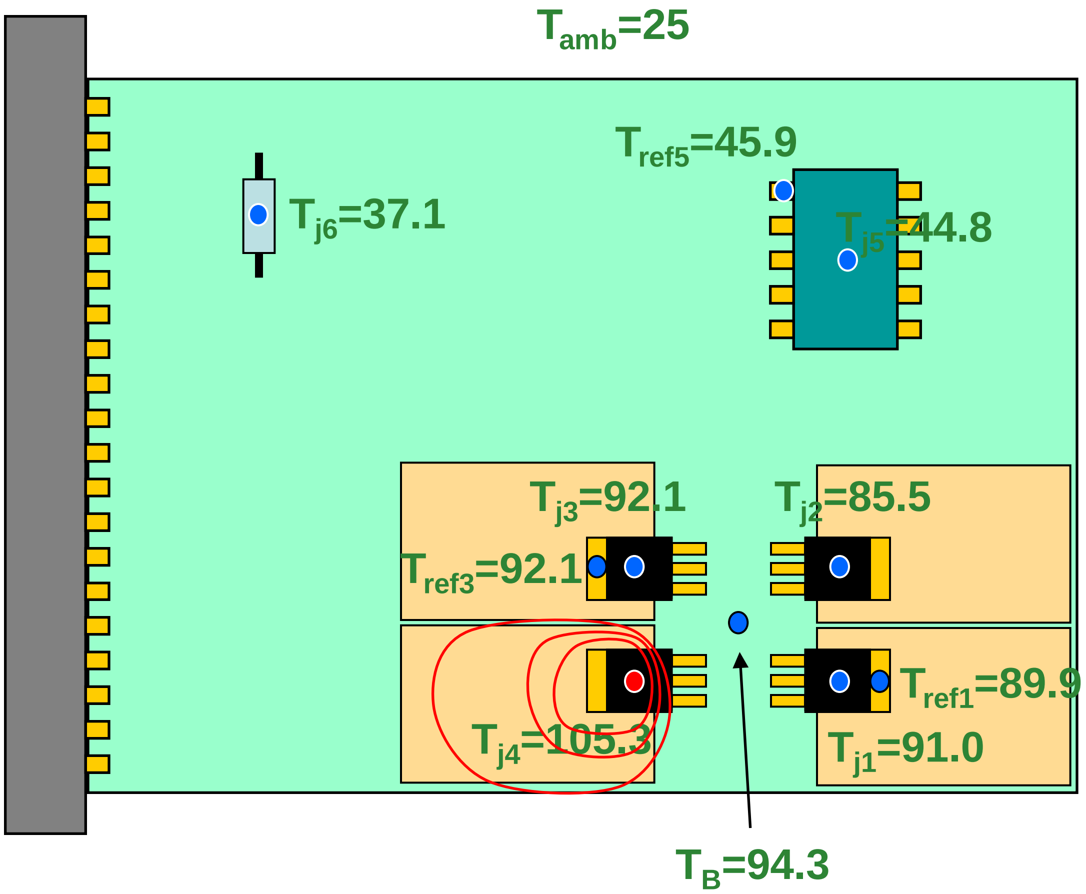
Ψ_{j1A}	65
θ_{j2A}	71
Ψ_{j3A}	60
Ψ_{j4A}	55
Ψ_{j5A}	25
Ψ_{j6A}	11
Ψ_{r1A}	65
Ψ_{r3A}	60
Ψ_{r5A}	24
Ψ_{BA}	63

Device 3 heated, 1.3 W



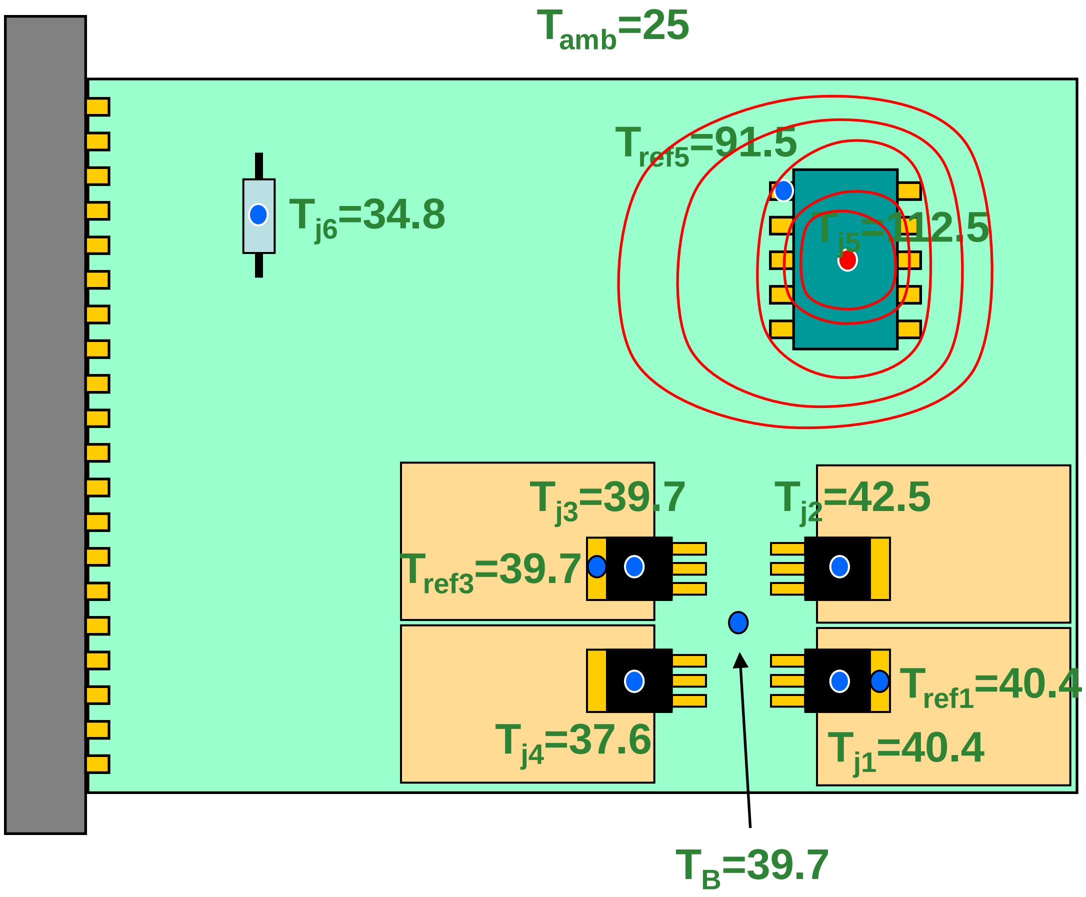
Ψ_{j1A}	55
Ψ_{j2A}	60
θ_{j3A}	65
Ψ_{j4A}	61
Ψ_{j5A}	21
Ψ_{j6A}	15
Ψ_{r1A}	55
Ψ_{r3A}	63
Ψ_{r5A}	14
Ψ_{BA}	62

Device 4 heated, 1.1 W



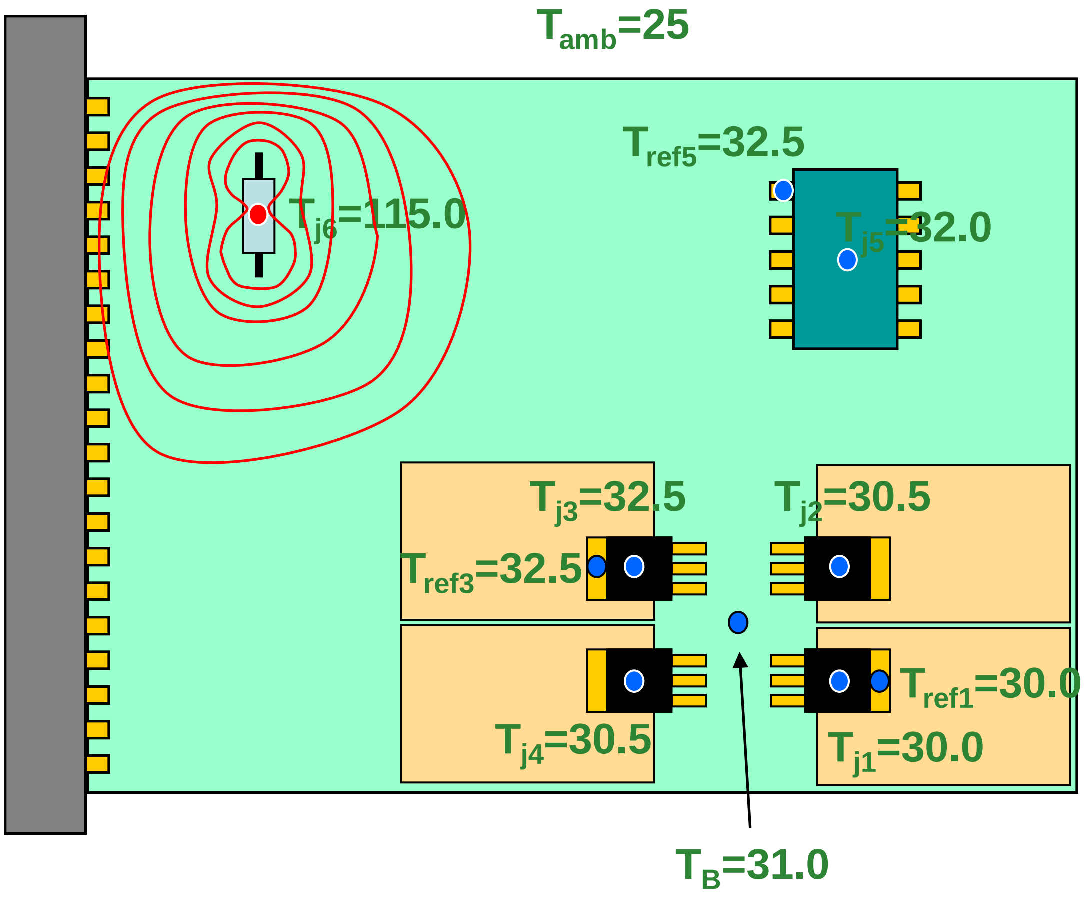
Ψ_{j1A}	60
Ψ_{j2A}	55
Ψ_{j3A}	61
θ_{j4A}	73
Ψ_{j5A}	18
Ψ_{j6A}	11
Ψ_{r1A}	59
Ψ_{r3A}	61
Ψ_{r5A}	19
Ψ_{BA}	63

Device 5 heated, 0.7 W



Ψ_{j1A}	22
Ψ_{j2A}	25
Ψ_{j3A}	21
Ψ_{j4A}	18
θ_{j5A}	125
Ψ_{j6A}	14
Ψ_{r1A}	22
Ψ_{r3A}	21
Ψ_{r5A}	95
Ψ_{BA}	21

Device 6 heated, 0.5 W



Ψ_{j1A}	10
Ψ_{j2A}	11
Ψ_{j3A}	15
Ψ_{j4A}	11
Ψ_{j5A}	14
θ_{j6A}	180
Ψ_{r1A}	10
Ψ_{r3A}	15
Ψ_{r5A}	15
Ψ_{BA}	12

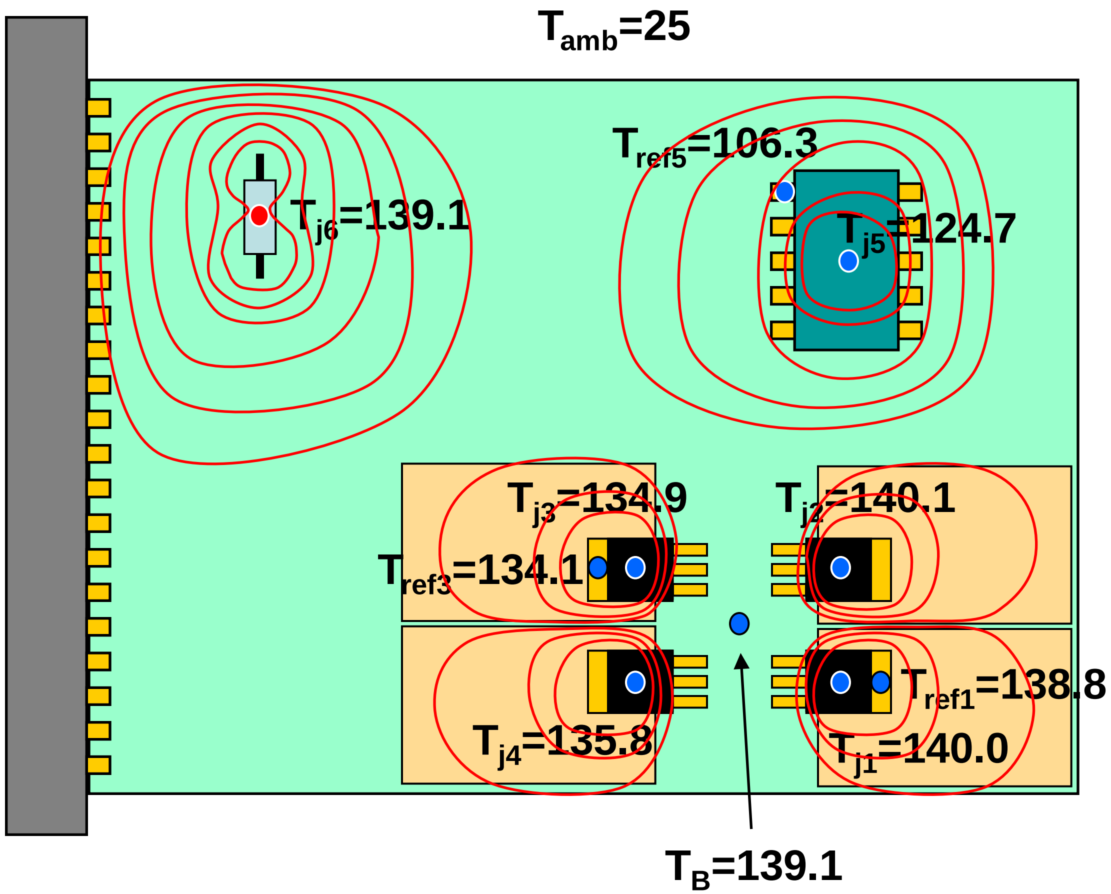
Collect the θ/Ψ values

columns are the heat sources

rows are the response locations

J1	75	65	55	60	22	10
J2	65	71	60	55	25	11
J3	55	60	65	61	21	15
J4	60	55	61	73	18	11
J5	22	25	21	18	125	14
J6	10	11	15	11	14	180
R1	73	65	55	59	22	10
R3	55	60	63	61	21	15
R5	20	24	14	19	95	15
B	65	63	62	63	21	12

Now apply actual power



Actual power in application

Q_{j1}	.4
Q_{j2}	.4
Q_{j3}	.4
Q_{j4}	.4
Q_{j5}	.5
Q_{j6}	.2

Compute some effective θ/Ψ values

Take T_{j1}, for instance. Remember when it was heated all alone, we calculated its self-heating theta-JA like this:

$$\theta_{\text{j1A}} = \frac{T_{j1} - T_{amb}}{q_1} = \frac{107.5 - 25}{1.1} = 75$$

$\neq$

Now let's see:

$$\theta_{\text{j1A}} = \frac{T_{j1} - T_{amb}}{q_1} = \frac{140 - 25}{0.4} = 288$$

And that’s not just a single aberration!

Self heating			
θ_{j1A}	288	←**3.8x**	75
θ_{j2A}	288	←**4.1x**	71
θ_{j3A}	274	←**4.2x**	65
θ_{j4A}	277	←**3.8x**	73
θ_{j5A}	199	←**1.6x**	125
θ_{j6A}	309	←**1.7x**	180

Junction to Reference			
$\Psi_{j1\text{-}R1}$	3.0	←**1.5x**	2.0
$\Psi_{j3\text{-}R3}$	2.0	←**1.0x**	2.0
$\Psi_{j5\text{-}R5}$	36.8	←**1.2x**	30.0

Junction to Board			
$\Psi_{j1\text{-}B}$	2.2	←**0.2x**	10.0
$\Psi_{j2\text{-}B}$	2.5	←**0.3x**	8.0
$\Psi_{j3\text{-}B}$	-10.5	←**-3.5x**	3.0
$\Psi_{j4\text{-}B}$	-8.3	←**-0.8x**	10.0

Is the moral clear?

- You simply *cannot* use published theta-JA values for devices in your real system, even if those values are perfectly accurate and correct as reported on the datasheet and you know the exact specifications of the test conditions.
- Not unless your actual application is identical to the manufacturer’s test board – and uses just that one device *all by itself*.

So is it *really* this bad?

Only sort-of. Let’s revisit the math for one device …

$$\begin{Bmatrix} T_{j1}\\ T_{j2}\\ \vdots\\ T_{jn}\end{Bmatrix} = \begin{bmatrix} \theta_{J1A} & \Psi_{12} & \cdots & \Psi_{1n}\\ \Psi_{12} & \theta_{J2A} & & \Psi_{2n}\\ \vdots & & \ddots & \vdots\\ \Psi_{1n} & \Psi_{2n} & \cdots & \theta_{JnA}\end{bmatrix}\begin{Bmatrix} q_1\\ q_2\\ \vdots\\ q_n\end{Bmatrix} + T_a$$

$$T_{j1} = \theta_{J1A} q_1 + \underbrace{\Psi_{12} q_2 + \ldots \Psi_{1n} q_n}\, + T_a$$

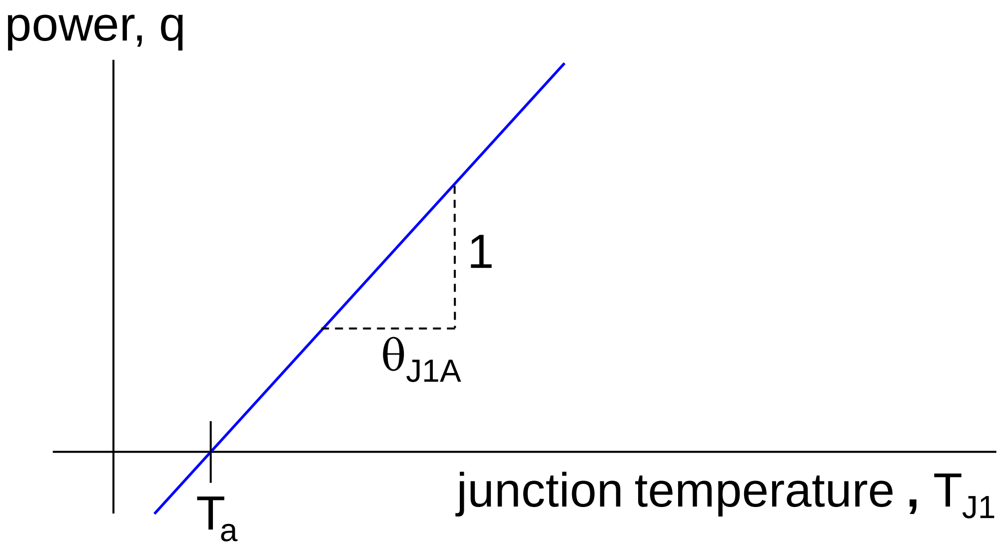
$$T_{j1} = \theta_{J1A} q_1 + \boxed{\sum_{2}^{n} \Psi_{1n} q_n + T_a}$$

“effective”
ambient

A graphical view

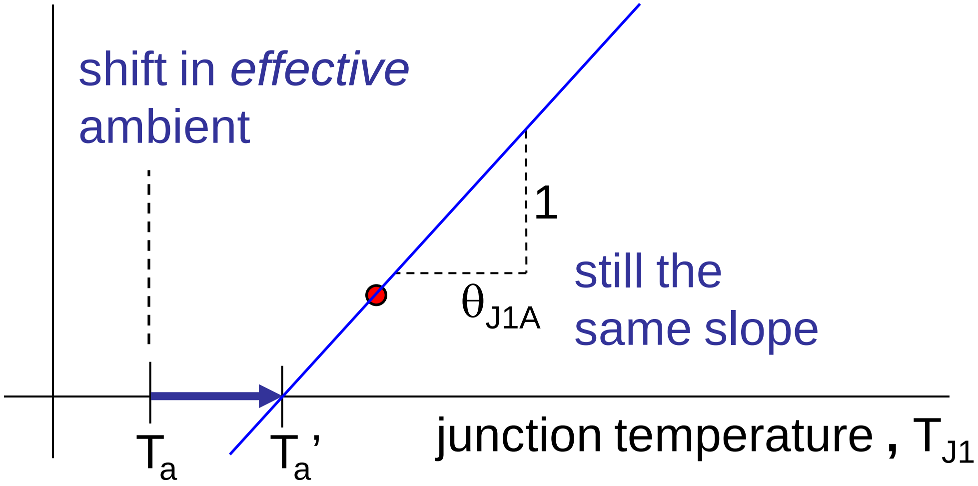
Isolated device

$$T_{j1} = \theta_{J1A} q_1 + T_a$$



Device in a system

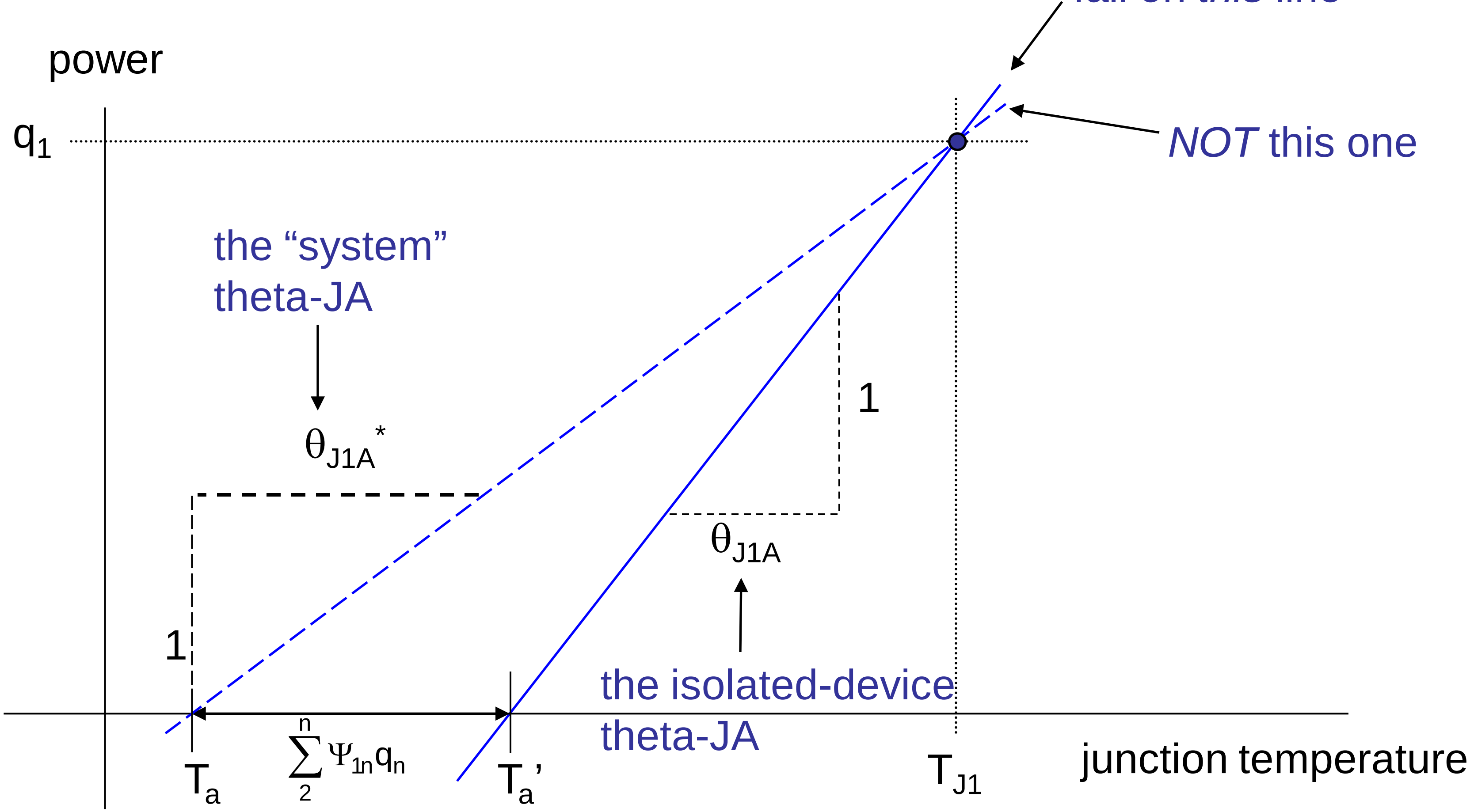
$$\begin{aligned} T_{j1} &= \theta_{J1A} q_1 + \underbrace{\sum_{2}^{n} \Psi_{1n} q_n + T_a} \\ &= \theta_{J1A} q_1 + \qquad T_a' \end{aligned}$$



shift in *effective* ambient

still the same slope

What about that “system” theta we saw earlier that was so different?



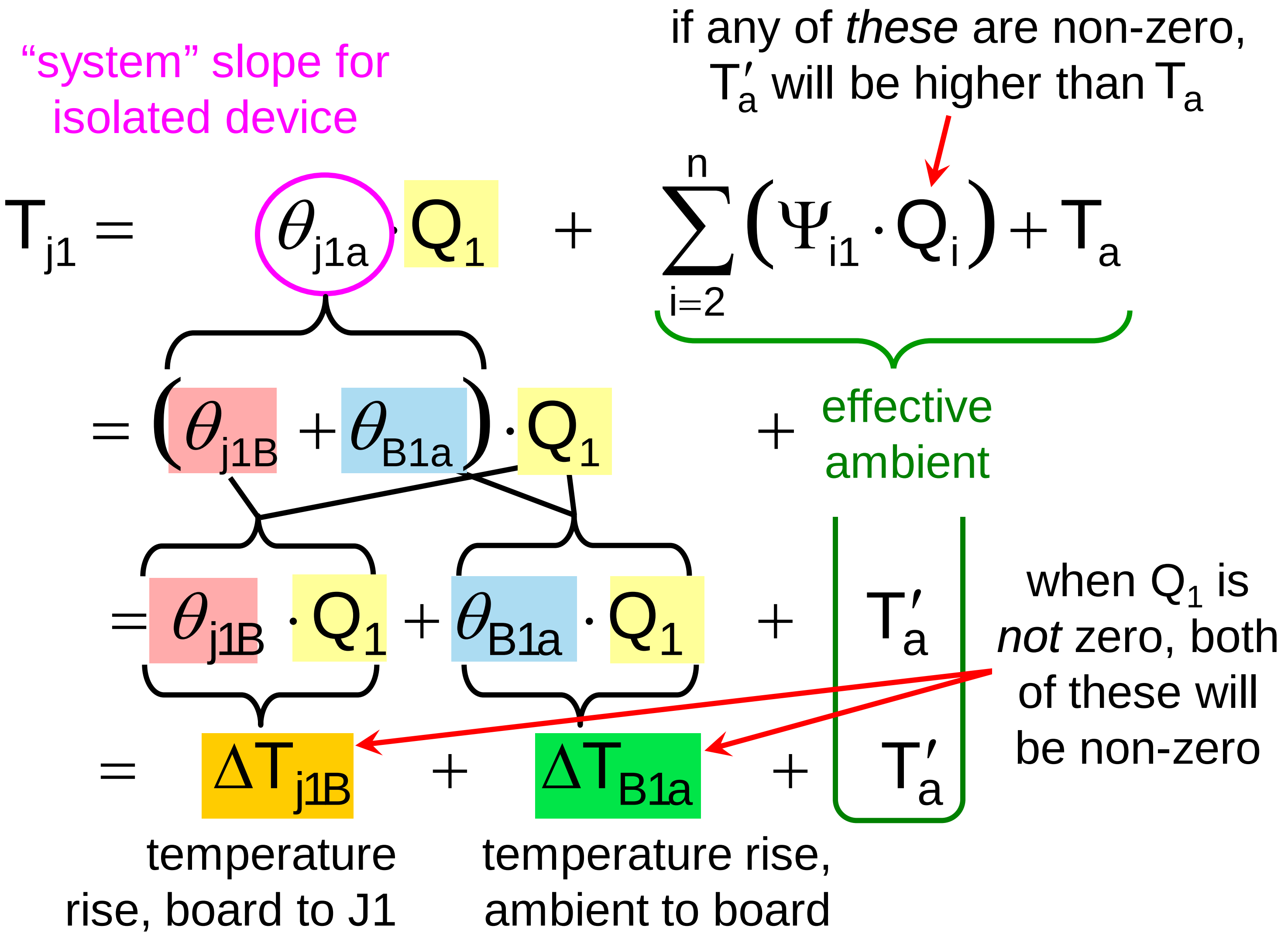
device #1 power/temperature perturbations will fall on *this* line

NOT this one

the “system” theta-JA

the isolated-device theta-JA

How does *effective ambient* relate to board temperature?



“system” slope for isolated device

if any of *these* are non-zero, T'_a will be higher than T_a

$$T_{j1} = \theta_{j1a} \cdot Q_1 + \underbrace{\sum_{i=2}^{n} \left(\Psi_{i1} \cdot Q_i \right) + T_a}_{\text{effective ambient}}$$

$$= \left(\theta_{j1B} + \theta_{B1a} \right) \cdot Q_1 + \text{effective ambient}$$

$$= \theta_{j1B} \cdot Q_1 + \theta_{B1a} \cdot Q_1 + T'_a$$

$$= \Delta T_{j1B} + \Delta T_{B1a} + T'_a$$

when Q_1 is *not* zero, both of these will be non-zero

temperature rise, board to J1

temperature rise, ambient to board

Controlling the matrix

How to harness this math in Excel®

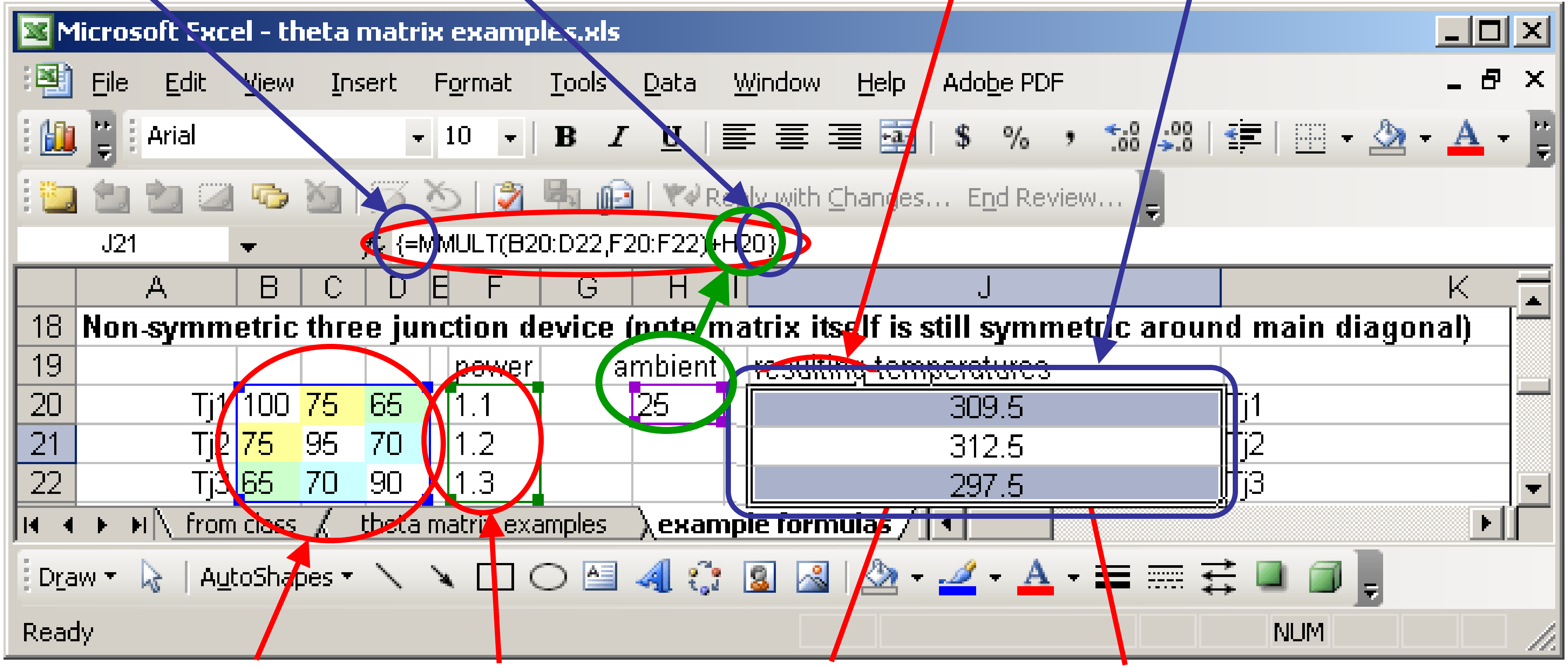
3x3 theta matrix, 3x1 power vector Excel® math

{=array formula notation}

obtained by using *Ctrl-Shift-Enter* rather than ordinary *Enter*

Matrix MULTiply

multi-cell placement of array formula



J21 {=MMULT(B20:D22,F20:F22)+H20}

	A	B	C	D	E	F	G	H	I	J	K
18	Non-symmetric three junction device (note matrix itself is still symmetric around main diagonal)										
19						power		ambient		resulting temperatures	
20	Tj1	100	75	65		1.1		25		309.5	Tj1
21	Tj2	75	95	70		1.2				312.5	Tj2
22	Tj3	65	70	90		1.3				297.5	Tj3

ambient

theta matrix

power vector

array reference to theta matrix

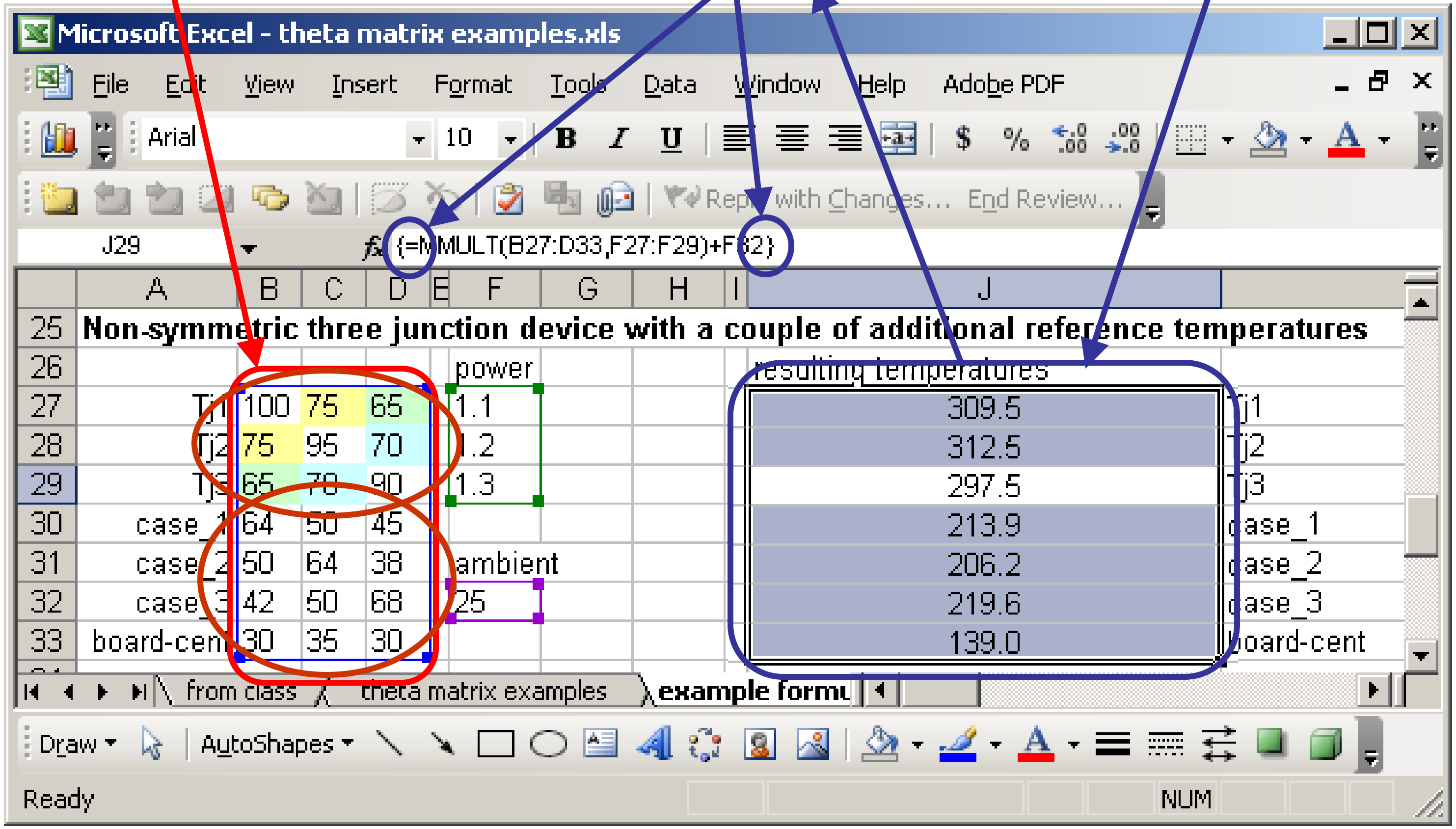
array reference to power vector

7x3 theta matrix, 3x1 power vector Excel® math

theta matrix is no longer square –
# of columns still must equal
# of rows of power vector

don't forget to use
Ctrl-Shift-Enter
to invoke array formula notation

array formula now
occupies 7 cells



Microsoft Excel - theta matrix examples.xls

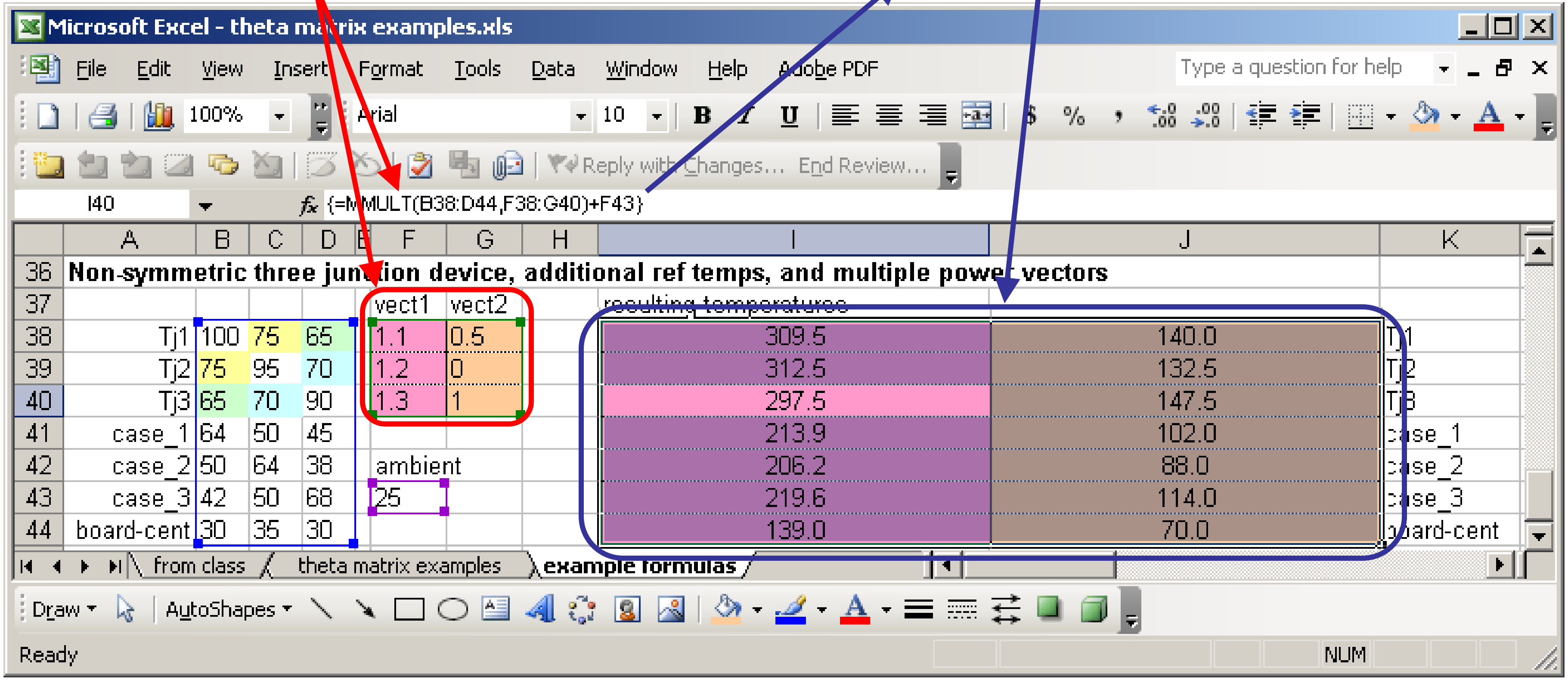
J29 {=MMULT(B27:D33,F27:F29)+F32}

	A	B	C	D	E	F	G	H	I	J	
25	Non-symmetric three junction device with a couple of additional reference temperatures										
26						power				resulting temperatures	
27	Tj1	100	75	65		1.1				309.5	Tj1
28	Tj2	75	95	70		1.2				312.5	Tj2
29	Tj3	65	70	90		1.3				297.5	Tj3
30	case_1	64	50	45						213.9	case_1
31	case_2	50	64	38		ambient				206.2	case_2
32	case_3	42	50	68		25				219.6	case_3
33	board-cen	30	35	30						139.0	board-cent

7x3 theta matrix, 3x2 power vector Excel® math

power “vector” is now a 3x*2* array – each column is a different power scenario, yet both are still processed using a single array (MMULT) formula

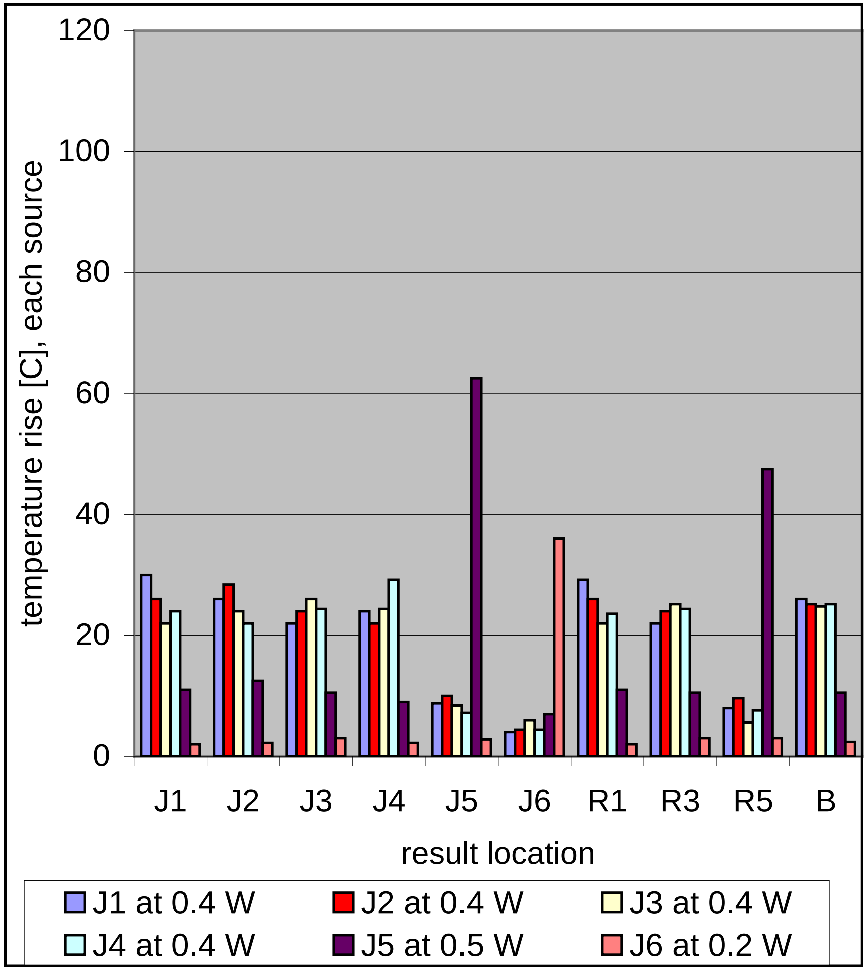
the single MMULT array formula now occupies 7 rows and *2* columns (one column for each independent power scenario result)

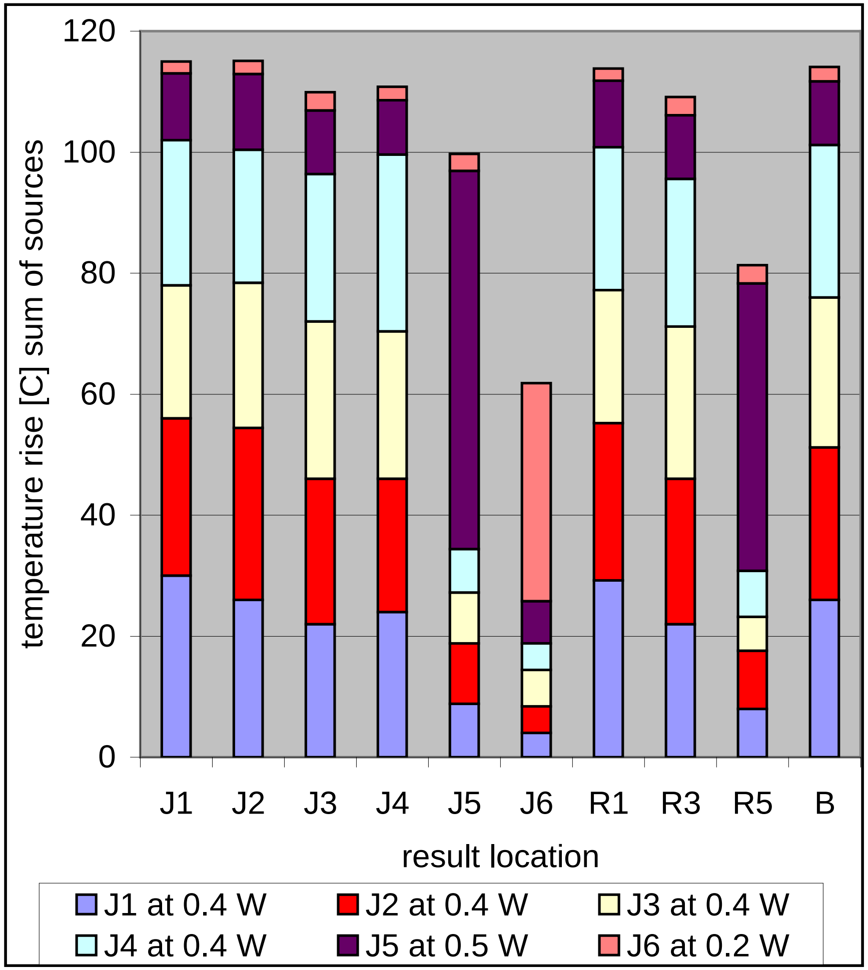


I40 {=MMULT(B38:D44,F38:G40)+F43}

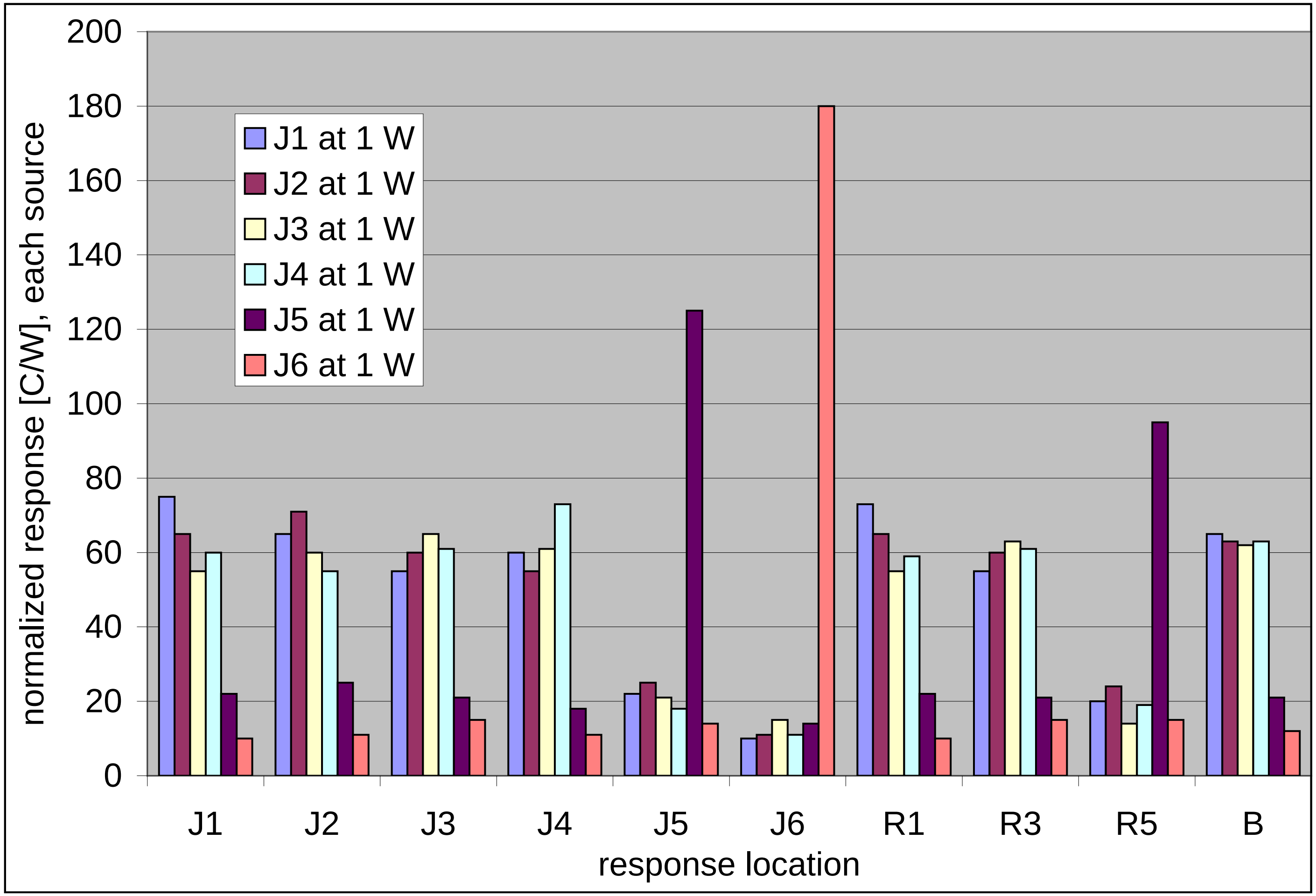
	A	B	C	D	E	F	G	H	I	J	K
36	**Non-symmetric three junction device, additional ref temps, and multiple power vectors**										
37						vect1	vect2		resulting temperatures		
38	Tj1	100	75	65		1.1	0.5		309.5	140.0	Tj1
39	Tj2	75	95	70		1.2	0		312.5	132.5	Tj2
40	Tj3	65	70	90		1.3	1		297.5	147.5	Tj3
41	case_1	64	50	45					213.9	102.0	ase_1
42	case_2	50	64	38		ambient			206.2	88.0	ase_2
43	case_3	42	50	68		25			219.6	114.0	ase_3
44	board-cent	30	35	30					139.0	70.0	oard-cent

Temperature direct contributions and totals





Normalized responses at each location due to each source



Some useful formulas

- conduction resistance…………………… $R = \dfrac{L}{k \cdot A}$
- convection resistance……………………. $R = \dfrac{1}{h \cdot A}$
- thermal capacitance…………………….. $C = \rho c_p V$
- characteristic time………………………
  - (dominated by 1-D conduction) $\tau = \dfrac{\rho c_p L^2}{k}$
- characteristic time……………………...
  - (dominated by 1-D convection) $\tau = \dfrac{\rho c_p L}{h}$
- short-time 1-D transient response……... $\Delta T = \dfrac{Q}{A} \dfrac{2}{\sqrt{\pi \rho c_p k}} \sqrt{t}$

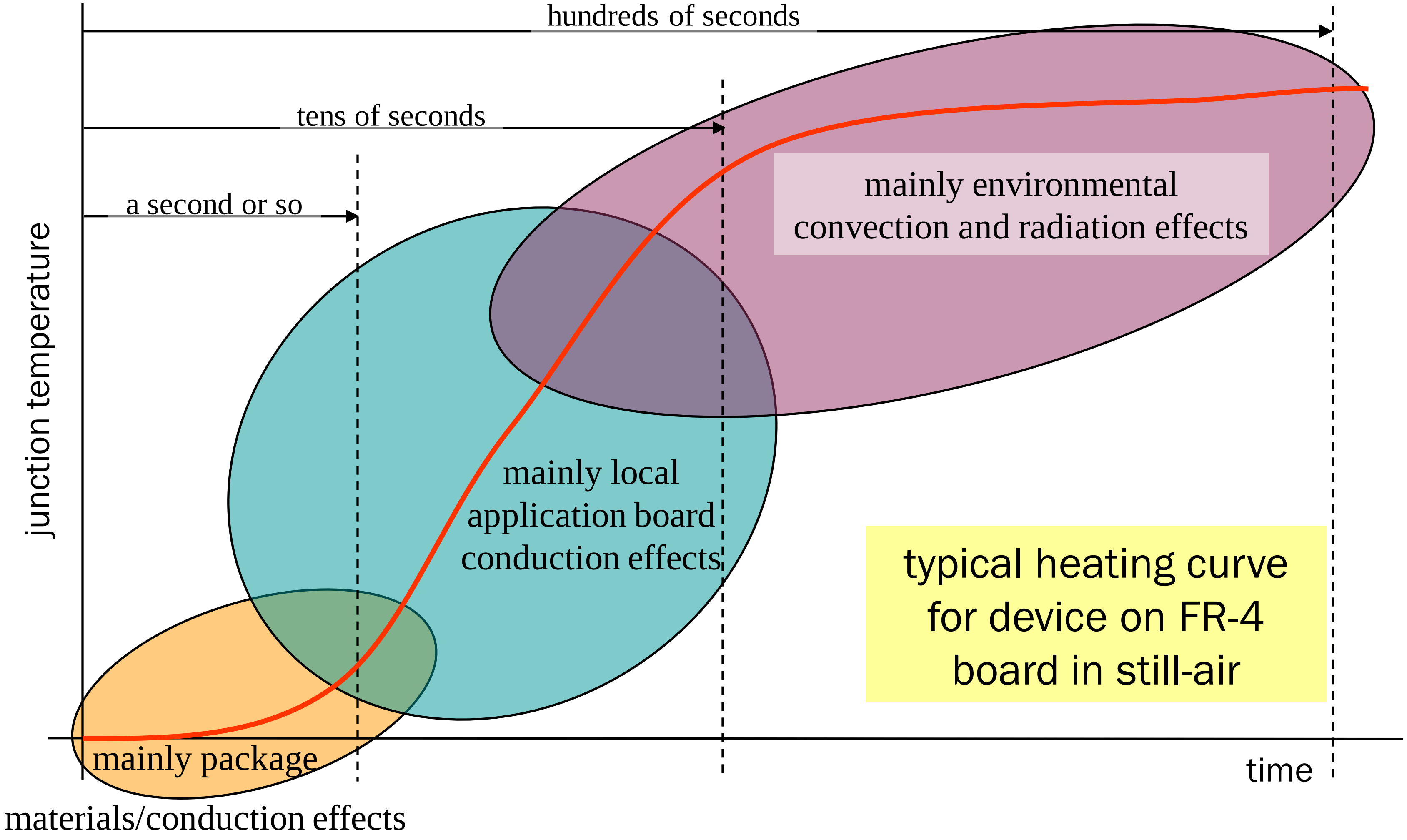
Terms used in preceding formulas

- L - thermal path length
- A - thermal path cross-sectional area
- k - thermal conductivity
- ρ - density
- c_p - heat capacity
- α - thermal diffusivity
- η - thermal effusivity
- h - convection heat-transfer “film coefficient”)
- ΔT - junction temperature rise
- Q - heating power
- t - time since heat was first applied

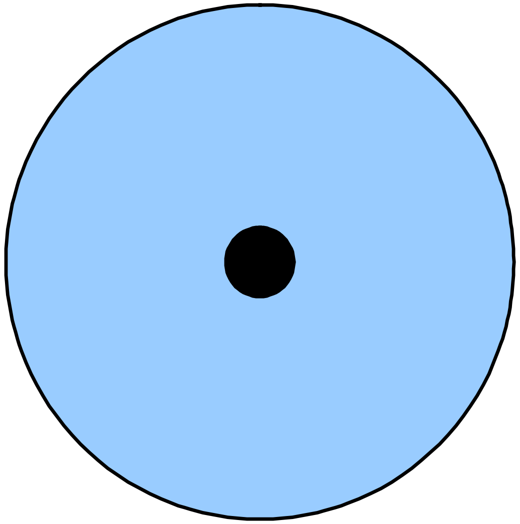
$$\alpha = \frac{k}{\rho c_p}$$

$$\eta = \sqrt{\rho c_p k}$$

When do these effects enter?

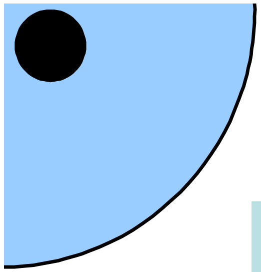


if



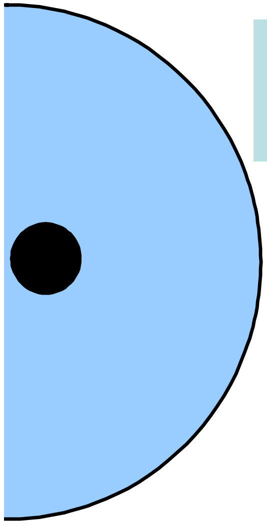
$\Rightarrow R$

then



$\approx 4R$

and



$\approx 2R$

Cylindrical and spherical conduction (through radial thickness) resistance formulas

Half-cylinder

$$R = \frac{\ln\left(\frac{r_o}{r_i}\right)}{\boxed{\pi} \cdot k \cdot L}$$

[included angle]

Full cylinder

$$R = \frac{\ln\left(\frac{r_o}{r_i}\right)}{\boxed{2\pi} \cdot k \cdot L}$$

$$R = \frac{\frac{1}{r_i} - \frac{1}{r_o}}{\boxed{2\pi} \cdot k}$$

Hemisphere

[solid angle]

$$R = \frac{\frac{1}{r_i} - \frac{1}{r_o}}{\boxed{4\pi} \cdot k}$$

Full sphere

where

- L – cylinder length
- r_i – inner radius
- r_o – outer radius

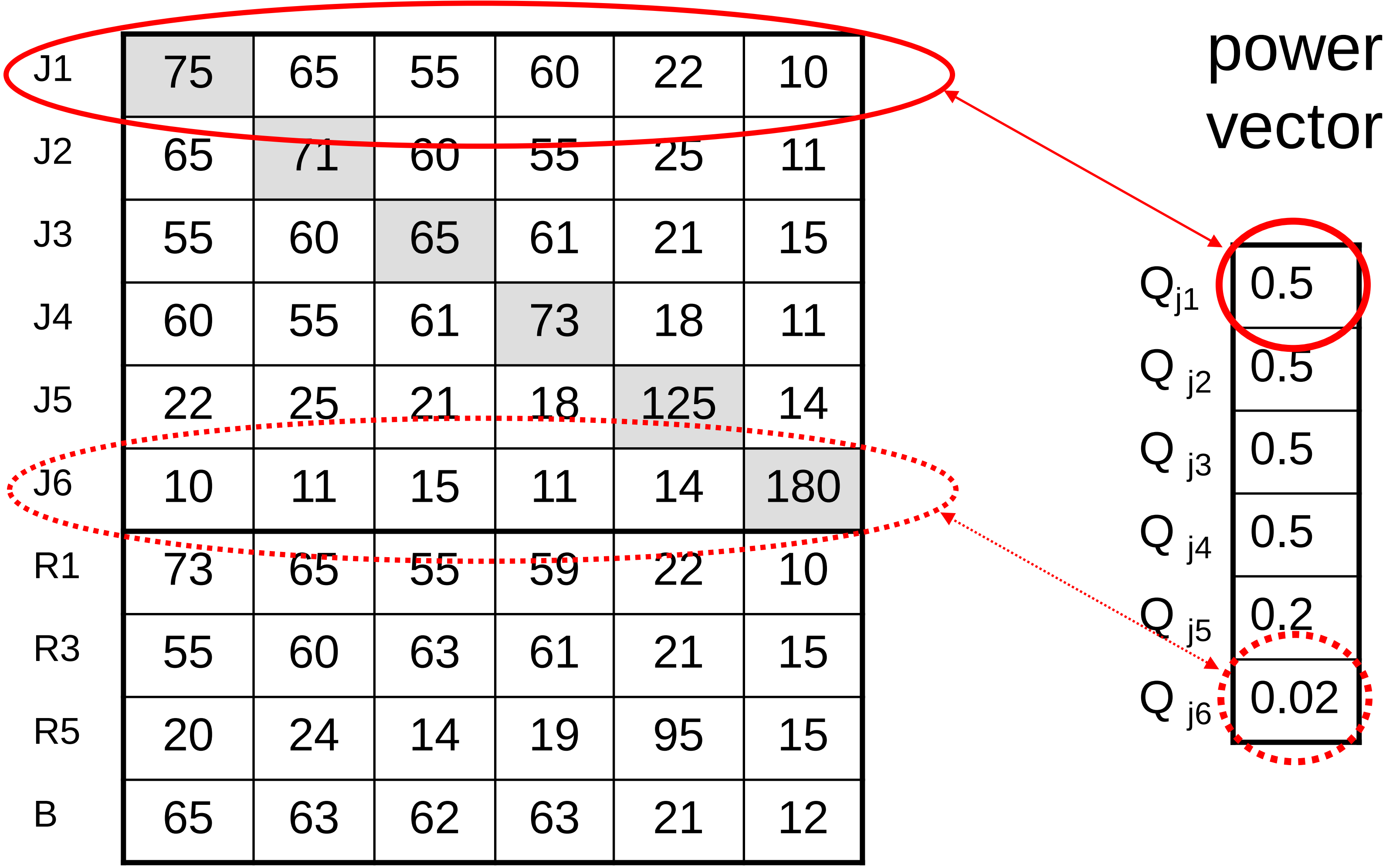
Predicting the temperature of high power components

- The device and system are equally important to get right

Predicting the temperature of low power components

- The system is probably more important than the device

Using the previous board example …



theta array

J1	75	65	55	60	22	10
J2	65	71	60	55	25	11
J3	55	60	65	61	21	15
J4	60	55	61	73	18	11
J5	22	25	21	18	125	14
J6	10	11	15	11	14	180
R1	73	65	55	59	22	10
R3	55	60	63	61	21	15
R5	20	24	14	19	95	15
B	65	63	62	63	21	12

power vector

Q_{j1}	0.5
Q_{j2}	0.5
Q_{j3}	0.5
Q_{j4}	0.5
Q_{j5}	0.2
Q_{j6}	0.02

Observe the relative contributions

For junction 1 (a high power component) we have:

the device itself …

the other devices …

$$= (75 \times 0.5) + (65 \times 0.5) + (55 \times 0.5) + (60 \times 0.5) + (22 \times 0.2) + (10 \times 0.02) + 25$$

$$= 37.5 + 32.5 + 27.5 + 30 + 4.4 + 0.2 + 25$$

$$= 37.5 + 94.6 + 25$$

Relative contributions to ΔT_{J6}

the other devices …

$$= (10 \times 0.5) + (11 \times 0.5) + (15 \times 0.5) + (11 \times 0.5) + (14 \times 0.2)$$

$$+ \quad (180 \times 0.02)$$

the device itself …

$$+ \quad 25$$

$$= \quad 5.0 + 5.5 + 7.5 + 5.5 + 2.8 \quad + \quad 3.6 \quad + \quad 25$$

$$= \quad 26.3 \quad + \quad 3.6 \quad + \quad 25$$

Thermal runaway

- Non-linear power vs. junction temperature device characteristic
- System thermal resistance isn’t low enough to shed small perturbations

A linear thermal cooling system

$$T_J = Q \cdot \theta_{Jx} + T_x$$

junction temperature as function of power, theta, and ground

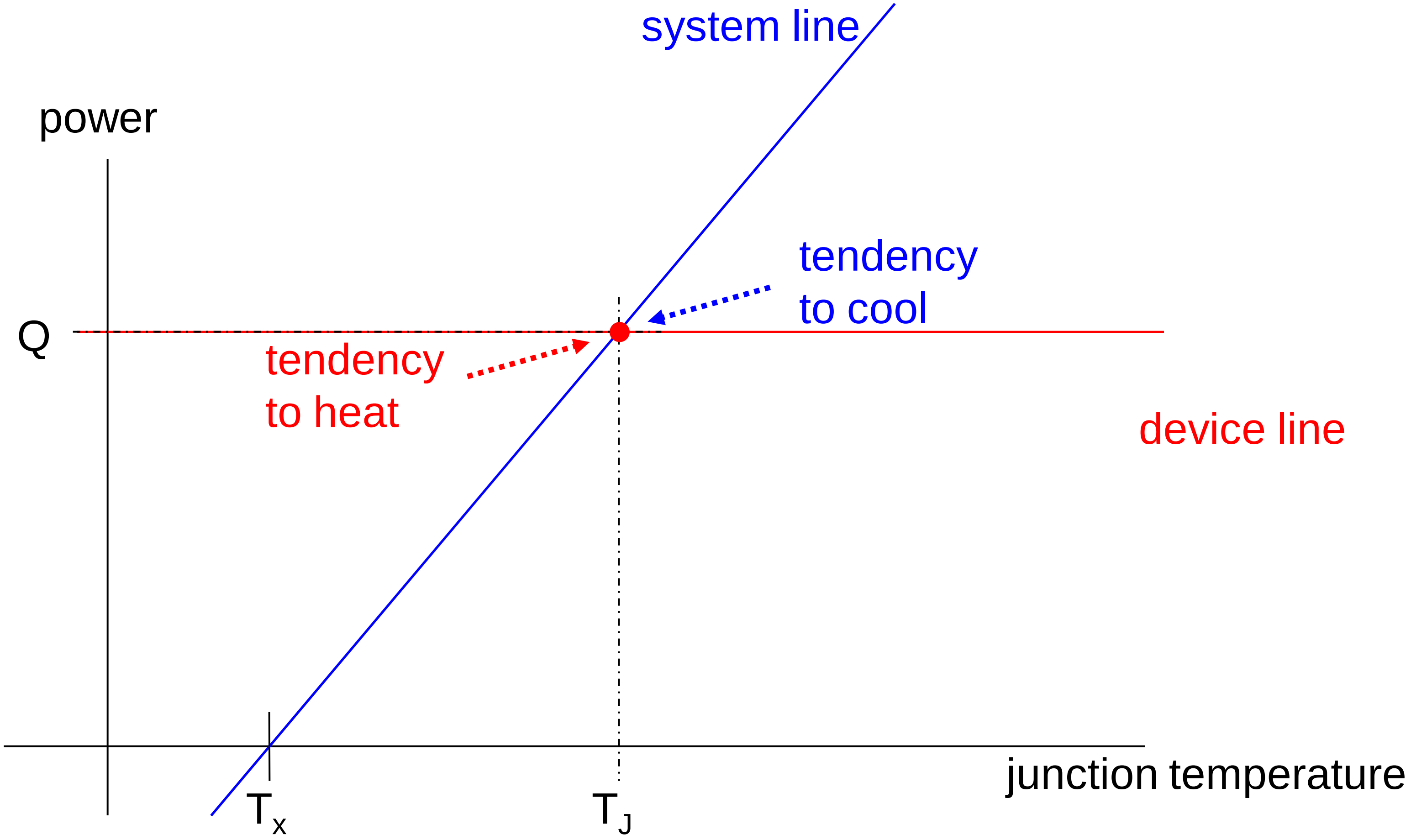
$$Q = \frac{T_J - T_x}{\theta_{Jx}}$$

… solving for power

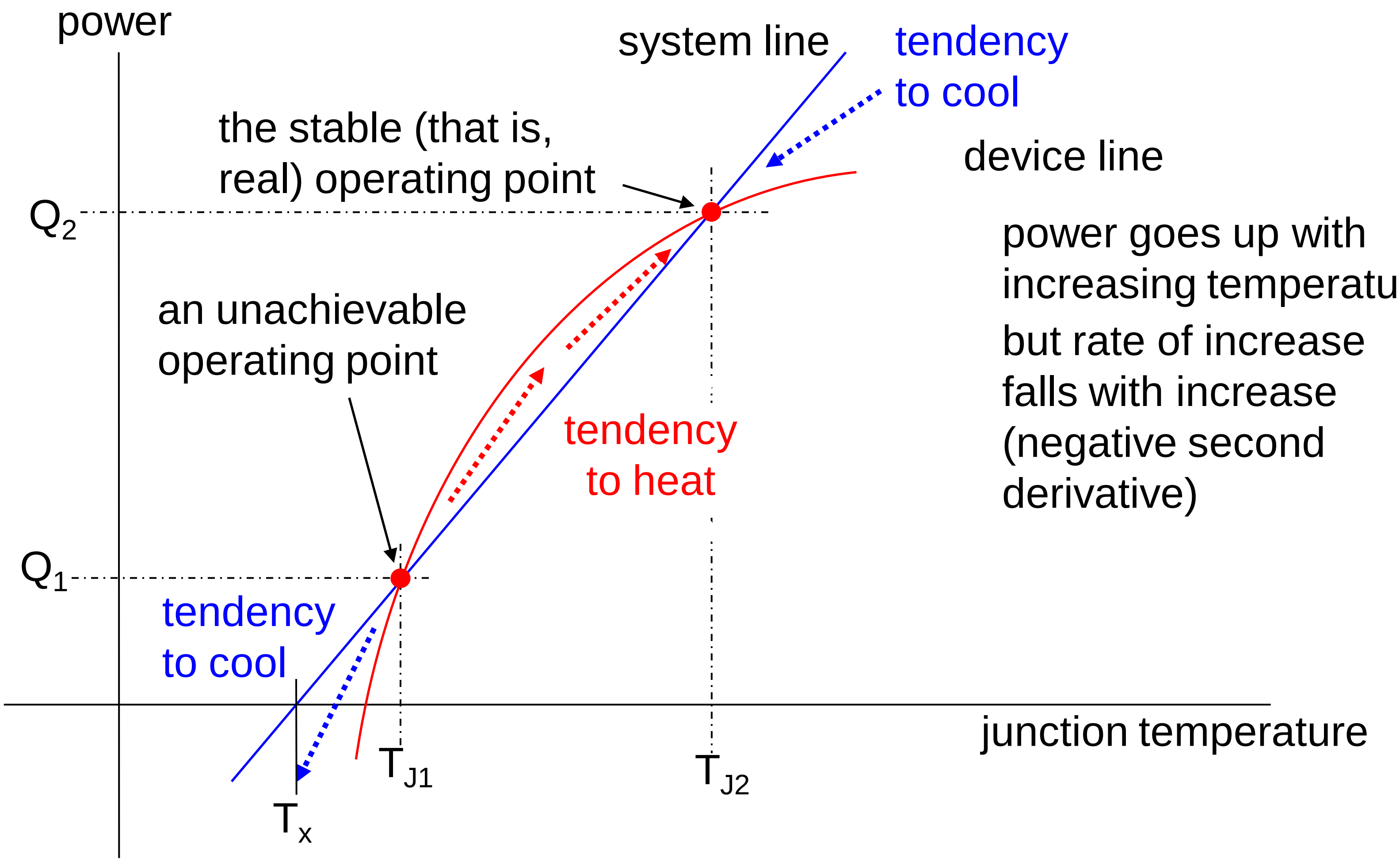
$$\frac{dQ}{dT} = \frac{1}{\theta_{Jx}}$$

sensitivity (slope) of power with respect to temperature

Effect of device line slope on system stability



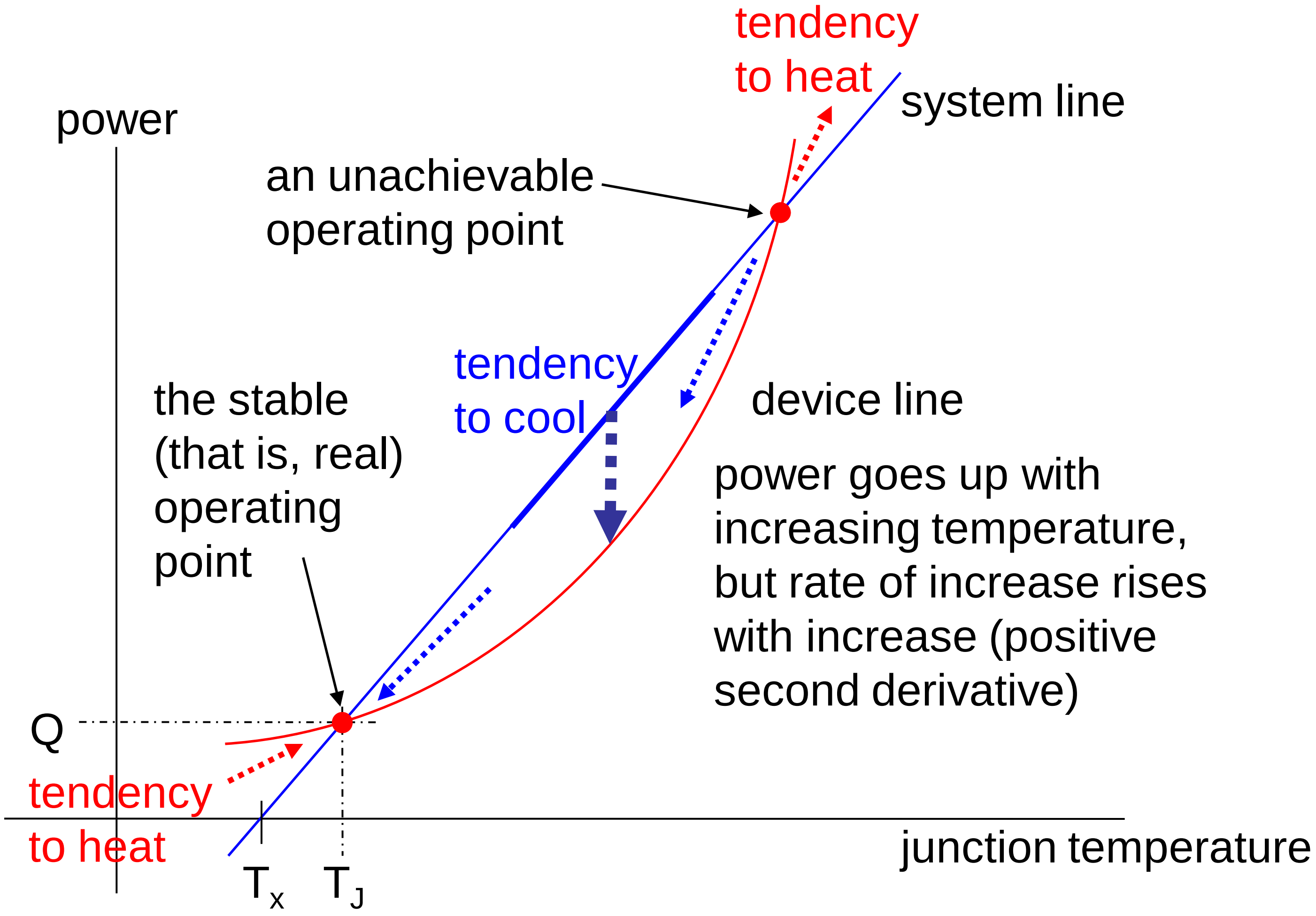
Operating points of thermal system when device line has negative second derivative



power goes up with increasing temperature

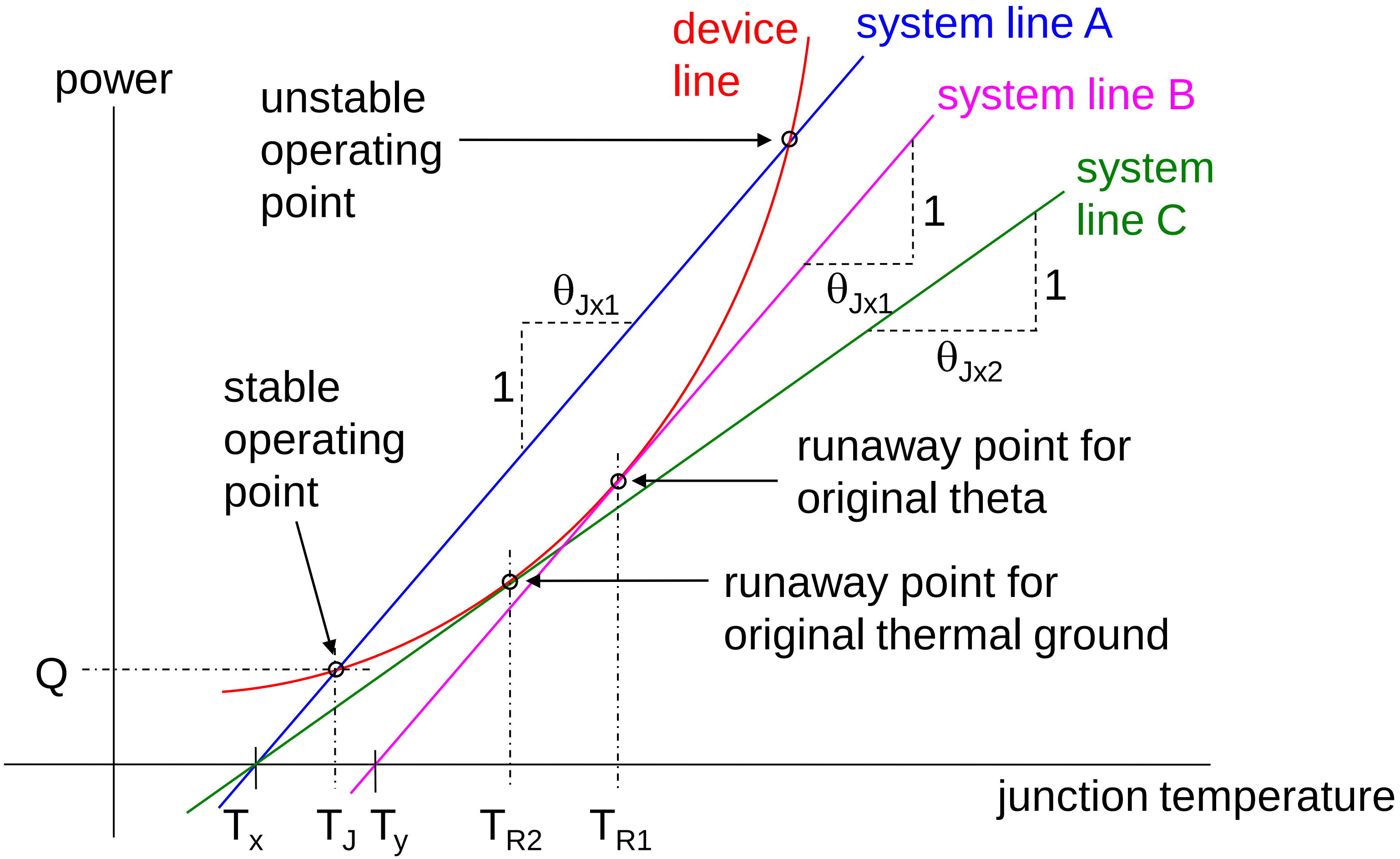
but rate of increase falls with increase (negative second derivative)

Operating points of thermal system when device line has *positive* second derivative

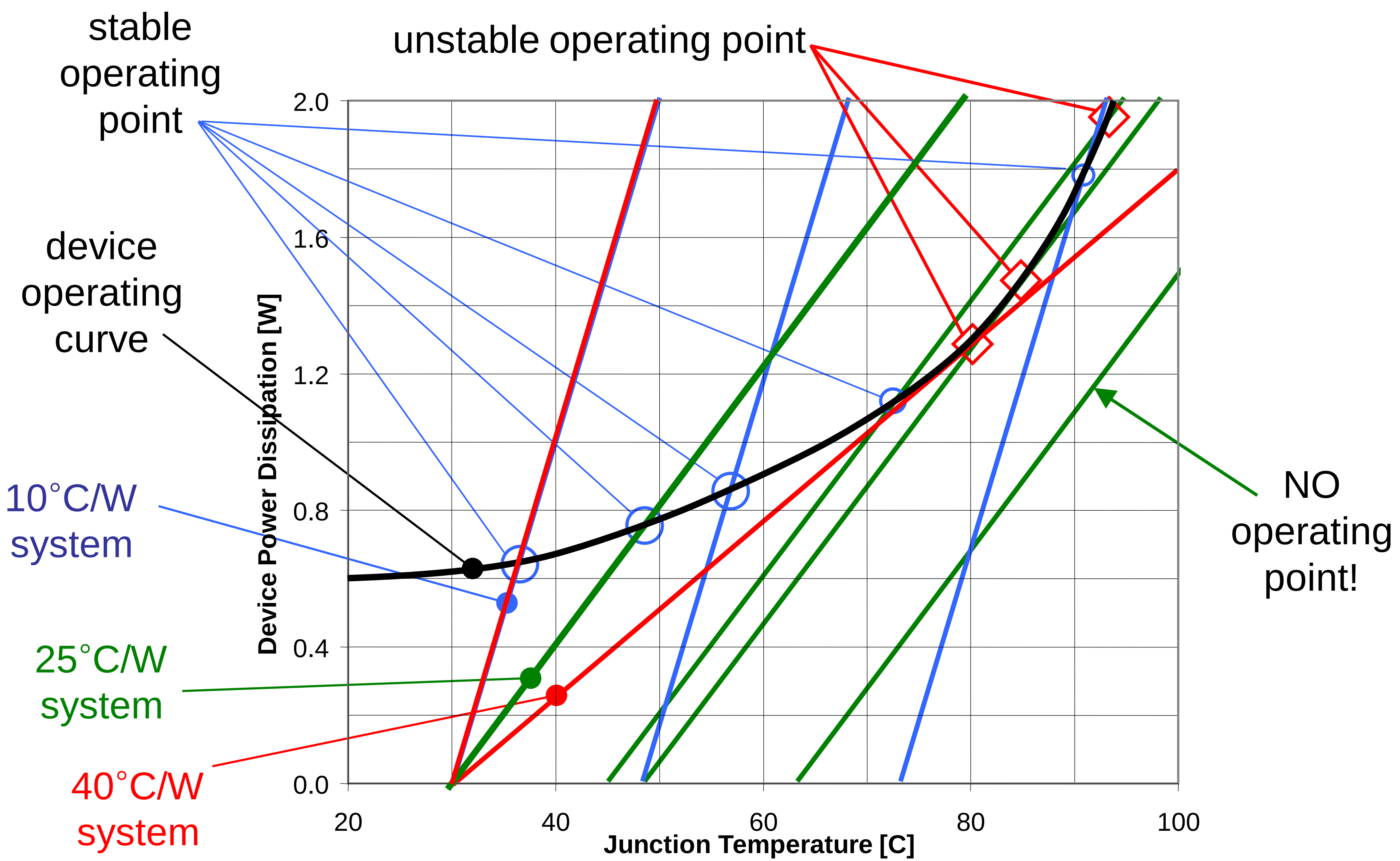


power goes up with increasing temperature, but rate of increase rises with increase (positive second derivative)

Generic power law device and generic linear cooling system



Let’s see how it works



Unfortunate coincidence of terms!

device <u>power</u>

$$Q = V \cdot I$$

a mathematical "power law"

$$y = a^{x}$$

an "exponential" power law (base is e)

$$y = e^{x}$$

Definition of power law device

rule of thumb for leakage;
2x increase for every 10°C

$$I = I_o 2^{\frac{T}{10}}$$

$$I = I_o e^{(\ln 2)\frac{T}{10}} = I_o e^{\frac{T}{\left(\frac{10}{\ln 2}\right)}}$$

$$I = I_o e^{\frac{T}{\lambda}}$$

defining: $\lambda = \dfrac{T_1 - T_2}{\ln\left({I_1}/{I_2} \right)}$

for constant voltage, power does the same

$$Q = V_R I_o e^{\frac{T}{\lambda}} = Q_o e^{\frac{T}{\lambda}}$$

1st and 2nd derivatives

$$\frac{dQ}{dT} = \frac{Q_o}{\lambda} e^{\frac{T}{\lambda}} \qquad \frac{d^2Q}{dT^2} = \frac{Q_o}{\lambda^2} e^{\frac{T}{\lambda}}$$

both always positive

The mathematical essence

System line

$$Q = \frac{T - T_x}{\theta_{Jx}}$$

Power law device line

$$Q = Q_o e^{\frac{T}{\lambda}}$$

Non-dimensionalizing

$$z = \frac{T - T_x}{\lambda}$$ **temperature**

$$q = \left(\frac{1}{Q_o} e^{\frac{-T_x}{\lambda}} \right) Q$$ **power**

Leads to:

(system)

$$q = kz$$

where:

$$k = \frac{\lambda}{\theta_{Jx} Q_o} e^{\frac{-T_x}{\lambda}}$$

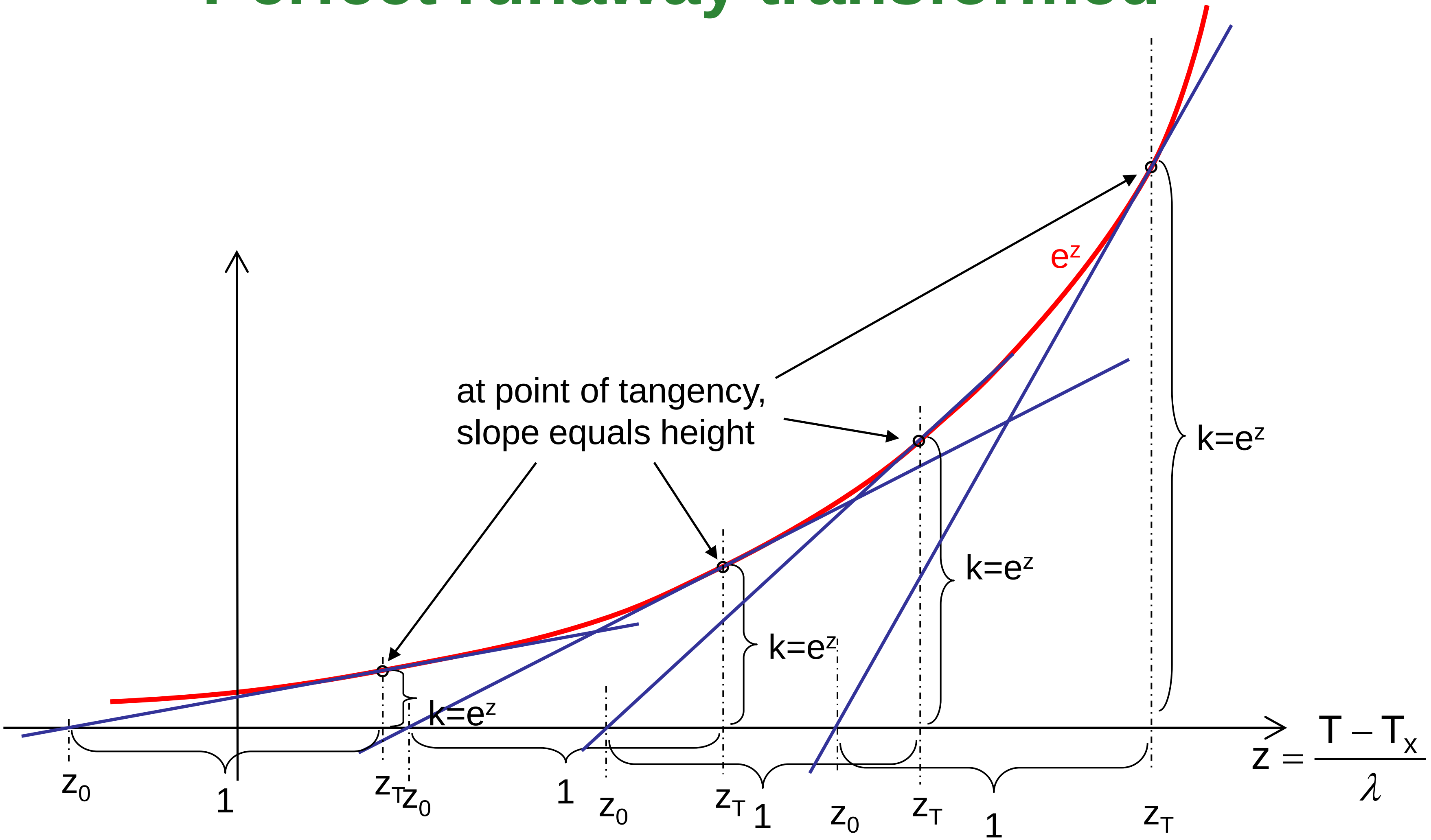
(power law device)

$$q = e^z$$

Eliminating q:

$$\boxed{kz = e^z}$$

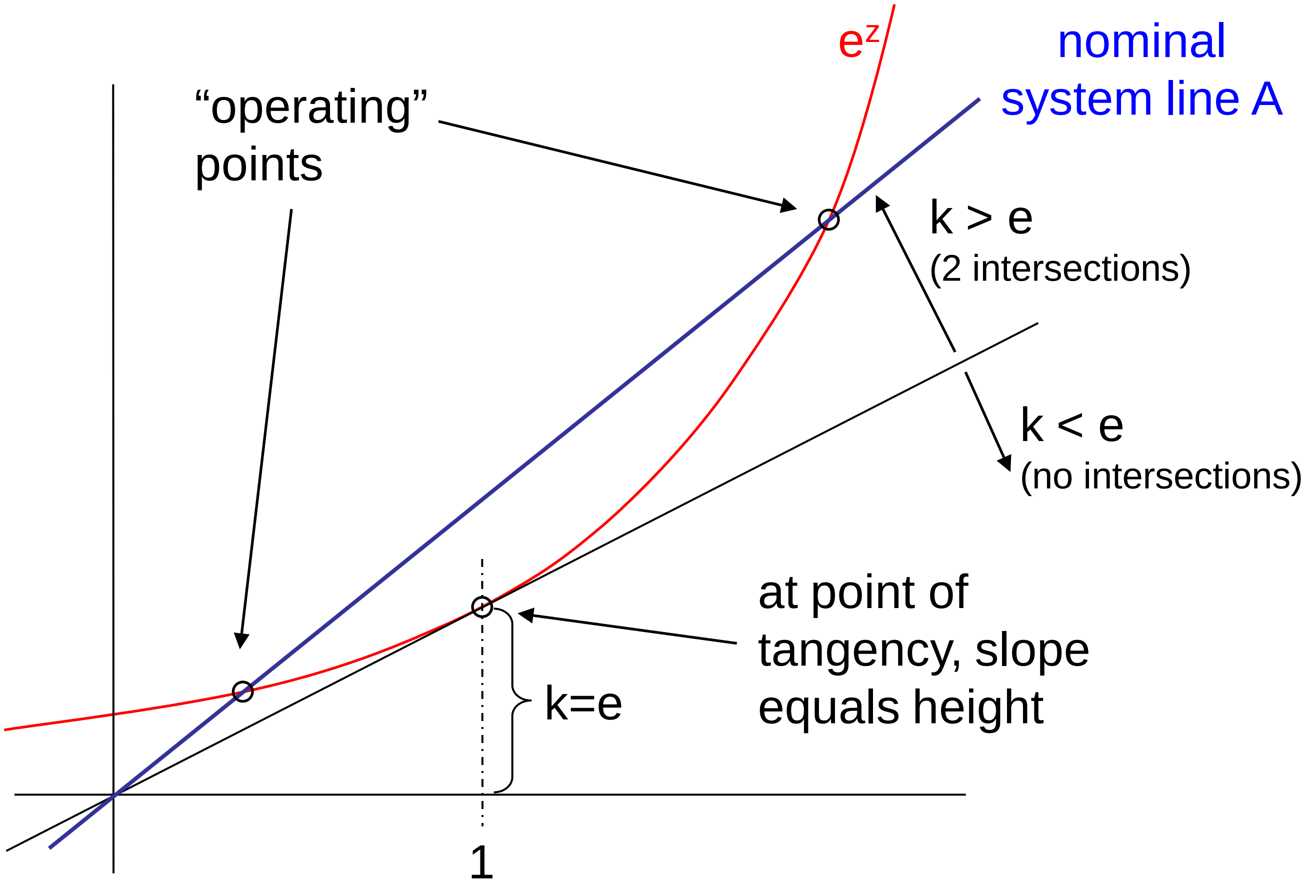
Perfect runaway transformed



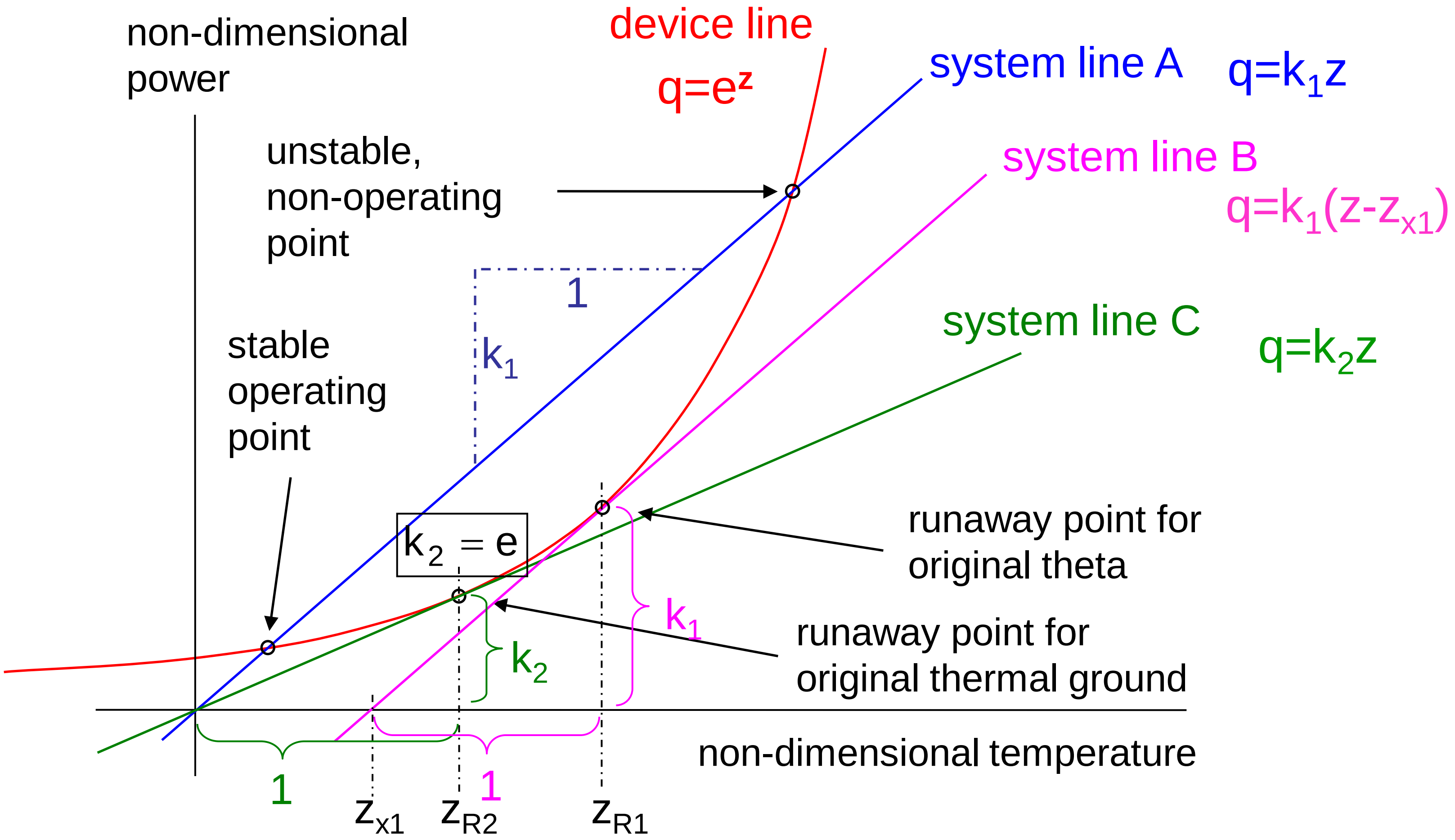
$$z = \frac{T - T_x}{\lambda}$$

$$\boxed{z_T - z_0 = 1}$$

Transforming the nominal system



Everything transformed



non-dimensional power

device line

$q=e^z$

system line A $q=k_1 z$

system line B $q=k_1(z-z_{x1})$

system line C $q=k_2 z$

unstable, non-operating point

stable operating point

$k_2=e$

runaway point for original theta

runaway point for original thermal ground

non-dimensional temperature

$z_{x1}=ln(k_1)-1$ $z_{R2}=1$ $z_{R1}=ln(k_1)$

“Perfect runaway” results in original terms

runaway temperature based on original slope

$$T_{R1} = \lambda \, ln\left(\frac{\lambda}{\theta_{Jx1} Q_o}\right)$$

runaway temperature based on original ambient

$$T_{R2} = T_x + \lambda$$

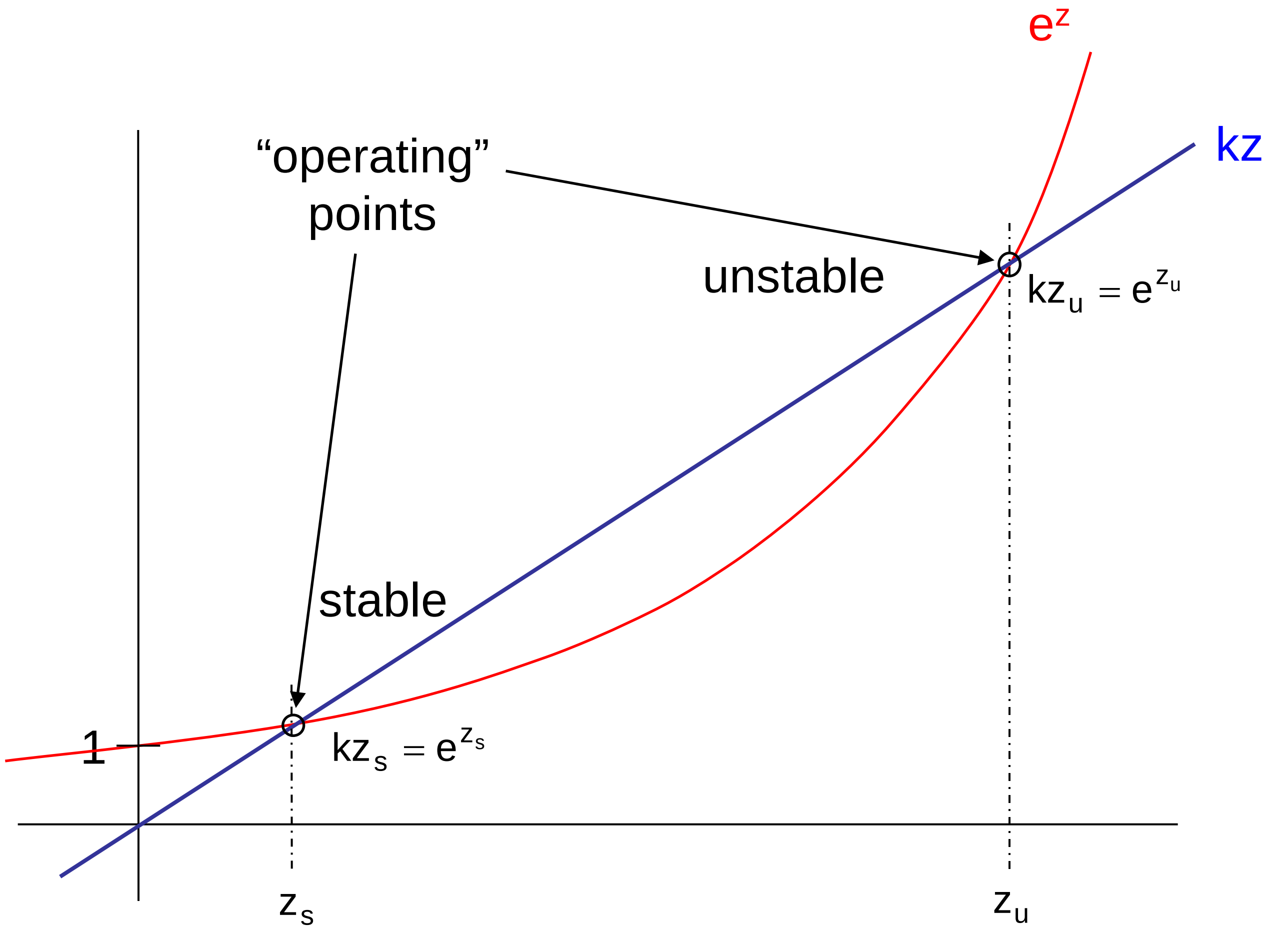
max ambient that goes with it

$$T_{x1} = \lambda \, ln\left(\frac{\lambda}{\theta_{Jx1} Q_o}\right) - \lambda$$

system resistance that goes with it

$$\theta_{Jx2} = \frac{\lambda}{Q_o} e^{-\left(\frac{T_x}{\lambda}+1\right)}$$

The “operating” points



Newton’s method for the intersections

$$z_{i+1} = z_i - \frac{-F(z_i)}{F'(z_i)}$$

$$kz = e^z$$

$$\ln kz = z$$

$$F(z) = z - \ln kz$$

$$F'(z) = 1 - \frac{1}{z}$$

$$z_{i+1} = \frac{\ln\left(\frac{k}{e} z_i\right)}{1 - \frac{1}{z_i}}$$

For k/e ranging between 1.01 and 1000, convergence is to a dozen significant digits in fewer than 10 iterations.

$$\boxed{z_o = \frac{1}{k} = \frac{1}{e \cdot \frac{k}{e}}}$$

this initial guess converges to lower, stable point

this initial guess converges to upper, unstable point

$$\boxed{z_o = \ln k = 1 + \ln\left(\frac{k}{e}\right)}$$

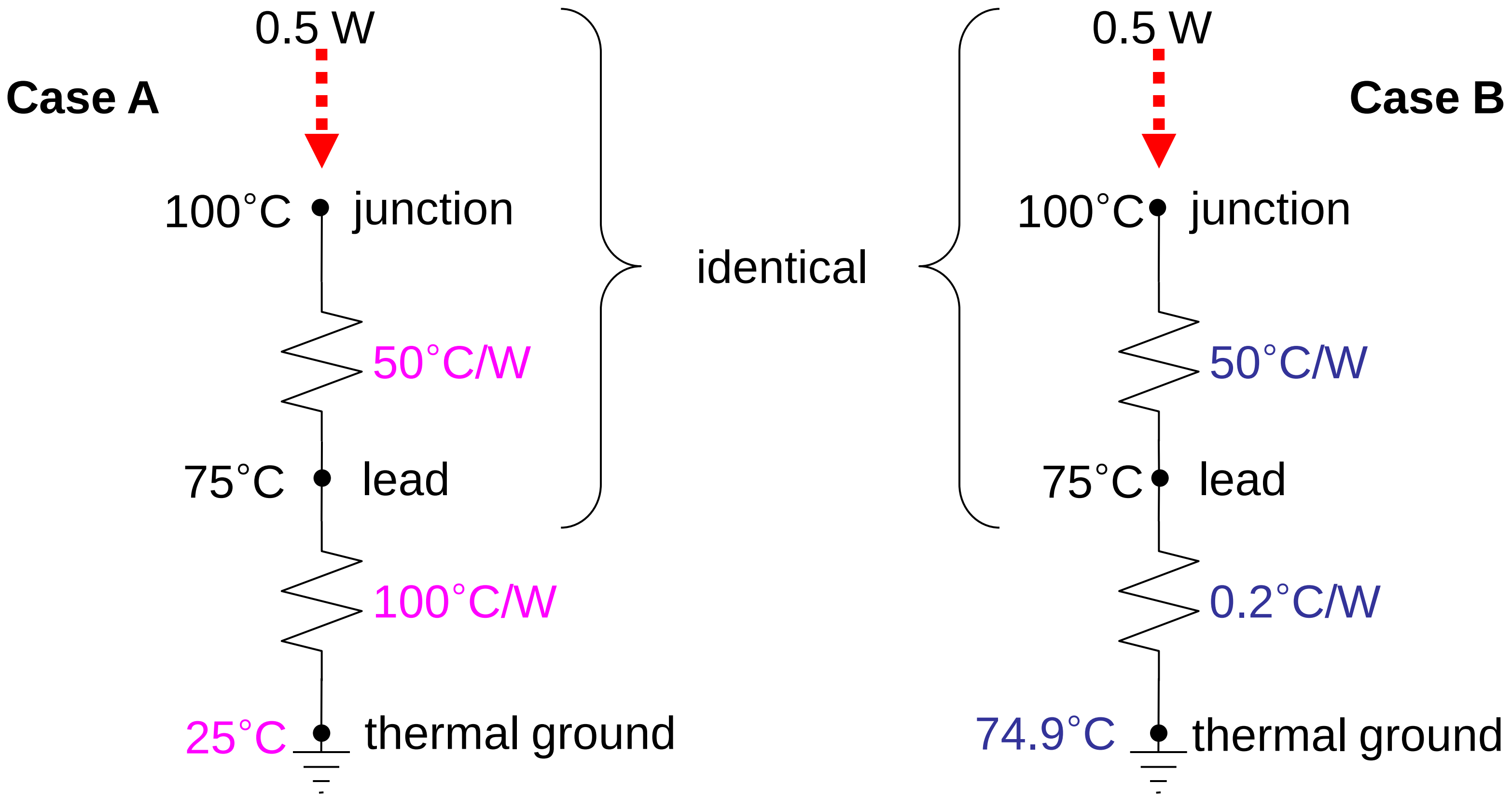
And the intersection points come from …

find the non-dimensional intersections first, then

$$T_{stable} = T_x + \lambda \cdot z_{stable}$$

$$T_{unstable} = T_x + \lambda \cdot z_{unstable}$$

A paradox



Case A

0.5 W

100°C junction

50°C/W

75°C lead

100°C/W

25°C thermal ground

identical

Case B

0.5 W

100°C junction

50°C/W

75°C lead

0.2°C/W

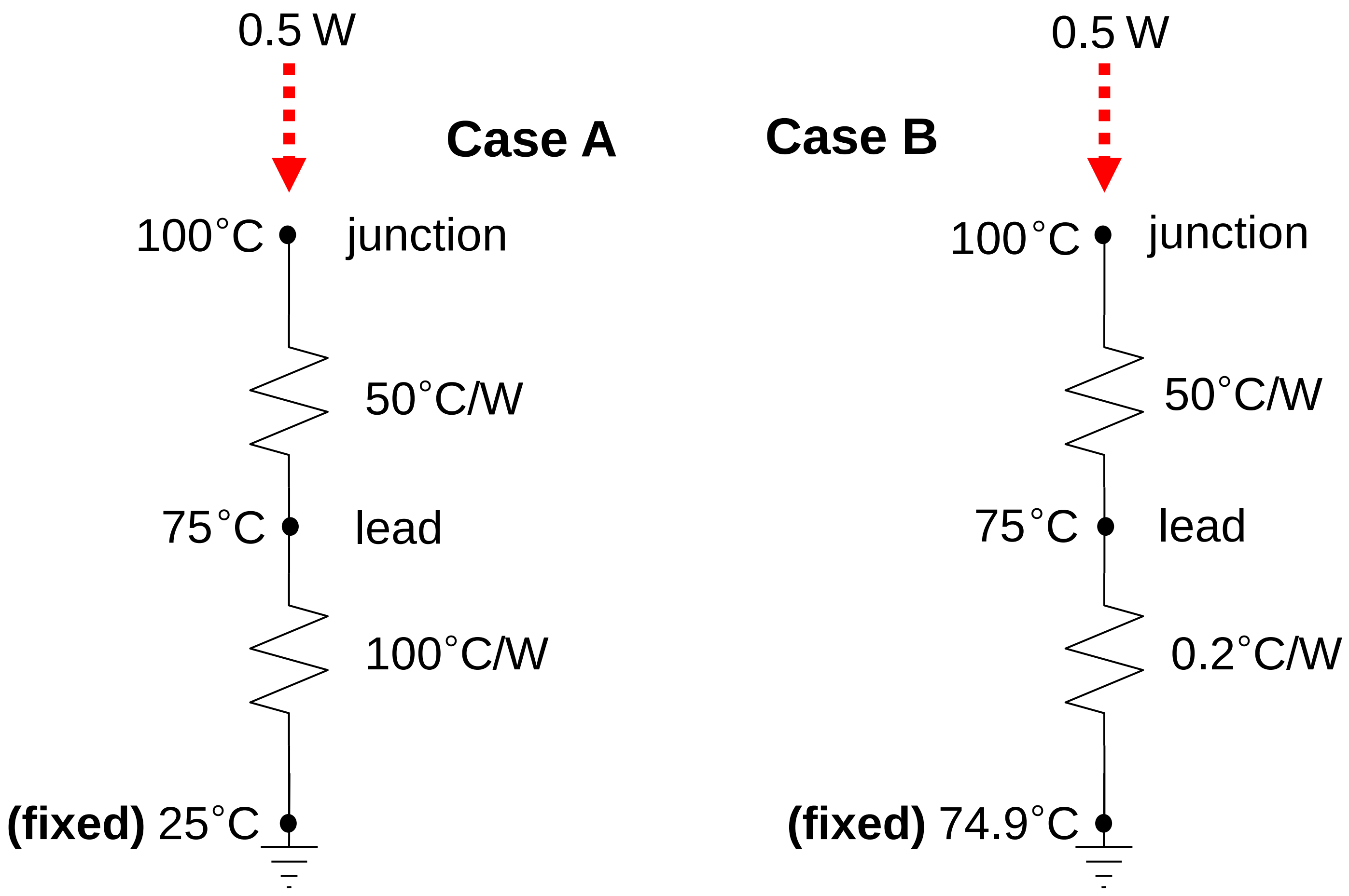
74.9°C thermal ground

thermal runaway,
based on θ_{Jx}=150°C/W,
calculated to be at **125°C**

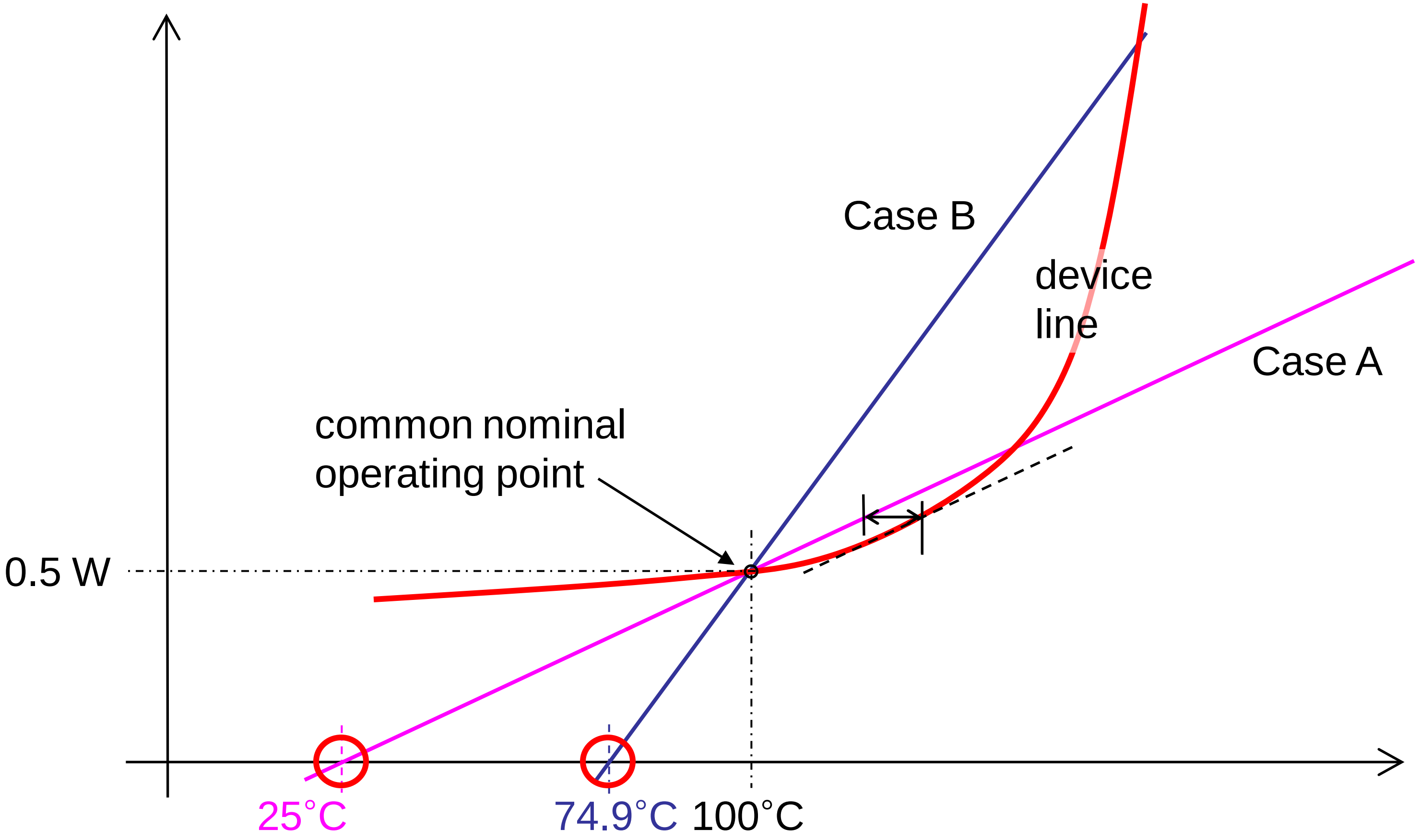
thermal runaway,
based on θ_{Jx}=50.2°C/W,
calculated to be at **150°C**

Paradox lost

raise the power by 0.1 W and see what happens



Illustrating the paradox



Real datasheet example

raw device data[†]

V_r [V]	12	40
T_{max} [°C]	125	125
T_{ref} [°C]	75	75
I_{tmax} [A]	8.50E-3	2.80E-2
I_{tref} [A]	5.20E-4	1.70E-3

$$I = I_0 e^{\frac{T}{\lambda}}$$

the device power curve parameters

	@12V	@40V
λ [°C]	17.9	17.8
Q_o [W]	9.4E-5	1.02E-3

$$\lambda = \frac{T_{max} - T_{ref}}{ln\left(I_{max} / I_{ref}\right)}$$

rule of thumb gave us: $= \dfrac{10}{ln(2)} = 14.4$

$$I_0 = I_{t\,max} e^{-\frac{T_{max}}{\lambda}} = I_{tref} e^{-\frac{T_{ref}}{\lambda}}$$

$$Q_0 = V_R I_0$$

[†] **MBRS140T3**

Runaway analysis in nominal system

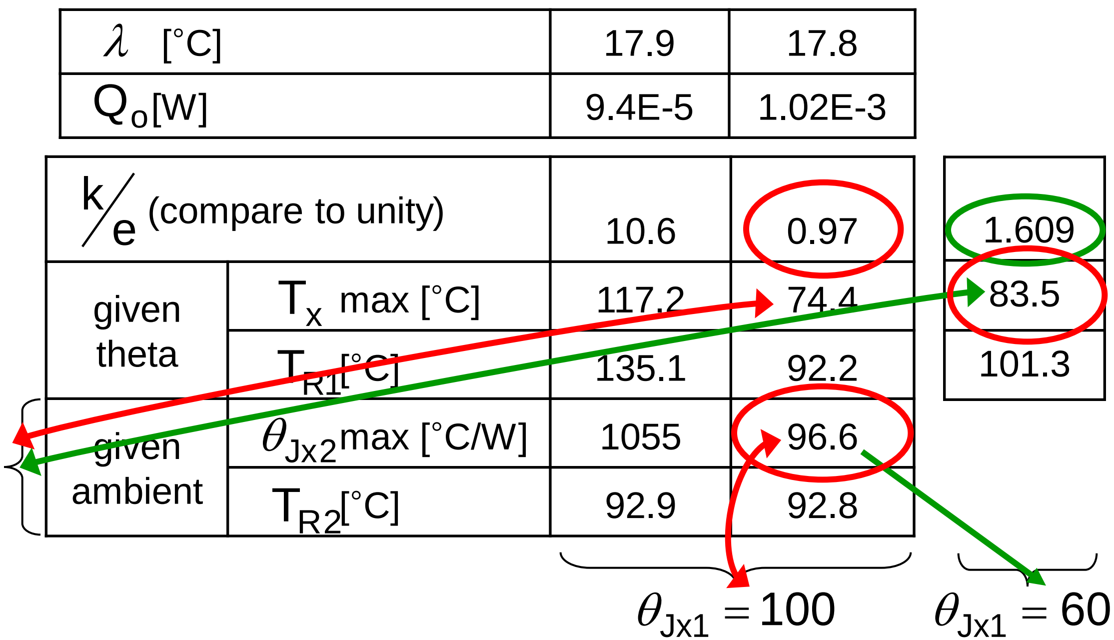
raw device data[†]

V_r [V]	12	40
T_{max} [°C]	125	125
T_{ref} [°C]	75	75
I_{tmax} [A]	8.50E-3	2.80E-2
I_{tref} [A]	5.20E-4	1.70E-3

$$\frac{k}{e} = \frac{\lambda}{\theta_{Jx} Q_o} e^{\frac{-T_x}{\lambda} - 1}$$

$$T_x = 75$$

computed results



		@12V	@40V	@40V
λ [°C]		17.9	17.8	
Q_o[W]		9.4E-5	1.02E-3	
k/e (compare to unity)		10.6	0.97	1.609
given theta	T_x max [°C]	117.2	74.4	83.5
	T_{R1}[°C]	135.1	92.2	101.3
given ambient	θ_{Jx2}max [°C/W]	1055	96.6	
	T_{R2}[°C]	92.9	92.8	

$\theta_{Jx1} = 100$

$\theta_{Jx1} = 60$

These translate into:

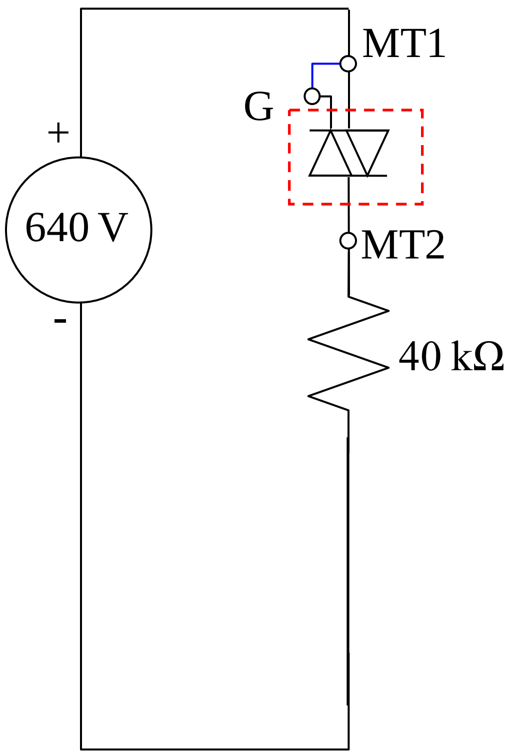
a stable operating point at 80.6°C (and 0.09 W), ← $z = 0.312$

an unstable point at 116.3°C (0.69 W) ← $z = 2.315$

[†] **MBRS140T3**

HTRB example

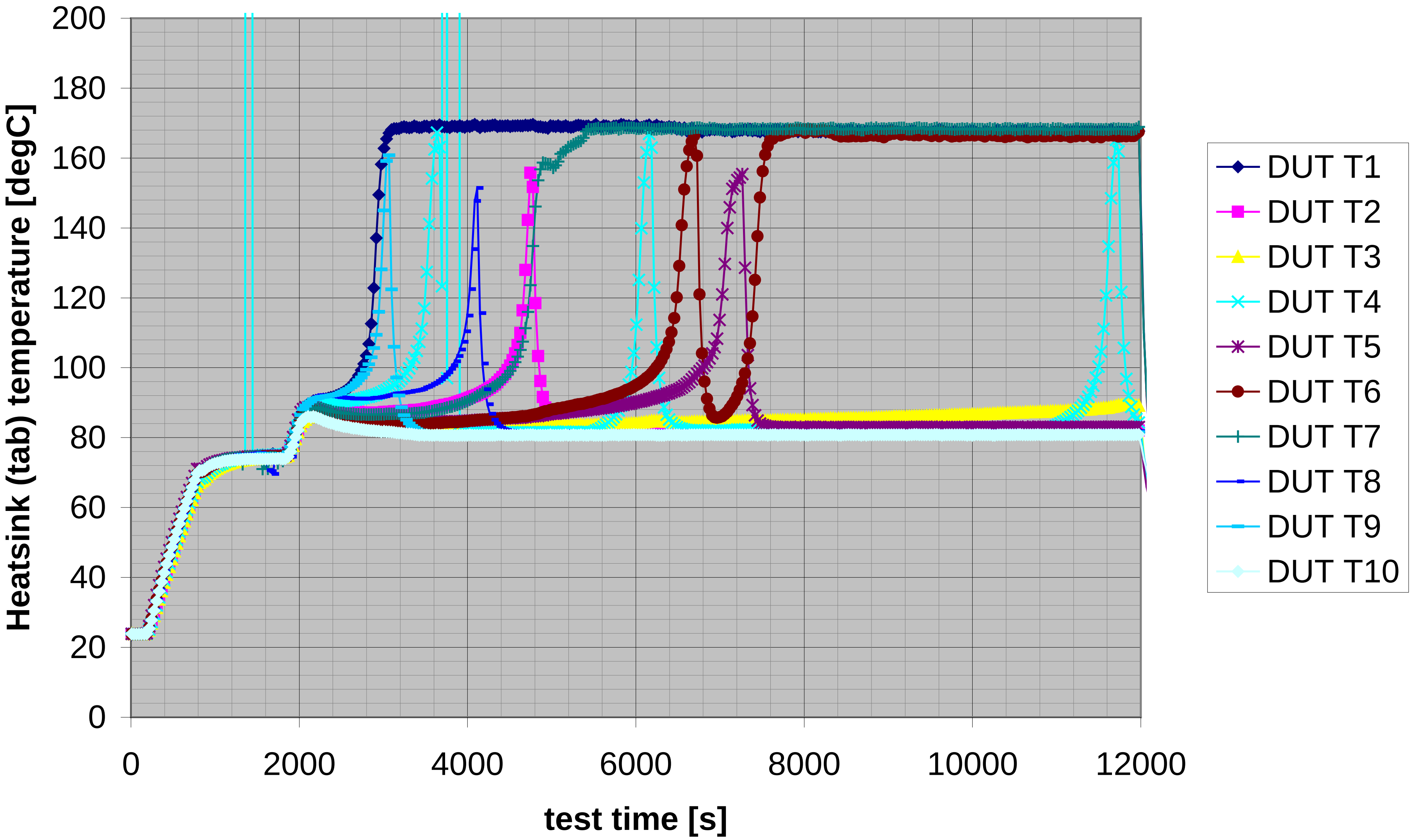
- Bidirectional Thyristor in reliability stress test (High Temperature Reverse Bias)
- Goal is life tests at elevated temperature (say 125°C)
- Problem is, they don't last very long, and if junction temperature is anything like the chamber temperature, they appear to fail way too early good!



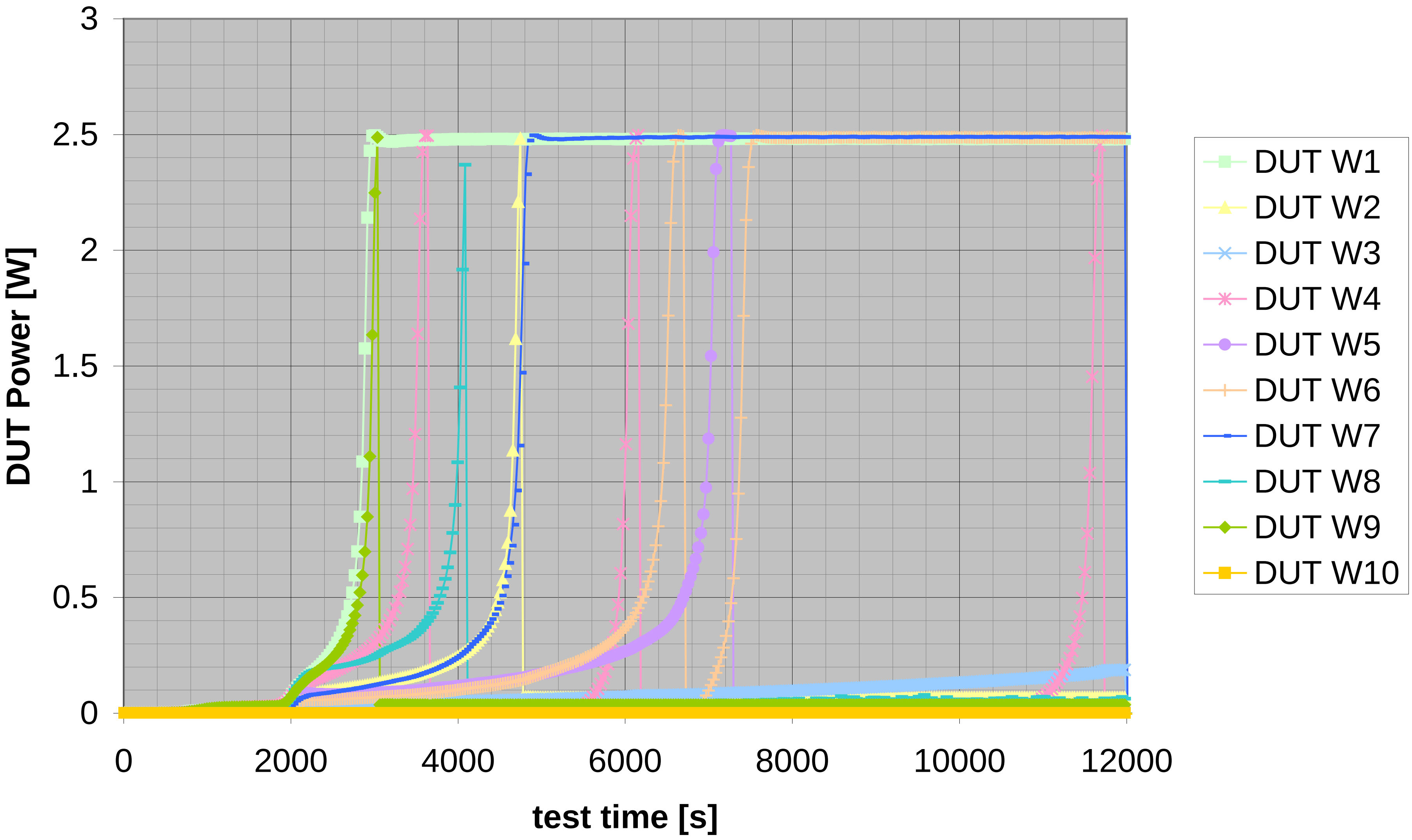
HTRB test circuit

*Special acknowledgements to Dave Billings and Geoff Garcia for their contributions to this project

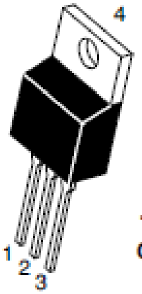
HTRB DUT tab temperature vs. test time



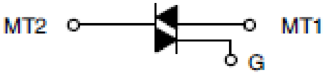
HTRB DUT power vs. test time



HTRB example



TO-220AB
CASE 221A
STYLE 4



THERMAL CHARACTERISTICS

Characteristic		Symbol	Value	Unit
Thermal Resistance,	Junction-to-Case Junction-to-Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.1 60	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 10 seconds		T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted; Electricals apply in both directions)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Peak Repetitive Blocking Current (V_D = Rated V_{DRM}, V_{RRM}; Gate Open)	T_J = 25°C T_J = 125°C	I_{DRM}/ I_{RRM}	– –	– –	0.005 2.0	mA

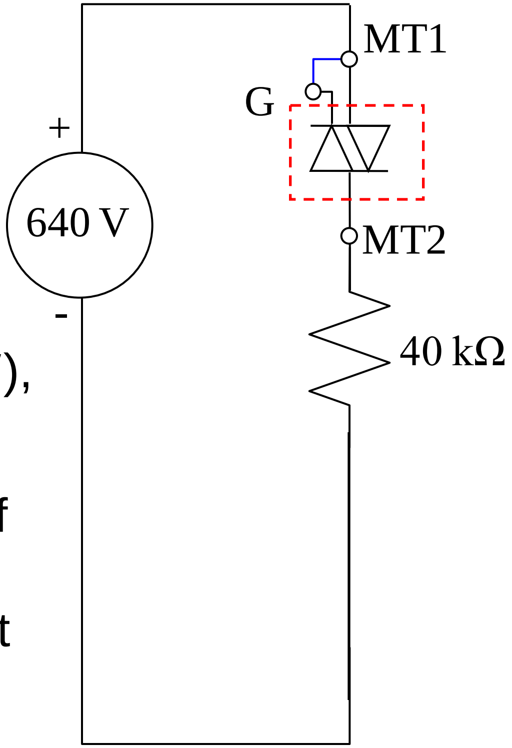
Quick calculations from datasheet

$$P_d = I \cdot (640 - 40000 \cdot I)$$

$$T_J = T_a + P_d \cdot \theta_{JA}$$

or

$$T_J = T_{HS} + P_d \cdot \theta_{J-HS}$$



HTRB test circuit

- At room temp, if I_{DRM} is 5 uA, then P_d is about zero (≈3mW), and T_J should thus equal chamber set point.
- At 85°C, I_{DRM} is about 0.1-0.2mA, thus P_d is on the order of 0.1W, so depending on theta-JA, T_J could be several degrees hotter than chamber set point (note, however, that T_J will still be well within 1°C of heatsink temperature, T_{HS})
- HOWEVER, at 125°C, if I_{DRM} is 2mA, then P_d will be in excess of 1W. Depending on theta-JA, T_J could be 30-60°C above chamber set point (though still within a couple of degrees of heatsink temperature, if known).

Calculations based on actual measurements

$$P_d = I \cdot (640 - 41000 \cdot I)$$

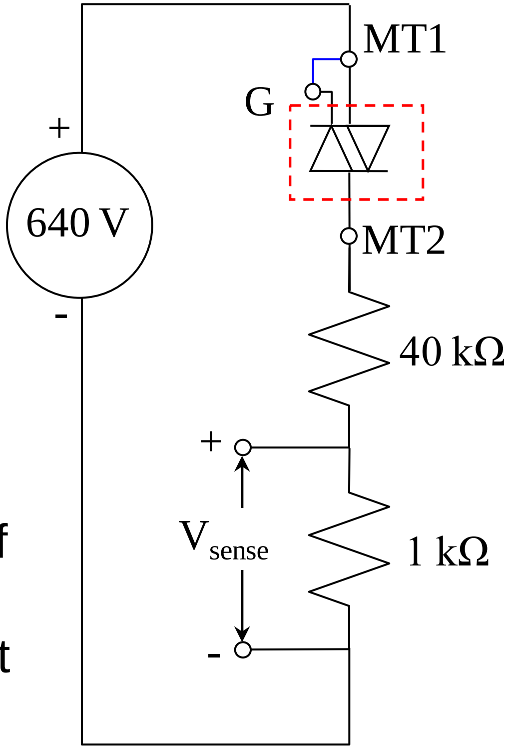
$$I = \frac{V_{sense}}{1000}$$

$$T_J = T_a + P_d \cdot \theta_{JA}$$

or

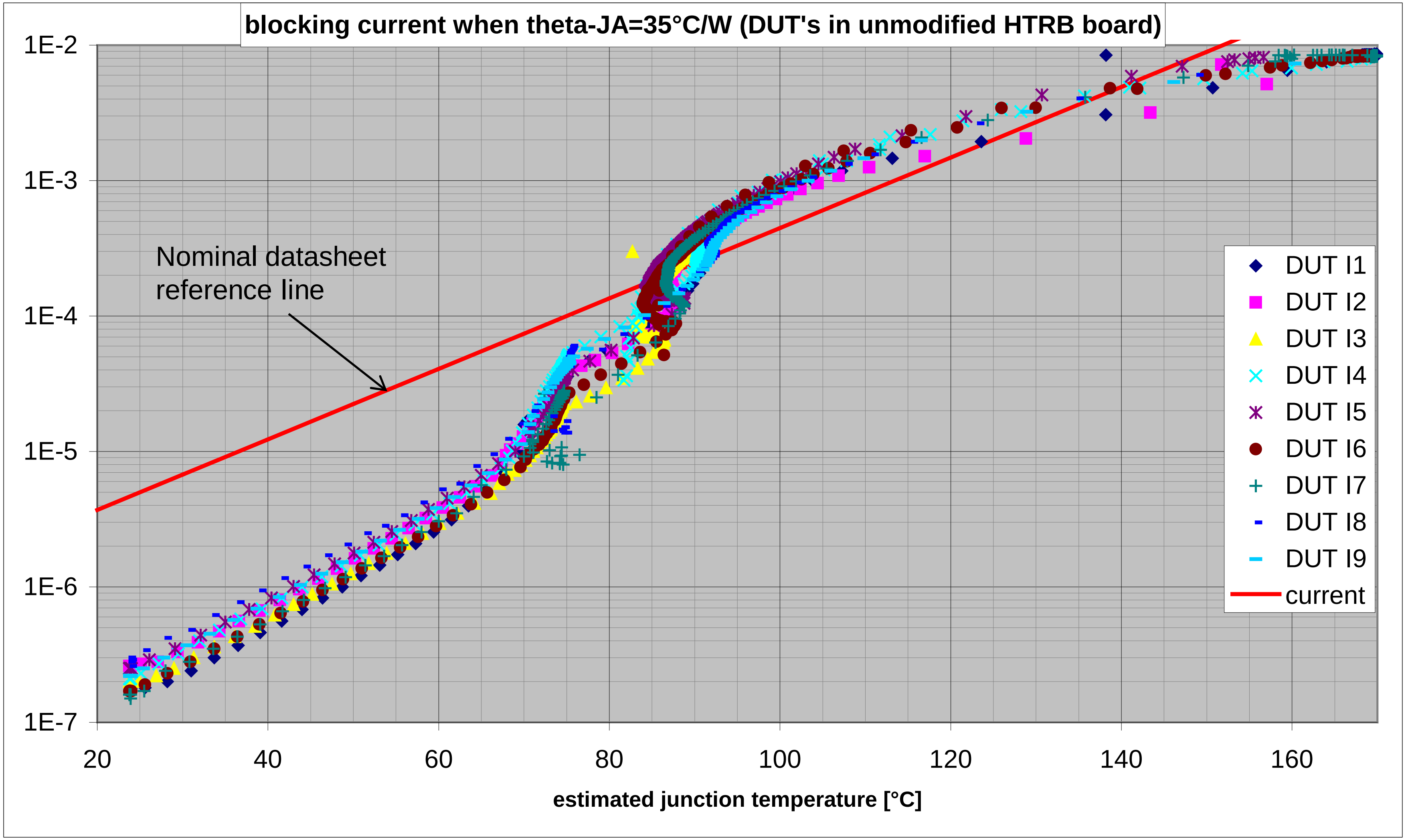
$$T_J = T_{HS} + P_d \cdot \theta_{J-HS}$$

- At room temp, I_{DRM} (via V_{sense}) is 0.2uA, thus P_d is about zero (≈0.1mW), and T_J should thus equal chamber set point.
- At 85°C, I_{DRM} is about 0.1-0.2mA, thus P_d is on the order of 0.1W, so depending on theta-JA, T_J could be several degrees hotter than chamber set point (note, however, that T_J will still be well within 1°C of heatsink temperature, T_{HS})
- At 125°C, I_{DRM} is 2-3mA; P_d could be as high as 1.5W
- Max current observed was nearly 8mA (for P_d of 2.5W), and estimated T_J of 170°C just prior to device failure.



Modified HTRB test circuit

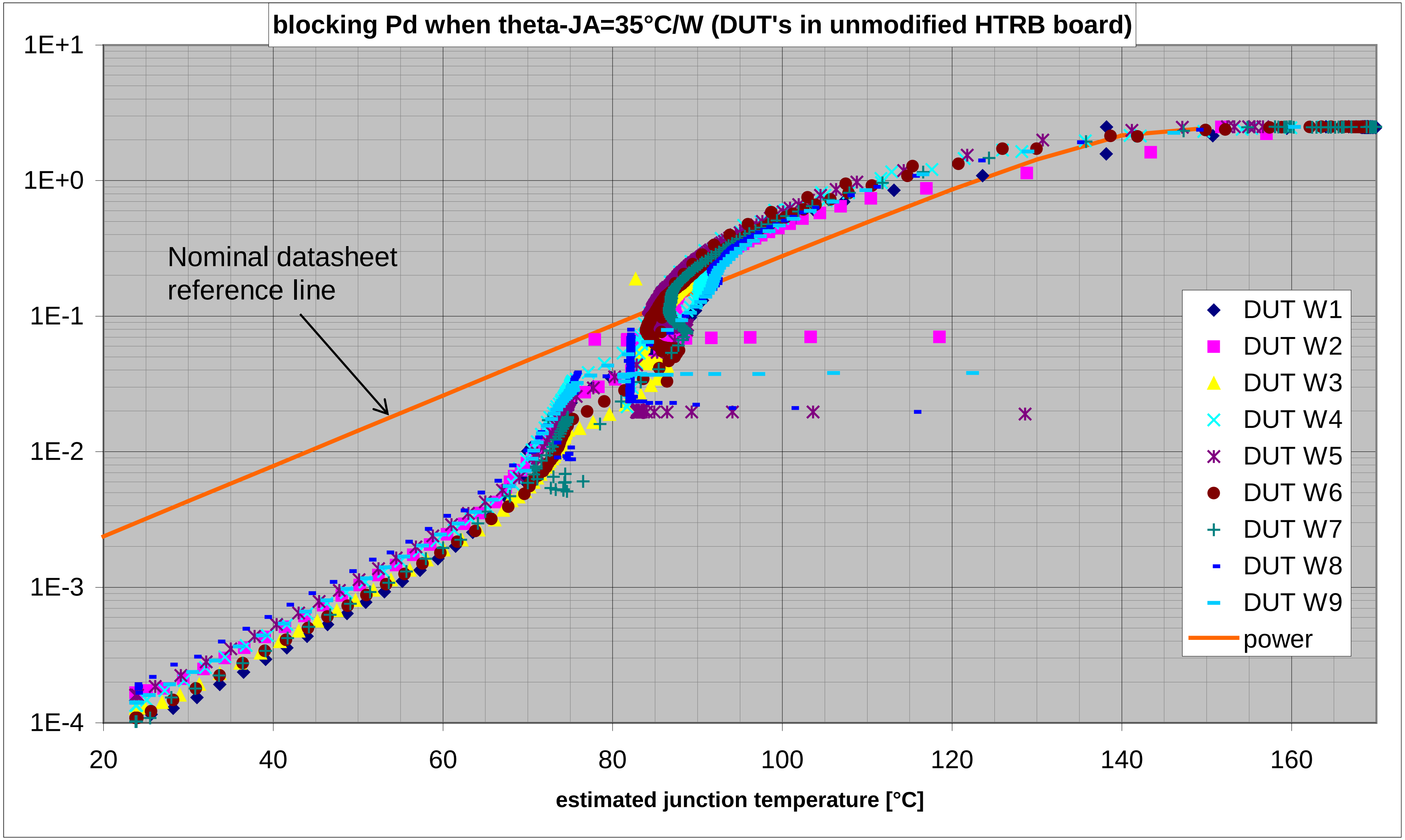
Actual “blocking current” data (time implicit)



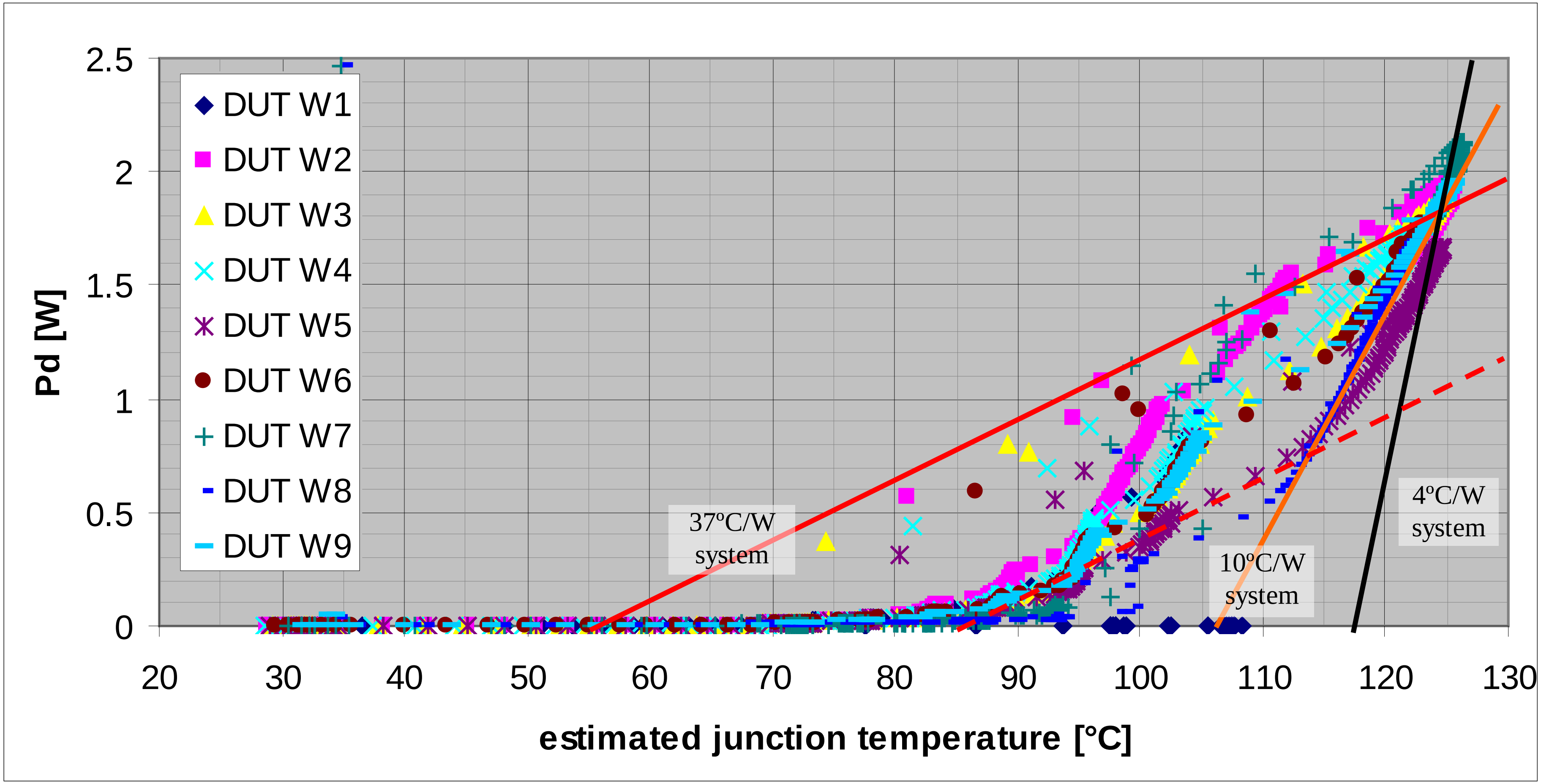
blocking current when theta-JA=35°C/W (DUT's in unmodified HTRB board)

Nominal datasheet reference line

Actual “blocking P_d” data (time implicit)

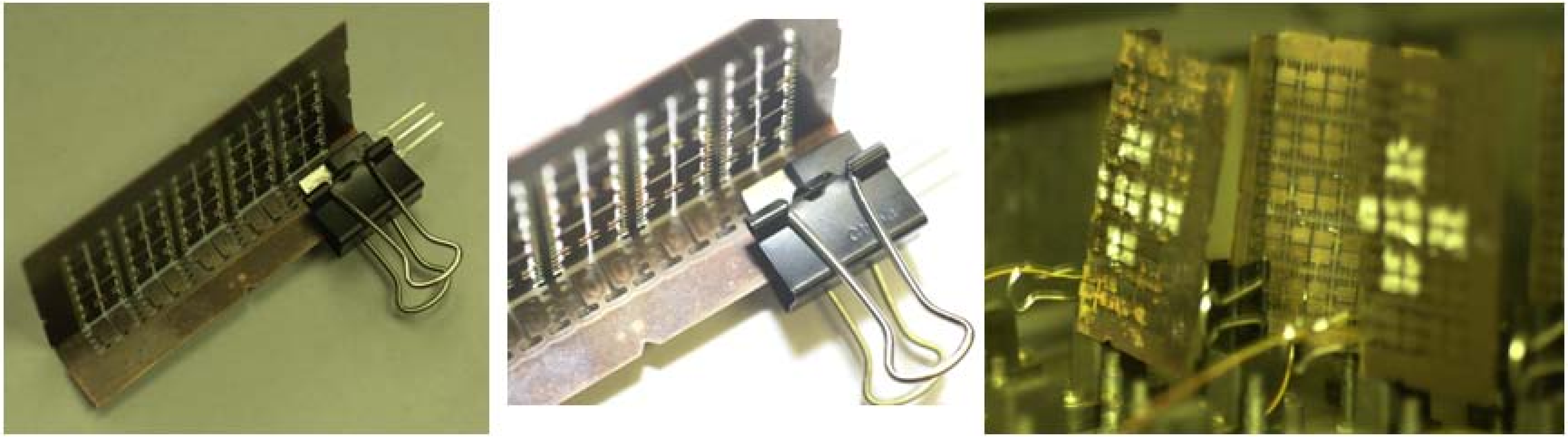


Power vs. temperature (linear scales)

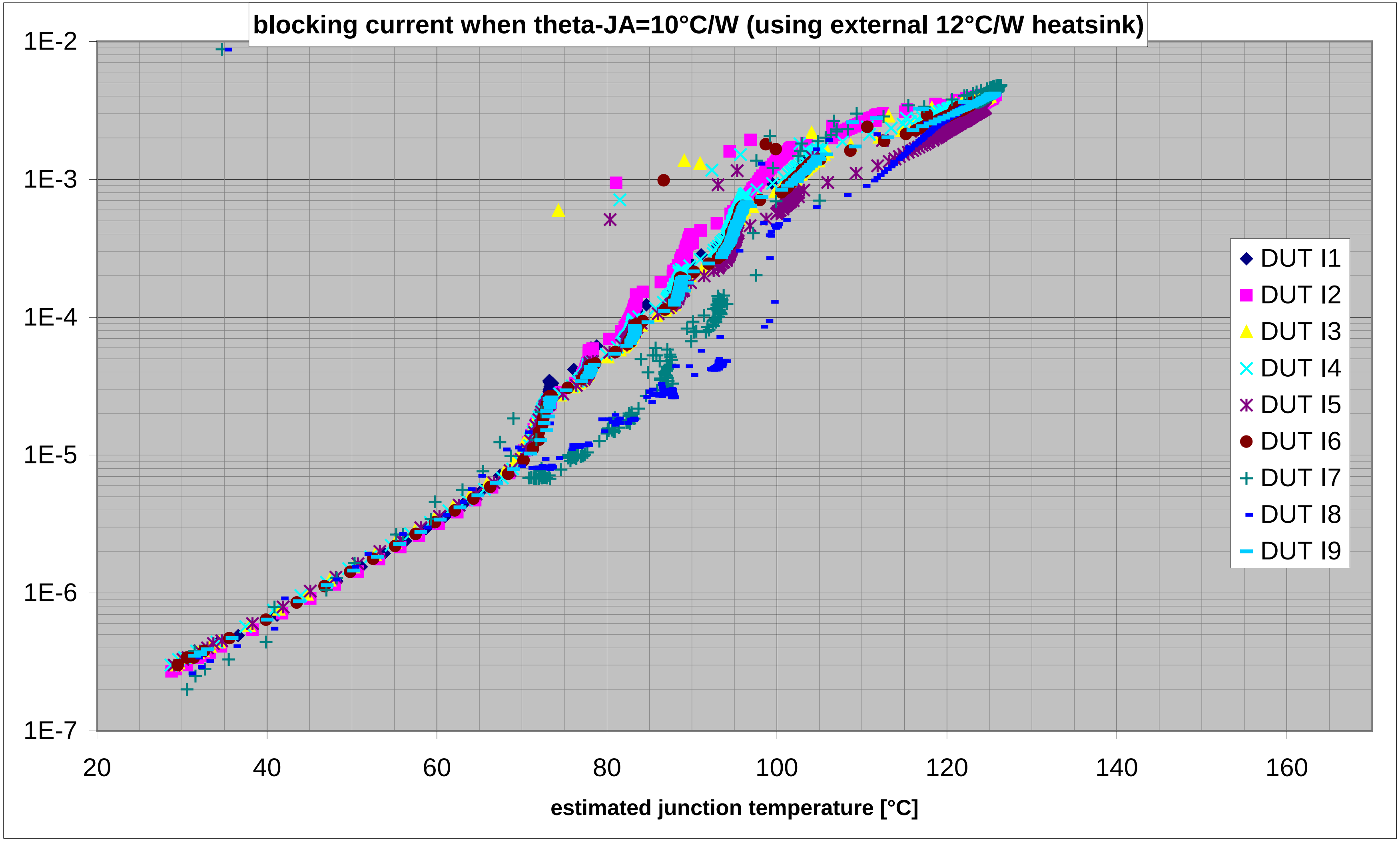


Proof-of-concept modified HTRB fixture

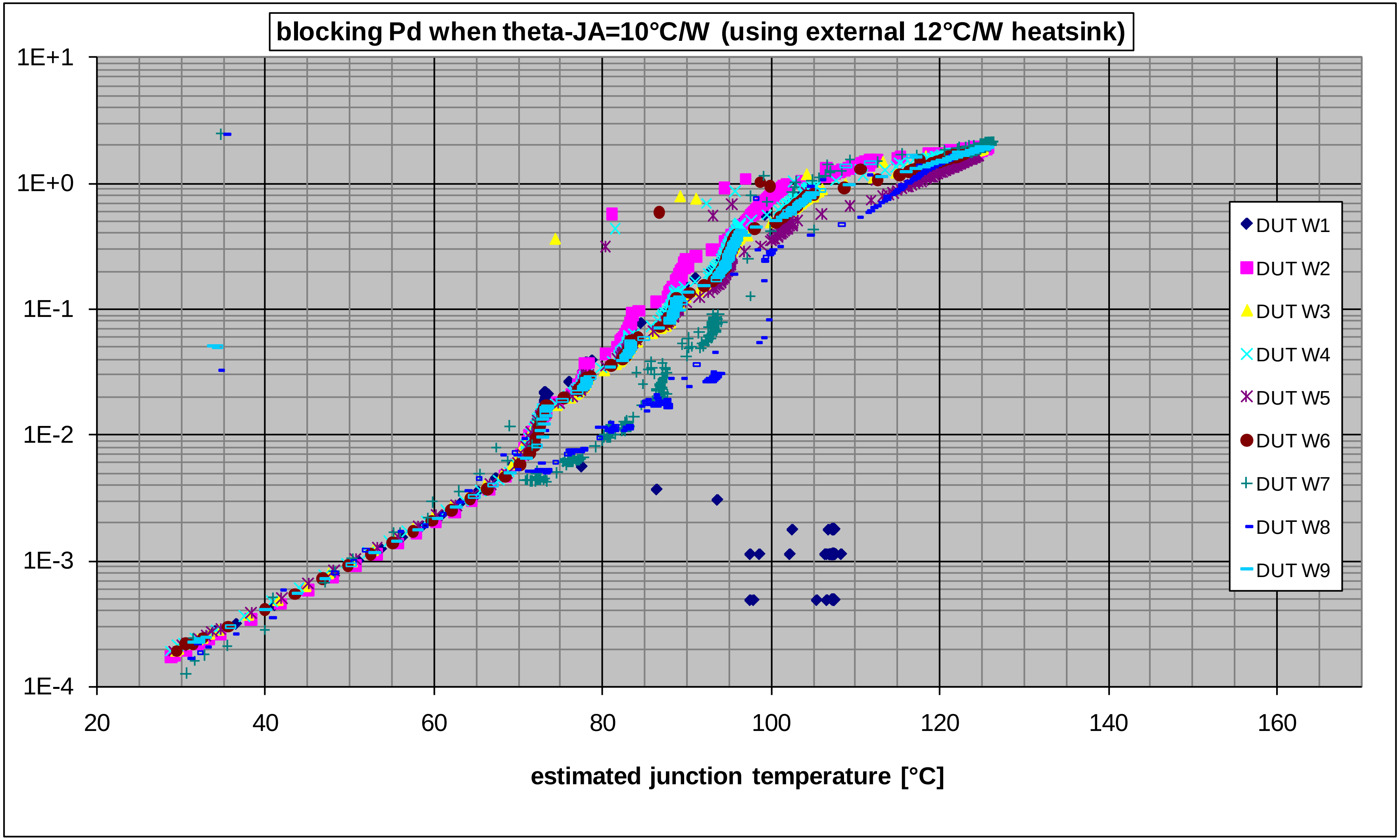
After observing a number of device failures at unacceptably short times and under what would have been expected to be junction temperatures well below the maximum rated temperature, the hypothesis of “thermal runaway” in the chamber became the favored explanation of the failures. If true, then lowering the theta-JA of the devices should provide some margin for avoiding the problem. Consequently, crude heatsinks were constructed from some handy copper test panels and attached to each of nine additional test specimens.



I vs. temperature on better heatsinks



P_d vs. temperature on better heatsinks



Thus, to obtain a net theta-JA of 4°C/W, one needs a net 2°C/W resistance from tab to ambient. A finite element model was constructed of a four-finned heatsink that would easily fit in the available space for each of 10 devices in a row of the current HTRB chambers. Figure 9 depicts this heatsink.

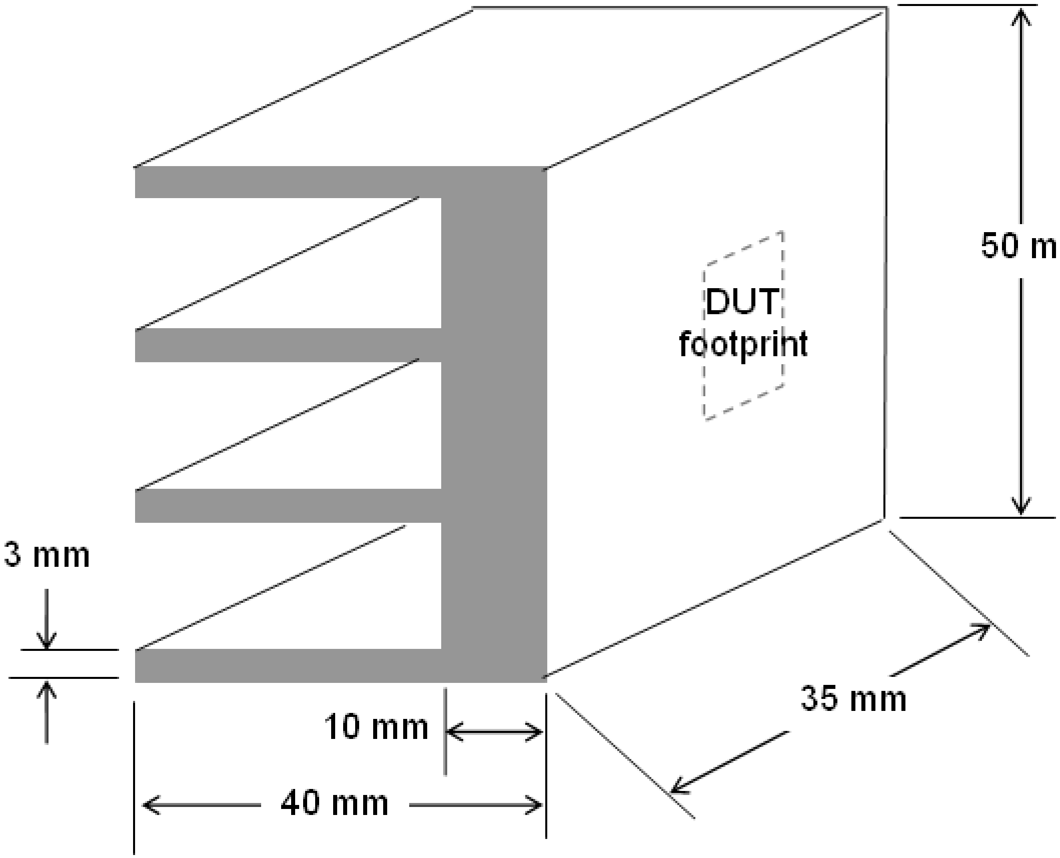


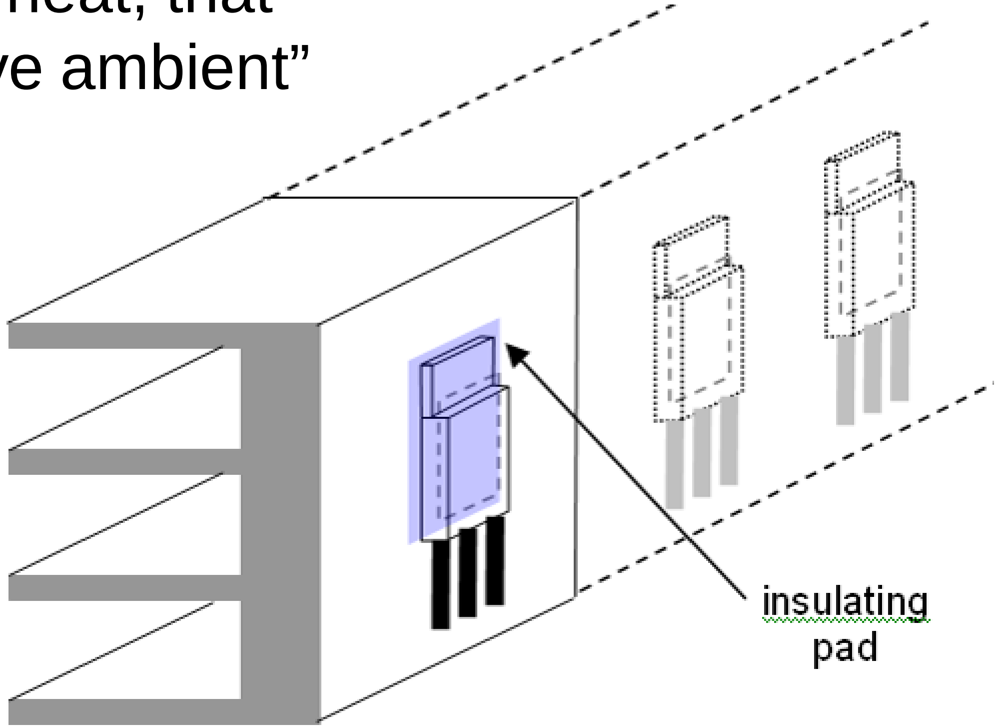
Figure 9 – A possible 1.9°C/W heatsink

Using a film coefficient of 40 W/m²/°C, this heatsink would have a convection resistance of 1.9°C/W.

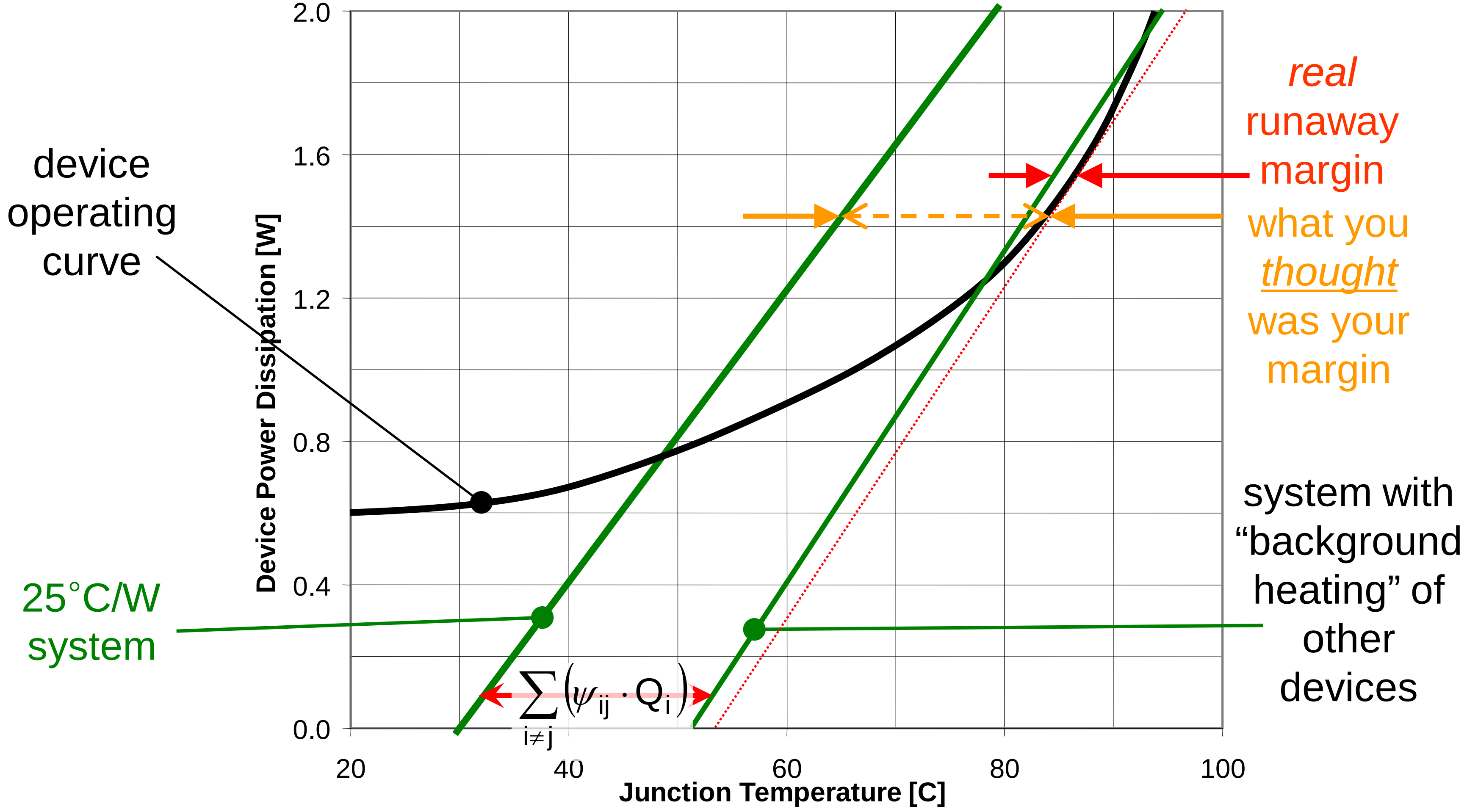
What if multiple devices on heatsink?

- Each device heats its neighbors to varying degrees, depending on distance

- This adds background heat, that is, it raises the “effective ambient” of each device



Graphically, background heat does this



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